

2008 EDN Microcontroller/Microprocessor Directory

32-bit microprocessors sorted by company

Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Actel Corporation www.actel.com	CoreMP7	ARM7TDMI-S	29	AHB 32/32	16, 32	1.5 / 1.5, 1.8, 2.5, 3.3	FPGA dependent (core)	User-added	Yes		Can add external to core
Altera www.altera.com	Excalibur: EPXA1 EPXA4 EPXA10	ARM V4T	133, 166, 200	32/32	16, 32	1.8, 2.5, 3.3	2W, FPGA-dependent	Low power (EPXA1)	32x8 user-definable	Can add in FPGA	8-kbyte instruction/data
Altera www.altera.com	Nios II/e (economy soft core)	Nios II	Over 200	32/32 (dynamic sizing)	32	1.2, 1.5		User-added	370-MHz user-definable MAC (9x9, 18x18, or 36x36)	Can add accelerator block	
Altera www.altera.com	Nios II/f (fast soft core)	Nios II	Over 180	32/32 (dynamic sizing)	32	1.2, 1.5		User-added	370-MHz user-definable MAC (9x9, 18x18, or 36x36)	Can add accelerator block	Configurable up to 64-kbyte instruction/data
Altera www.altera.com	Nios II/s (standard soft core)	Nios II	Over 160	32/32 (dynamic sizing)	32	1.2, 1.5		User-added	370-MHz user-definable MAC (9x9, 18x18, or 36x36)	Can add accelerator block	Configurable up to 64-kbyte instruction/data
Altera www.altera.com	Nios (soft core)	Nios	Over 125	16/16, or 32/32	16	1.5, 1.8, 2.5, 3.3, 5		User-added	250-MHz 36x36 DSP block, two-cycle 16x16, 1-bit/clock, user-definable	Can add accelerator block	Configurable 1- to 16-kbyte instruction/data, direct mapped, write-through
Altium www.altium.com	TSK3000 (Standard and JTAG enabled softcore)	TSK3000	Over 50	32/32	32	1.5, 1.8, 2.5, 3.3, 5	Device-dependent		31x31		
AMCC www.amcc.com	PowerPC 405CR	PowerPC	133 to 266	32	32	2.5/3.3	0.8W (200MHz)		16x16 MAC		16/8-kbyte instruction/data
AMCC www.amcc.com	PowerPC 405EP	PowerPC	133 to 333	32	32	1.8/3.3	0.76W		16x16 MAC		
AMCC www.amcc.com	PowerPC 405EX	PowerPC	400 to 600	32	32	1.2/2.5/3.3	1.9W	Three levels	16x16 MAC		16-kbyte instruction/data
AMCC www.amcc.com	PowerPC 405EXr	PowerPC	333 to 533	32	32	1.2/2.5/3.3	1.75W	Three levels	16x16 MAC		16-kbyte instruction/data
AMCC www.amcc.com	PowerPC 405GP	PowerPC	133 to 266	32	32	2.5/3.3	1.5W (200MHz)		16x16 MAC		16/8-kbyte instruction/data
AMCC www.amcc.com	PowerPC 405GPr	PowerPC	266 to 400	32	32	1.8/3.3	0.72W (266MHz)		16x16 MAC		16-kbyte instruction/data
AMCC www.amcc.com	PowerPC 440EP	PowerPC	333 to 667	32	32	1.5/2.5, 3.3	3W (533MHz)		16x16 MAC	Double precision, five stage with 2.0 MFLOPS/MHz	32-kbyte instruction/data
AMCC www.amcc.com	PowerPC 440EPx	PowerPC	400 to 667	32/64	32	1.5/2.5, 3.3	<4W		16x16 MAC	Double precision, five stage with 2.0 MFLOPS/MHz	32-kbyte instruction/data
AMCC www.amcc.com	PowerPC 440GP	PowerPC	333 to 500	32/64	32	1.85/2.5, 3.3	<4W		16x16 MAC		32-kbyte instruction/data

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
Up to 1-Mbyte Flash on-chip and up to 4-Gbyte external	Can add external		IP core	User Configurable 16 or 32-bit timers, PWM, watchdog	User configurable UART, GPIO, SPI, I ² C, PCIF, 10/100 Ethernet	IRQ, FIQ configurable	Can be used with 12-bit ADC on Fusion FPGAs	-40 to +125	Live at power up, reprogrammable or radiation tolerant block	Free in Actel FPGAs to no license fees or royalties
32- to 256-kbyte SRAM, 16- to 128-kbyte dual-port SRAM	SDRAM, Flash	Dual 64-entry TLB	484/672/1020 FBGA	32-bit, watchdog	Configurable number of UART, up to 170 GPIO, SPI, IDE, PCI, 10/100 Ethernet	3 modes, 6 sources, 31 or 63 levels		0 to +70 -40 to +85	4/16/38K FPGA logic elements, two AMBA AHB bus bridges, JTAG debug, ETM9 trace	\$40 to \$500
Up to nine 64-kbyte RAM blocks	SRAM, SSRAM, SDRAM, DDR SDRAM, CFI Flash		IP core	32-bit, watchdog, PWM, configurable	RS-232, SPI, GPIO, IDE, PCI, JTAG, Ethernet, DMA, Compact Flash	32		N/A (Core)	Over 30 DMIPs, 256 custom instructions, unlimited hardware accelerators, over 60 available peripherals	From 35 cents; royalty to free in Altera FPGAs; ASIC license
Up to nine 64-kbyte RAM blocks	SRAM, SSRAM, SDRAM, DDR SDRAM, CFI Flash		IP core	32-bit, watchdog, PWM, configurable	RS-232, SPI, GPIO, IDE, PCI, JTAG, Ethernet, DMA, Compact Flash	32		N/A (Core)	Over 200 DMIPs, 256 custom instructions, unlimited hardware accelerators, over 60 available peripherals	From \$1.12; royalty to free in Altera FPGAs; ASIC license
Up to nine 64-kbyte RAM blocks	SRAM, SSRAM, SDRAM, DDR SDRAM, CFI Flash		IP core	32-bit, watchdog, PWM, configurable	RS-232, SPI, GPIO, IDE, PCI, JTAG, Ethernet, DMA, Compact Flash	32		N/A (Core)	Over 125 DMIPs, 256 custom instructions, unlimited hardware accelerators, over 60 available peripherals	From 78 cents; royalty to free in Altera FPGAs; ASIC license
Up to 12 64-kbyte RAM blocks, multiple configuration register file	SRAM, SSRAM, SDRAM, Flash		IP core	32-bit, watchdog, PWM, configurable	Configurable, RS-232, SPI, GPIO, IDE, PCI, Ethernet	Up to 64, configurable		N/A (Core)	Custom instructions, hardware accelerators, simultaneous multiple master bus	Royalty to free license in Altera PLDs; ASIC license
Up to 16-Mbyte RAM blocks	SRAM, SDRAM		IP core	64-bit block, 32-bit PIT	CAN/RS232, EMAC, I ² C, LCD, Serial Flash, Configurable IO Port, PS2, SPI, RS-232, SPI, VGA, BT656 Analog Video, External Timer, Ethernet, DMA, JTAG	32		N/A (Core)	JTAG enabled on-chip debug interface, over 50 DMIPs, over 59 available peripherals	
	2-channel DMA, SRAM, SDRAM	Yes	316/413/456 PBGA	Yes	10/100 Ethernet, two UART, I ² C, GPIO, UIC, CodePack	7 external, 19 internal		-40 to +85	Single cycle access on-chip SRAM	\$12.00 to \$27.50
4-kbyte external	2-channel DMA, SRAM, SDRAM	Yes	385 PBGA, RoHS-compliant	Yes	Two UART, I ² C, GPIO, UIC, two 10/100 Ethernet	7 external, 19 internal		-40 to +85		\$9.50 to \$20.25
	4-channel DMA, DDR1/2 up to 200MHz 16/32-bit	Yes	27mm2, 388-pin EPGBA, RoHS-compliant	Yes	Two 1-Lane PCI Express v1.1, two 10/100/1G Ethernet, UART, SPI, External Bus Master, USB2.0 OTG	10 external, 8 internal, 32 GPIO		-40 to +85	802.11n WLAN AP and Gateway for Enterprise, SMB and high-end SOHO, WiMax Subscriber CPE, Control Plane	\$12 to \$19
	4-channel DMA, DDR1/2 up to 200MHz 16/32-bit	Yes	27mm2, 388-pin EPGBA, RoHS-compliant	Yes	Two 1-Lane PCI Express v1.1, two 10/100/1G Ethernet, UART, SPI, External Bus Master, USB2.0 OTG	10 external, 8 internal, 32 GPIO		-40 to +85	802.11n WLAN AP and Gateway for Enterprise, SMB and high-end SOHO, WiMax Subscriber CPE, Control Plane	\$10 to \$16.50
4-kbyte external	2-channel DMA, SRAM, SDRAM	Yes	316/413/456 PBGA	Yes	10/100 Ethernet, two UART, I ² C, GPIO, UIC, CodePack	7 external, 19 internal		-40 to +85	Single cycle access on-chip SRAM	\$12.00 to \$34.00
4-kbyte external	2-channel DMA, SRAM, SDRAM	Yes	456 PBGA, RoHS-compliant	Yes	10/100 Ethernet, two UART, I ² C, GPIO, UIC, CodePack	13 external, 19 internal		-40 to +85	Single cycle access on-chip SRAM	\$23.00 to \$39.25
	4-channel DMA, SRAM, SDRAM	Yes	456 PBGA, RoHS-compliant	Yes	Two 10/100 Ethernet, DMA, SPI, USB Host and device and PHYs, UIC, two I ² C, four UART, GPIO	10 external, 63 internal		-40 to +85		\$24.25 to \$56.50
16-kbyte external	4-channel DMA, DDRII SDRAM controller with ECC, NAND Flash	Yes	680 PBGA thermally enhanced, RoHS-compliant	Yes	Two 10/100/1000 Ethernet, SPI (SCP), four UART, two I ² C, 53 GPIO, USB2.0 host and device, PHY	10 external, programmable controller		-40 to +85	Optional Internet Security Core with TRNG, Turbo Security Engine	\$34.50 to \$68.00
8-kbyte external	4-channel DMA, DDR SRAM	Yes	552 CBGA	Yes	Two 10/100 Ethernet, two UART, two I ² C, GPIO, UIC, GPT	13 external, 63 internal		-40 to +85	PCI-X	\$42.00 to \$106.00

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AMCC www.amcc.com	PowerPC 440GR	PowerPC	333 to 667	32	32	1.5/2.5, 3.3	<4W		16x16 MAC		32-kbyte instruction/data
AMCC www.amcc.com	PowerPC 440GRx	PowerPC	400 to 667	32/64	32	1.5/2.5, 3.3	<4W		16x16 MAC		32-kbyte instruction/data
AMCC www.amcc.com	PowerPC 440GX	PowerPC	533 to 800	32/64	32	1.5/2.5, 3.3	<6W		16x16 MAC		32-kbyte instruction/data
AMCC www.amcc.com	PowerPC 440SP	PowerPC	533 to 667	32/64	32	1.5/2.5, 3.3	<6W (533MHz)		16x16 MAC		32-kbyte instruction/data
AMCC www.amcc.com	PowerPC 440SPe	PowerPC	533 to 800	32/64	32	1.5/2.5, 3.3	<7W (533MHz)		16x16 MAC		32-kbyte instruction/data
AMCC www.amcc.com	PowerPC 460EX	PowerPC	600 to 1200	32/64	32	1.25/1.8/2.5/3.3	<6W (1 GHz)			Yes	32-kbyte instruction/data
AMCC www.amcc.com	PowerPC 460GT	PowerPC	600 to 1200	32/64	32	1.2/1.8/2.5/3.3	<6W (1 GHz)			Yes	32-kbyte instruction/data
AMCC www.amcc.com	PowerPC 460GTx	PowerPC	800 to 1400	32/64	32	1.2/1.8/2.5/3.3	<8W (1GHz)		16 x16 MAC		32-kbyte instruction/data
AMCC www.amcc.com	PowerPC 460SX	PowerPC	800 to 1400	32/64	32	1.2/1.8/2.5/3.3	<10W (1GHz)		16 x16 MAC		32-kbyte instruction/data
AMCC www.amcc.com	PowerPC NPe405H	PowerPC	200 to 266	32	32	2.5/3.3	1.7 to 2.4W		16x16 MAC		16/8-kbyte instruction/data
AMD www.amd.com	AMD Mobile Sempron	x86	1600 to 2000	16/16	variable (x86)	1.1 to 1.35 (1.2 HT)	25 and 62W TDP	ACPI C1/C2/C3		Yes	64-kbyte instruction/data, L2: 256/128-kbyte
AMD www.amd.com	Geode GX 466@0.9W	x86	333	internal: 32	32	1.5	0.9W	ACPI 0W (S3)		Integrated	16-kbyte instruction/data
AMD www.amd.com	Geode GX 500@1.0W	x86	366	internal: 32	32	1.5	1W	ACPI 0W (S3)		Integrated	16-kbyte instruction/data
AMD www.amd.com	Geode GX 533@1.1W	x86	400	internal: 32	32	1.5	1.1W	ACPI 0W (S3)		Integrated	16-kbyte instruction/data
AMD www.amd.com	Geode LX 700@0.8W	x86	433	internal: 32	32	1.2	0.8W	ACPI 0W (S3)		Integrated	64/64-kbyte instruction/data, L2: 128-kbyte
AMD www.amd.com	Geode LX 800@0.9W	x86	500	internal: 32	32	1.2	0.9W	ACPI 0W (S3)		Integrated	64/64-kbyte instruction/data, L2: 128-kbyte
AMD www.amd.com	Geode NX 1250@6W	x86	667	internal: 32	32	1.1	6W	3W (Stop Grant)		Integrated	384-kbyte
AMD www.amd.com	Geode NX 1500@6W	x86	1000	internal: 32	32	1	6W	3W (Stop Grant)		Integrated	384-kbyte

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Four banks - each up to 256-Mbyte	4-channel DMA, DDR SDRAM controller with ECC, NAND Flash	Yes	456 PBGA, RoHS-compliant	Programmable	Two 10/100 Ethernet, MAL, up to four UARTs, two I ² C, SPI	10 external, 64 internal		-40 to +85		\$23.00 to \$51.00
16-kbyte external	4-channel DMA, DDRII SDRAM controller with ECC, NAND Flash	Yes	680 PBGA thermally enhanced PBGA, RoHS-compliant	Yes	Two 10/100/1000 Ethernet, packet reject inputs; four UART; two I ² C; 53 GPIO; SPI (SCP)	10 external, programmable controller		-40 to +85	Optional security accelerator or Turbo Security Engine with TRNG	\$34.50 to \$64.50
256-kbyte L2 or external	4-channel DMA, DDRII SDRAM controller with ECC, NAND Flash	Yes	552 CBGA	Yes	Two 10/100 Ethernet, two 10/100/1000 Ethernet, two I ² C, two UART, GPIO, GPT, UIC	18 external, 63 internal		-40 to +85 -40 to +105	PCI-X	\$71.00 to \$125.50
256-kbyte L2 or up to 4-Gbytes external	2-channel DMA, 32/64-bit, DDRII-667 SDRAM	Yes	783 FC-PBGA RoHS compliant	Yes	Three PCI-X (2 64-bit, 1 32-bit) 10/100/1000 Ethernet, three UART, two I ² C, GPIO, UIC, GPT, I20, XOR	18 external, 63 internal		-40 to +100	RAID 5, 6 acceleration	\$74 to \$89
256-kbyte L2 or up to 16-Gbytes external	2-channel DMA, 32/64-bit, DDRII-667 SDRAM	Yes	675 FC-PBGA RoHS compliant	Yes	Three PCI Express ("x8" plus 2 "x4"), 64-bit PCI-X, 10/100/1000 Ethernet, three UART, two I ² C, GPIO, UIC, GPT, I20, XOR	16 external, 101 internal		0 to +95	RAID 5, 6 acceleration	\$80 to \$120
256-kbyte L2 or external	4-channel DMA	Yes	728 TE-EPBGA RoHS-compliant		2x PCI Express, -one "x4"lane and one "x1" lane; 1 SATA II port; 10/100/1G Ethernet,	16 external, 48 internal		-40 to +85	USB 2.0 OTG; SATA (up to 3.0Gb/s); Ipsec/SSL acceleration; Turbo security; QOS and TCP/IP Acceleration hardware, RAID 5 Acceleration	\$47 to \$92
256-kbyte L2 or external	4-channel DMA	Yes	728 TE-PBGA RoHS-compliant		PCI Express, -one "x4"lane and one "x1" lane; 2.5Gbit/s fdx per lane - 4 ports 10/100/1G Ethernet, UARTS, NAND Cntl, I ² C, GPIO, UIC, GPT	16 external, 48 internal		-40 to +85	SRIO support; Turbo security; QOS and TCP/IP Acceleration hardware	\$49 to \$96
512-kbyte L2, 32-kbyte on-chip SRAM, up to 16-Gbyte external	3-channel DMA, 32/64bit, DDRII-800 SDRAM	Yes	783 FC-PBGA RoHS-compliant	Yes	Two Gen 2 PCI Express (2 "x4" or 1 "x8") , 4x 10/100/1G Ethernet, UARTS, NAND Cntl, I ² C, GPIO, UIC, GPT	16 external, 101 internal		0 to +95	Network Turbo security	\$75 to \$106
512-kbyte L2, 32-kbyte on-chip SRAM or up to 16-Gbyte external	3-channel DMA, 32/64bit, DDRII-800 SDRAM	Yes	783 FC-PBGA RoHS-compliant	Yes	Three Gen 2 PCI Express (one "x8" and 2 "x4") , 4x 10/100/1G Ethernet, UARTS, NAND Cntl, I ² C, GPIO, UIC, GPT, XOR	16 external, 101 internal		0 to +95	RAID 5, 6 acceleration, I20, XTS-AES Storage security Engine - Network Turbo security - On-Chip memory (32KB)	\$94 to \$140
4-kbyte external	4-channel DMA, SDRAM, DMA	Yes	324 PBGA, 580 PBGA	Yes	Four 10/100 Ethernet, I ² C, two UART, GPIO, UIC, 32-channel HDLC, eight-port HDLC	7 external, 19 internal		-40 to +85		\$28.75 to \$61.50
DDR400/333/266/200	Integrated		754 uPGA, lidless		Hyper-Transport			0 to +95	NX bit, SSE3	\$107 to \$142
See cache	DDR SDRAM	256 entry TLB								\$26.50
See cache	DDR SDRAM	256 entry TLB								\$29.15
See cache	DDR SDRAM	256 entry TLB								\$32.75
	DDR									
	DDR									
See cache	SDRAM	256 entry TLB	453 Socket A OPGA					-40 to +95		\$65
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AMD www.amd.com	Geode NX 1750@14W	x86	1400	internal: 32	32	1.25	14W	3W (Stop Grant)		Integrated	384-kbyte
Analog Devices www.analog.com	AD1940 AD1941	SigmaDSP	75		40	2.5/3.3/5	239 mW		56-bit fixed point		
Analog Devices www.analog.com	AD1953	SigmaDSP	25		35	5	540 mW	230 mW	48-bit fixed point		
Analog Devices www.analog.com	ADAU1401	SigmaDSP	50		40	1.8/3.3	287 mW		56-bit fixed point		
Analog Devices www.analog.com	ADAU1701	SigmaDSP	50		40	1.8/3.3	287 mW		56-bit fixed point		
Analog Devices www.analog.com	ADAU1702	SigmaDSP	25		40	1.8/3.3	287 mW		56-bit fixed point		
Analog Devices www.analog.com	ADSP-21261	SHARC	150	16: muxed	48	1.2/3.3			32-bit fixed point / 32 and 40-bit floating point	32-bit	
Analog Devices www.analog.com	ADSP-21262	SHARC	200	16: muxed	48	1.2/3.3			32-bit fixed point / 32 and 40-bit floating point	32-bit	
Analog Devices www.analog.com	ADSP-21266	SHARC	150, 200	16: muxed	48	1.2/3.3			32-bit fixed point / 32 and 40-bit floating point	32-bit	
Analog Devices www.analog.com	ADSP-21362	SHARC	200, 333	16: muxed	48	1.2/3.3			32-bit fixed point / 32 and 40-bit floating point	32-bit	
Analog Devices www.analog.com	ADSP-21363	SHARC	200, 333	16: muxed	48	1.2/3.3			32-bit fixed point / 32 and 40-bit floating point	32-bit	
Analog Devices www.analog.com	ADSP-21364	SHARC	333	16: muxed	48	1.2/3.3			32-bit fixed point / 32 and 40-bit floating point	32-bit	
Analog Devices www.analog.com	ADSP-21365	SHARC	333	16: muxed	48	1.2/3.3			32-bit fixed point / 32 and 40-bit floating point	32-bit	

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See cache	SDRAM	256 entry TLB	453 Socket A OPGA					-40 to +95		\$55
7.5-kbyte program, 4-kbyte parameter, 6 kwords data			7x7-mm 48-lead LQFP		16-channel I2S or TDM, SPI (AD1940), I2C (AD1941)			-40 to +105	on-board 1.8 V regulator	\$5.96
2.5-kbyte program, 0.75-kbyte parameter			7x7-mm 48-lead LQFP		I2S, TDM, SPI		3-channel 24-bit audio DAC, 112 dB SNR	-40 to +105		\$5.88
5-kbyte program, 4 kbyte parameter, 2 kwords data			7x7-mm 48-lead LQFP		8-channel I2S/TDM I/O, SPI, I2C		audio ADC: 2-channel 24-bit, 100 dB audio DAC: 4-channel 24-bit, 104 dB control ADC: 4-channel 8-bit	-40 to +105	on-board 1.8 V regulator, PLL, 12 GPIOs	\$4.73
5-kbyte program, 4 kbyte parameter, 2 kwords data			7x7-mm 48-lead LQFP		8-channel I2S/TDM I/O, SPI, I2C		audio ADC: 2-channel 24-bit, 100 dB audio DAC: 4-channel 24-bit, 104 dB control ADC: 4-channel 8-bit	0 to +70	on-board 1.8 V regulator, PLL, 12 GPIOs	\$3.72
2.5-kbyte program, 4-kbyte parameter, 0.5 kwords data			7x7-mm 48-lead LQFP		8-channel I2S/TDM I/O, SPI, I2C		audio ADC: 2-channel 24-bit, 100 dB audio DAC: 4-channel 24-bit, 104 dB control ADC: 4-channel 8-bit	0 to +70	on-board 1.8 V regulator, PLL, 12 GPIOs	\$2.93
1-Mbit SRAM, 3-Mbit ROM	18 zero-overhead DMA channel		136 BGA, 144 LQFP	3 timers with PWM output and capture, two precision clock generators	SPI, Signal Routing Unit, four TDM serial ports, input data port, 18-channel DMA	10, four dedicated flags/IRQs, six flag inputs and outputs		0 to +70, -40 to +85	Up to 16 simultaneous I2S channels	\$5.25
2-Mbit SRAM, 4-Mbit ROM	22 zero-overhead DMA channel		136 BGA, 144 LQFP	3 timers with PWM output and capture, two precision clock generators	SPI, Signal Routing Unit, six TDM serial ports, input data port, 22-channel DMA	10, four dedicated flags/IRQs, six flag inputs and outputs		0 to +70, -40 to +85	Up to 24 simultaneous I2S channels	\$14.91
2-Mbit SRAM, 4-Mbit ROM	22 zero-overhead DMA channel		136 BGA, 144 LQFP	3 timers with PWM output and capture, two precision clock generators	SPI, Signal Routing Unit, six TDM serial ports, input data port, 22-channel DMA	10, four dedicated flags/IRQs, six flag inputs and outputs		0 to +70, -40 to +85	Up to 24 simultaneous I2S channels, Audio decoders in ROM need license	\$12.53 to \$14.91
3-Mbit SRAM, 4-Mbit ROM	25 zero-overhead DMA channel		136 BGA, 144 LQFP E-PAD	3 timers with PWM output and capture, 16 PWM output channels, two precision clock generators	Signal Routing Unit, S/PDIF receive/transmit, SPI, six TDM serial ports, input data port, 25-channel DMA	10, six flag inputs and outputs		0 to +70, -40 to +85, -40 to +105 (200MHz QFP only)	Up to 24 simultaneous I2S channels, 8-channel asynchronous sample rate converter	\$19.90 to \$28.67
3-Mbit SRAM, 4-Mbit ROM	25 zero-overhead DMA channel		136 BGA, 144 LQFP E-PAD	3 timers with PWM output and capture, 16 PWM output channels, two precision clock generators	Signal Routing Unit with six TDM serial ports, SPI, input data port, 25-channel DMA	10, six flag inputs and outputs		0 to +70, -40 to +85, -40 to +105 (200MHz QFP only)	Up to 24 simultaneous I2S channels	\$17.80 to \$25.64
3-Mbit SRAM, 4-Mbit ROM	25 zero-overhead DMA channel		136 BGA, 144 LQFP E-PAD	3 timers with PWM output and capture, 16 PWM output channels, two precision clock generators	Signal Routing Unit, S/PDIF receive/transmit, SPI, six TDM serial ports, input data port, 25-channel DMA	10, six flag inputs and outputs		0 to +70, -40 to +85, -40 to +105 (200MHz QFP only)	Up to 24 simultaneous I2S channels, 8-channel asynchronous sample rate converter	\$26.20 to \$37.74
3-Mbit SRAM, 4-Mbit ROM	25 zero-overhead DMA channel		136 BGA, 144 LQFP E-PAD	3 timers with PWM output and capture, 16 PWM output channels, two precision clock generators	Signal Routing Unit, S/PDIF receive/transmit, SPI, six TDM serial ports, input data port, 25-channel DMA	10, six flag inputs and outputs		0 to +70, -40 to +85, -40 to +105 (200MHz QFP only)	Up to 24 simultaneous I2S channels, Audio decoders in ROM need license from IP holders, 8-channel asynchronous sample rate converter, DTCP	\$20.95 to \$30.18

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Analog Devices www.analog.com	ADSP-21366	SHARC	333	16: muxed	48	1.2/3.3			32-bit fixed point / 32 and 40-bit floating point	32-bit	
Analog Devices www.analog.com	ADSP-21367	SHARC	266, 333, 400	32: SDRAM	48	1.2 (1.3)/3.3			32-bit fixed point / 32 and 40-bit floating point	32-bit	
Analog Devices www.analog.com	ADSP-21368	SHARC	333, 400	32: SDRAM	48	1.2 (1.3)/3.3			32-bit fixed point / 32 and 40-bit floating point	32-bit	
Analog Devices www.analog.com	ADSP-21369	SHARC	266, 333, 400	32: SDRAM	48	1.2 (1.3)/3.3			32-bit fixed point / 32 and 40-bit floating point	32-bit	
Analog Devices www.analog.com	ADSP-21371	SHARC	266	32: SDRAM	48	1.2/3/3			32-bit fixed point / 32 and 40-bit floating point	32-bit	
Analog Devices www.analog.com	ADSP-21375	SHARC	266	16: SDRAM	48	1.2/3/3			32-bit fixed point / 32 and 40-bit floating point	32-bit	
Analog Devices www.analog.com	ADSP-BF522 ADSP-BF524 ADSP-BF526	Blackfin	300,400	20/16 Async/Sync	16, 32, 64	0.8 to 1.4/ 1.8 to 3.3		Full-On, active, sleep, deep sleep, hibernate (50 uA)	Dual 16-bit MACs dual 40-bit ALUs 40-bit shifter dual data address generators quad 8-bit video ALUs	16-bit Fixed Point / 32-bit Floating Point	Up to 16/32-kbyte instruction/data
Analog Devices www.analog.com	ADSP-BF522C ADSP-BF524C ADSP-BF526C	Blackfin	300,400	20/16 Async/Sync	16, 32, 64	0.8 to 1.4/ 1.8 to 3.3		Full-On, active, sleep, deep sleep, hibernate (50 uA)	Dual 16-bit MACs dual 40-bit ALUs 40-bit shifter dual data address generators quad 8-bit video ALUs	16-bit Fixed Point / 32-bit Floating Point	Up to 16/32-kbyte instruction/data
Analog Devices www.analog.com	ADSP-BF523 ADSP-BF525 ADSP-BF527	Blackfin	300,600	20/16 Async/Sync	16, 32, 64	0.8 to 1.4/ 1.8 to 3.3		Full-On, active, sleep, deep sleep, hibernate (50 uA)	Dual 16-bit MACs dual 40-bit ALUs 40-bit shifter dual data address generators quad 8-bit video ALUs	16-bit Fixed Point / 32-bit Floating Point	Up to 16/32-kbyte instruction/data
Analog Devices www.analog.com	ADSP-BF523C ADSP-BF525C ADSP-BF527C	Blackfin	300,600	20/16 Async/Sync	16, 32, 64	0.8 to 1.4/ 1.8 to 3.3		Full-On, active, sleep, deep sleep, hibernate (50 uA)	Dual 16-bit MACs dual 40-bit ALUs 40-bit shifter dual data address generators quad 8-bit video ALUs	16-bit Fixed Point / 32-bit Floating Point	Up to 16/32-kbyte instruction/data
Analog Devices www.analog.com	ADSP-BF531 ADSP-BF532 ADSP-BF533	Blackfin	400, 600	20/16 Async/Sync	16, 32, 64	0.8 to 1.4/ 2.25 to 3.6	264 mW (600 MHz)	Full-On, active, sleep, deep sleep, hibernate (50 uA)	Dual 16-bit MACs dual 40-bit ALUs 40-bit shifter dual data address generators quad 8-bit video ALUs	16-bit Fixed Point / 32-bit Floating Point	Up to 16/32-kbyte instruction/data
Analog Devices www.analog.com	ADSP-BF534	Blackfin	400 to 500	20/16 Async/Sync	16, 32, 64	0.8 to 1.2/ 2.25 to 3.6	250 mW	Full-On, active, sleep, deep sleep, hibernate (50 uA)	Dual 16-bit MACs dual 40-bit ALUs 40-bit shifter dual data address generators quad 8-bit video ALUs	16-bit Fixed Point / 32-bit Floating Point	Up to 16/32-kbyte instruction/data

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
3-Mbit SRAM, 4-Mbit ROM	25 zero-overhead DMA channel		136 BGA, 144 LQFP E-PAD	3 timers with PWM output and capture, 16 PWM output channels, two precision clock generators	Signal Routing Unit, S/PDIF receive/transmit, SPI, six TDM serial ports, input data port, 25-channel DMA	10, six flag inputs and outputs		0 to +70, -40 to +85, -40 to +105 (200MHz QFP only)	Up to 24 simultaneous I2S channels, Audio decoders in ROM, need license from IP holders, 8-channel asynchronous sample rate converter	\$19.90 to \$28.67
2-Mbit SRAM, 6-Mbit ROM, SDRAM controller	34 zero-overhead DMA channel		256 SBGA, 208 MQFP	3 timers with PWM output and capture plus 16 PWM output channels, four precision clock generators	Eight TDM serial ports, S/PDIF transmit/receive, two UARTS, up to 34 GPIO, two SPI, one TWI, input data port, signal routing unit	10		0 to +70, -40 to +85	Up to 32 simultaneous I2S channels, Audio decoders in ROM need license from IP holders, asynchronous sample rate converter	\$18.32 to \$30.71
2-Mbit SRAM, 6-Mbit ROM, SDRAM controller	34 zero-overhead DMA channel		256 SBGA	3 timers with PWM output and capture plus 16 PWM output channels, four precision clock generators	Eight TDM serial ports, S/PDIF transmit/receive, two UARTS, up to 34 GPIO, two SPI, one TWI, input data port, signal routing unit	10		0 to +70, -40 to +85	Up to 32 simultaneous I2S channels, shared-memory to arbitrate the bus and gluelessly access a common memory device, asynchronous sample rate converter	\$27.52 to \$36.70
2-Mbit SRAM, 6-Mbit ROM, SDRAM controller	34 zero-overhead DMA channel		256 SBGA, 208 MQFP	3 timers with PWM output and capture plus 16 PWM output channels, four precision clock generators	Eight TDM serial ports, S/PDIF transmit/receive, two UARTS, up to 34 GPIO, two SPI, one TWI, input data port, signal routing unit	10		0 to +70, -40 to +85	Up to 32 simultaneous I2S channels, asynchronous sample rate converter.	\$17.50 to \$20.13
1-Mbit SRAM, 4-Mbit ROM, SDRAM controller	24 zero-overhead DMA channel		208 MQFP	2 timers, four precision clock generators	Four TDM serial ports, UART, one TWI, input data port, signal routing unit	3		0 to +70	Up to 16 simultaneous I2S channels, supports execution from external SDRAM	\$11.27
0.5-Mbit SRAM, 2-Mbit ROM, SDRAM controller	24 zero-overhead DMA channel		208 MQFP	2 timers, four precision clock generators	Four TDM serial ports, UART, one TWI, input data port, signal routing unit	3		0 to +70	Up to 16 simultaneous I2S channels, supports execution from external SDRAM	\$7.95
64-kbyte instruction SRAM, 64-kbyte data SRAM, 4-kbyte scratchpad RAM	SRAM, SDRAM, Flash, EPROM	Yes	208 Mini-BGA, 289 Mini-PBGA	Eight 32-bit with PWM, 32-bit core, 32-bit up/down, real-time, watchdog	Parallel peripheral interface for ITU-R 656; two SPORT, two UART, SPI, 48 GPIO, HS USB OTG(524,526), 10/100 Ethernet MAC(526)	54 independent interrupt ports		-40 to +85 0 to +70	Voltage regulator, PLL, JTAG, NAND flash controller, LockBox Security	
64-kbyte instruction SRAM, 64-kbyte data SRAM, 4-kbyte scratchpad RAM	SRAM, SDRAM, Flash, EPROM	Yes	208 Mini-BGA, 289 Mini-PBGA	Eight 32-bit with PWM, 32-bit core, 32-bit up/down, real-time, watchdog	Parallel peripheral interface for ITU-R 656; two SPORT, two UART, SPI, 48 GPIO, HS USB OTG(524C,526C), 10/100 Ethernet MAC(526C)	54 independent interrupt ports		-40 to +85 0 to +70	Voltage regulator, PLL, JTAG, embedded stereo audio codec, NAND Flash Controller, LockBox Security	
64-kbyte instruction SRAM, 64-kbyte data SRAM, 4-kbyte scratchpad RAM	SRAM, SDRAM, Flash, EPROM	Yes	208 Mini-BGA, 289 Mini-PBGA	Eight 32-bit with PWM, 32-bit core, 32-bit up/down, real-time, watchdog	Parallel peripheral interface for ITU-R 656; two SPORT, two UART, SPI, 48 GPIO, HS USB OTG(525,527), 10/100 Ethernet MAC(527)	54 independent interrupt ports		-40 to +85 0 to +70	Voltage regulator, PLL, JTAG, NAND flash controller, LockBox Security	
64-kbyte instruction SRAM, 64-kbyte data SRAM, 4-kbyte scratchpad RAM	SRAM, SDRAM, Flash, EPROM	Yes	208 Mini-BGA, 289 Mini-PBGA	Eight 32-bit with PWM, 32-bit core, 32-bit up/down, real-time, watchdog	Parallel peripheral interface for ITU-R 656; two SPORT, two UART, SPI, 48 GPIO, HS USB OTG(525C,527C), 10/100 Ethernet MAC(527C)	54 independent interrupt ports		-40 to +85 0 to +70	Voltage regulator, PLL, JTAG, embedded stereo audio codec, NAND Flash Controller, LockBox Security	
Up to 80-kbyte instruction SRAM, up to 64-kbyte data SRAM, 4-kbyte scratchpad RAM	SRAM, SDRAM, Flash, EPROM	Yes	160 Mini-BGA, 169-PBGA, 176 LQFP	Three 32-bit with PWM, 32-bit core, real-time, watchdog	Parallel peripheral interface for ITU-R 656; two SPORT, UART, SPI, 16 GPIO	External controller		-40 to +85 0 to +70	Voltage regulator, PLL, JTAG	\$5.45 to \$14.95
64-kbyte instruction SRAM, 64-kbyte data SRAM, 4-kbyte scratchpad RAM	SRAM, SDRAM, Flash, EPROM, DMA, two external DMA	Yes	182 Mini-BGA, 208 Sparse MiniBGA	Three 32-bit with PWM, 32-bit core, real-time, watchdog	Parallel peripheral interface for ITU-R 656; CAN, TWI, two SPORT, two UART, SPI, 48 GPIO	External controller		-40 to +85 -40 to +105	Voltage regulator, two external DMA request lines, PLL, JTAG	\$9.65 to \$13.10

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Analog Devices www.analog.com	ADSP-BF535	Blackfin	200 to 350	26/32 Async/Sync	16, 32, 64	1.0 to 1.6/ 3.15 to 3.45	797 mW	Full-On, active, sleep, deep sleep	Dual 16-bit MACs dual 40-bit ALUs 40-bit shifter dual data address generators quad 8-bit video ALUs	16-bit Fixed Point / 32-bit Floating Point	Up to 16/32-kbyte instruction/data
Analog Devices www.analog.com	ADSP-BF536 ADSP-BF537	Blackfin	300 to 600	20/16 Async/Sync	16, 32, 64	0.8 to 1.2/ 2.25 to 3.6	250 mW	Full-On, active, sleep, deep sleep, hibernate (50 uA)	Dual 16-bit MACs dual 40-bit ALUs 40-bit shifter dual data address generators quad 8-bit video ALUs	16-bit Fixed Point / 32-bit Floating Point	Up to 16/32-kbyte instruction/data
Analog Devices www.analog.com	ADSP-BF538 ADSP-BF538F	Blackfin	400 to 500	20/16 Async/Sync	16, 32, 64	0.8 to 1.2	250 mW	Full-On, active, sleep, deep sleep, hibernate	Dual 16-bit MACs dual 40-bit ALUs 40-bit shifter dual data address generators quad 8-bit video ALUs	16-bit Fixed Point / 32-bit Floating Point	Up to 16/32-kbyte instruction/data
Analog Devices www.analog.com	ADSP-BF539 ADSP-BF539F	Blackfin	400 to 500	20/16 Async/Sync	16, 32, 64	1.0 to 1.2	250 mW	Full-On, active, sleep, deep sleep, hibernate	Dual 16-bit MACs dual 40-bit ALUs 40-bit shifter dual data address generators quad 8-bit video ALUs	16-bit Fixed Point / 32-bit Floating Point	Up to 16/32-kbyte instruction/data
Analog Devices www.analog.com	ADSP-BF542 ADSP-BF544 ADSP-BF547 ADSP-BF548 ADSP-BF549	Blackfin	400, 533, 600	20/16 Async/Sync	16, 32, 64	0.9 to tbd/ 1.8 to 3.3		Full-On, active, sleep, deep sleep, hibernate (50 uA)	Dual 16-bit MACs dual 40-bit ALUs 40-bit shifter dual data address generators quad 8-bit video ALUs	16-bit Fixed Point / 32-bit Floating Point	Up to 16/32-kbyte instruction/data
Analog Devices www.analog.com	ADSP-BF561	Blackfin	500, 600 dual core	26/32 Async/Sync	16, 32, 64	0.8 to 1.2/ 2.25 to 3.6	650 mW (600 MHz)	Full-On, active, sleep, deep sleep, hibernate (50 uA)	Dual 16-bit MACs dual 40-bit ALUs 40-bit shifter dual data address generators quad 8-bit video ALUs	16-bit Fixed Point / 32-bit Floating Point	Up to 16/32-kbyte instruction/data (per core)
Analog Devices www.analog.com	ADuC7020	ARM7TDMI	40	16	16, 32	2.7 to 3.6	150 mW	90 µW	Multiply instruction		
Analog Devices www.analog.com	ADuC7021	ARM7TDMI	40	16	16, 32	2.7 to 3.6	150 mW	90 µW	Multiply instruction		
Analog Devices www.analog.com	ADuC7022	ARM7TDMI	40	16	16, 32	2.7 to 3.6	150 mW	90 µW	Multiply instruction		
Analog Devices www.analog.com	ADuC7024	ARM7TDMI	40	16	16, 32	2.7 to 3.6	150 mW	90 µW	Multiply instruction		
Analog Devices www.analog.com	ADuC7025	ARM7TDMI	40	16	16, 32	2.7 to 3.6	150 mW	90 µW	Multiply instruction		
Analog Devices www.analog.com	ADuC7026	ARM7TDMI	40	16	16, 32	2.7 to 3.6	150 mW	90 µW	Multiply instruction		
Analog Devices www.analog.com	ADuC7027	ARM7TDMI	40	16	16, 32	2.7 to 3.6	150 mW	90 µW	Multiply instruction		

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
16-kbyte instruction SRAM, 32-kbyte data SRAM, 4-kbyte scratchpad RAM, 256-kbyte L2 SRAM	SRAM, SDRAM, Flash, EPROM, DMA	Yes	260 PBGA	Three 32-bit with PWM, 32-bit core, real-time, watchdog	PCI, USB Device, two SPORT, UART, SPI	External controller		-40 to +85 0 to +70	JTAG	\$22.00 to \$31.25
64-kbyte instruction SRAM, up to 64-kbyte data SRAM, 4-kbyte scratchpad RAM	SRAM, SDRAM, Flash, EPROM, DMA, two external DMA	Yes	182 Mini-BGA, 208 Sparse Mini-BGA	Eight 32-bit with PWM, 32-bit core, real-time, watchdog	10/100 Ethernet, Parallel peripheral interface for ITU-R 656; CAN 2.0 Controller, TWI, two SPORT, two UART, SPI, 48 GPIO	External controller		-40 to +85 0 to +70	Voltage regulator, request lines, PLL, JTAG	\$8.05 to \$16.55
80-kbyte instruction SRAM, 64-kbyte data SRAM, 4-kbyte scratchpad RAM, 512-kbyte or 1-Mbyte of Flash	SRAM, SDRAM, Flash, EPROM, DMA, two external DMA	Yes	316-ball mBGA, Pb-Free	Four 32-bit, watchdog	PPI, 4 Serial Ports, 2 DMA, 3 UARTS, 2 TWI, up to 54 GPIO	External controller		-40 to +85	Voltage regulator, CAN2.0B Controller, PLL, JTAG	\$13.54 to \$17.45
80-kbyte instruction SRAM, 64-kbyte data SRAM, 4-kbyte scratchpad RAM, 512-kbyte or 1-Mbyte of Flash	SRAM, SDRAM, Flash, EPROM, DMA, two external DMA	Yes	316-ball mBGA, Pb-Free	Four 32-bit General Purpose programmable timers w/ 1 watchdog Timer	Up to 80-kbyte instruction SRAM, 64-kbyte data SRAM, 4-kbyte scratchpad RAM, 512 Kbyte or 1 MB of Flash Memory(BF538F only)	External controller		-40 to +105	MXVR Media Transceiver, Voltage regulator, CAN2.0B Controller, PLL, JTAG	
64-kbyte instruction SRAM, 64-kbyte data SRAM, 4-kbyte scratchpad RAM, up to 128-kbyte L2 SRAM	SRAM, SDRAM, Flash, EPROM	Yes	400 Mini-BGA	Eight 32-bit with PWM, 32-bit core, 32-bit up/down, real-time, watchdog	Enhanced PPIs, ATAPI controller, CAN 2.0, 4 Serial Ports, 3 SPI, 3 UART, TWI, HS USB OTG, Pixel Compositor, Rotary Encoder, Keypad Controller	54 independent interrupt ports		-40 to +85 0 to +70	Voltage regulator, PLL, JTAG, Lock Box Security, MXVR Media Transceiver (BF549 only)	
(32-kbyte instruction SRAM, 64-kbyte data SRAM, 4-kbyte scratchpad RAM) per core, 128-kbyte L2 SRAM	SRAM, SDRAM, Flash, EPROM, three DMA controllers	Yes	Two 256 Mini-BGA packages, 297-PBGA	12 32-bit with PWM, two 32-bit core, two watchdog	Two parallel peripheral interface supporting ITU-R 656; two SPORT, UART, SPI, 48 GPIO	External controller		-40 to +85 0 to +70	Voltage regulator, PLL, JTAG	
62-kbyte Flash/EE, 8-kbyte SRAM	In-circuit download		40 LFCSP, 6x6 mm	Four 32-bit	SPI, two I ² C, UART, JTAG	24	Five-channel, 12-bit, 1-MSPS; four 12-bit voltage output DACs	-40 to +125	16-element PLA, voltage comparator, temperature sensor, JTAG based debug	\$7.62
62-kbyte Flash/EE, 8-kbyte SRAM	In-circuit download		40 LFCSP, 6x6 mm	Four 32-bit	SPI, two I ² C, UART, JTAG	24	Eight-channel, 12-bit, 1-MSPS; two 12-bit voltage output DACs	-40 to +125	16-element PLA, voltage comparator, temperature sensor, JTAG based debug	\$4.36 to \$6.39
62-kbyte Flash/EE, 8-kbyte SRAM	In-circuit download		40 LFCSP, 6x6 mm	Four 32-bit	SPI, two I ² C, UART, JTAG	24	10-channel, 12-bit, 1-MSPS	-40 to +125	16-element PLA, voltage comparator, temperature sensor, JTAG based debug	\$3.75 to \$5.34
62-kbyte Flash/EE, 8-kbyte SRAM	In-circuit download		64 LFCSP, 9x9 mm; 64 LQFP	Four 32-bit, three-phase PWM	SPI, two I ² C, UART, JTAG	24	10 channel, 12-bit, 1-MSPS; two 12-bit voltage output DACs	-40 to +125	16-element PLA, voltage comparator, temperature sensor, JTAG based debug	\$7.62
62-kbyte Flash/EE, 8-kbyte SRAM	In-circuit download		64 LFCSP, 9x9 mm	Four 32-bit, three-phase PWM	SPI, two I ² C, UART, JTAG	24	12-channel, 12-bit, 1-MSPS	-40 to +125	16-element PLA, voltage comparator, temperature sensor, JTAG based debug	\$5.45 to \$6.50
62-kbyte Flash/EE, 8-kbyte SRAM	In-circuit download		80 LQFP	Four 32-bit, three-phase PWM	SPI, two I ² C, UART, JTAG	24	12-channel, 12-bit, 1-MSPS; four voltage-output 12 bit DACs	-40 to +85	16-element PLA, voltage comparator, temperature sensor, JTAG based debug	\$10.60
62-kbyte Flash/EE, 8-kbyte SRAM	In-circuit download		80 LQFP	Four 32-bit, three-phase PWM	SPI, two I ² C, UART, JTAG	24	16-channel, 12-bit, 1-MSPS	-40 to +85	16-element PLA, voltage comparator, temperature sensor, JTAG based debug	\$5.85 to \$6.90

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Analog Devices www.analog.com	ADuC7060	ARM7TDMI	10.24	16	16, 32	2.375 to 2.625	25mW	90 µW	Multiply instruction		
Analog Devices www.analog.com	ADuC7061	ARM7TDMI	10.24	16	16, 32	2.375 to 2.625	25mW	90 µW	Multiply instruction		
Analog Devices www.analog.com	ADuC7062	ARM7TDMI	10.24	16	16, 32	2.375 to 2.625	25mW	90 µW	Multiply instruction		
Analog Devices www.analog.com	ADuC7128	ARM7TDMI	41.78	16	16, 32	3.0 to 3.6	150 mW	90 µW	Multiply instruction		
Analog Devices www.analog.com	ADuC7129	ARM7TDMI	41.78	16	16, 32	3.0 to 3.6	150 mW	90 µW	Multiply instruction		
Analog Devices www.analog.com	ADuC848	8051	98 kHz to 12.58	external: 24/8 data	8	3/5	2.3 mA (3.6V)	33 to 39 mW			
ARC International www.arc.com	ARC 605	ARCompact	200 to 400 worst case (130nm)	32	16, 32	1 to 5	0.06 mW/MHz (0.13)	Sleep mode, clock gating, RAM controls			
ARC International www.arc.com	ARC 610D	ARCompact	200 to 400 worst case (130nm)	32	16, 32	1 to 5	0.07 mW/MHz (0.13)	Sleep mode, clock gating, RAM controls	16/32 MUL/MAC DSP extensions Optional ARC XY subsystem	Optional FPX extensions, single and/or double precision	
ARC International www.arc.com	ARC 625D	ARCompact	200 to 400 worst case (130nm)	32	16, 32	1 to 5	0.08 mW/MHz (0.13)	Sleep mode, clock gating, RAM controls	16/32 MUL/MAC DSP extensions Optional ARC XY subsystem	Optional FPX extensions, single and/or double precision	2- to 32-kbyte instruction/data (configurable)
ARC International www.arc.com	ARC 710D	ARCompact	Up to 700 worst case (90nm)	32	16, 32	1 to 5	0.16 mW/MHz (0.13)	Sleep mode, RAM controls	16/32 MUL/MAC DSP extensions Optional ARC XY subsystem	Optional FPX extensions, single and/or double precision	
ARC International www.arc.com	ARC 725D	ARCompact	Up to 700 worst case (90nm)	32	16, 32	1 to 5	0.16 mW/MHz (0.13)	Sleep mode, RAM controls	16/32 MUL/MAC DSP extensions Optional ARC XY subsystem	Optional FPX extensions, single and/or double precision	8- to 64-kbyte instruction/data (configurable)
ARC International www.arc.com	ARC 750D	ARCompact	Up to 700 worst case (90nm)	32	16, 32	1 to 5	0.16 mW/MHz (0.13)	Sleep mode, RAM controls	16/32 MUL/MAC DSP extensions Optional ARC XY subsystem	Optional FPX extensions, single and/or double precision	8- to 64-kbyte instruction/data (configurable)
ARC International www.arc.com	ARC Media Subsystem	ARCompact	Up to 700 worst case (90nm)	32	16, 32	1 to 5	0.24 mW/MHz	Domain clock gating, Voltage domains, Dynamic voltage and frequency scaling, power management unit	16/32 MUL/MAC DSP extensions Optional ARC XY subsystem	Optional FPX extensions, single and/or double precision	8- to 64-kbyte instruction/data (configurable)
ARC International www.arc.com	ARC Sound Subsystem Family	ARCompact	Up to 700 worst case (90nm)	32	16, 32	1 to 5	0.24 mW/MHz	Domain clock gating, Voltage domains, Dynamic voltage and frequency scaling, power management unit	16/32 MUL/MAC DSP extensions Optional ARC XY subsystem	Optional FPX extensions, single and/or double precision	8- to 64-kbyte instruction/data (configurable)

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
30-kbyte Flash/EE, 4-kbyte SRAM			32 LFCSP 5*5mm, 48-LFCSP, 48-LQFP	Four timers, 6-channel 16-bit PWM	SPI/ I ² C, UART, JTAG	16 sources	Dual 24-bit ADCs - 8KSPS, 12-Bit DAC	-40 to +125	Vectored Interrupt controller supporting IRQ nesting and priority control	\$4.90
30-kbyte Flash/EE, 4-kbyte SRAM			32 LFCSP 5*5mm, 48-LFCSP, 48-LQFP	Four timers, 6-channel 16-bit PWM	SPI/ I ² C, UART, JTAG	16 sources	Dual 24-bit ADCs - 8KSPS, 12-Bit DAC	-40 to +125	Vectored Interrupt controller supporting IRQ nesting and priority control	\$3.90
30-kbyte Flash/EE, 4-kbyte SRAM			32 LFCSP 5*5mm, 48-LFCSP, 48-LQFP	Four timers, 6-channel 16-bit PWM	SPI/I ² C, UART, JTAG	16 sources	Dual 24-bit ADCs - 8KSPS, 12-Bit DAC	-40 to +125	Vectored Interrupt controller supporting IRQ nesting and priority control	\$3.40
126-kbyte Flash/EE, 8-kbyte SRAM	In-circuit download		64-LFCSP, 9x9mm 64 LQFP	Five 32-bit, 6-channel PWM with H-mode bridge	SPI, two I ² C, two UART, JTAG	24	10-channel, 12-bit, 1-MSPS	-40 to +125	On-chip quadrature encoder, integrated DDS with low-pass filter	\$6.95
126-kbyte Flash/EE, 8-kbyte SRAM	In-circuit download		80 lead LQFP	Five 32-bit	SPI, two I ² C, two UART, JTAG, 6-channel DMA with H-mode bridge	24	16-channel, 12-bit, 1-MSPS	-40 to +125	On-chip quadrature encoder, integrated DDS with low-pass filter	\$6.95
62-kbyte Flash/EE, 4-kbyte Flash/EE, 2-kbyte + 256-byte SRAM			8x8-mm CSP, 52 MQFP	Three 16-bit, wake-up, real-time, single and dual PWM	UART, SPI, I ² C	11	10-channel 16-bit, sigma-delta with PGA; 12-bit DAC	-40 to +125	Single-cycle 8052 core, PLL	\$4.65 to \$6.85
Configurable 1- to 512-kbyte instruction, 2- to 16-kbyte data	Licensee option		IP core	Licensee option	Licensee option	Up to 32	Licensee option	(Core)	BVCI, AMBA bridge, JTAG to Ethernet debug, Optional Trace	License
Configurable 1- to 512-kbyte instruction, 2- to 16-kbyte data	Licensee option		IP core	Licensee option	Licensee option	Up to 32	Licensee option	(Core)	BVCI, AMBA bridge, JTAG to Ethernet debug, Optional Trace	License
Configurable 1- to 512-kbyte instruction, 2- to 16-kbyte data	Licensee option		IP core	Licensee option	Licensee option	Up to 32	Licensee option	(Core)	BVCI, AMBA bridge, JTAG to Ethernet debug, Optional Trace	License
Configurable 8- to 512-kbyte instruction, 8- to 256-kbyte data	Licensee option		IP core	Licensee option	Licensee option	Up to 32	Licensee option	(Core)	BVCI, AMBA bridge, JTAG to Ethernet debug, Optional Trace	License
Configurable 8- to 512-kbyte instruction, 8- to 256-kbyte data	Licensee option		IP core	Licensee option	Licensee option	Up to 32	Licensee option	(Core)	BVCI, AMBA bridge, JTAG to Ethernet debug, Optional Trace	License
Configurable 8- to 512-kbyte instruction, 8- to 256-kbyte data	Licensee option	Optional and configurable	IP core	Licensee option	Licensee option	Up to 32	Licensee option	(Core)	BVCI, AMBA bridge, JTAG to Ethernet debug, Optional Trace	License
Configurable 8- to 512-kbyte instruction, 8- to 256-kbyte data	Licensee option		IP Subsystem	Licensee option	Licensee option	Up to 32	Licensee option	(Core)	Studio quality audio; Supports multiple audio standards	License
Configurable 8- to 512-kbyte instruction, 8- to 256-kbyte data	Licensee option		IP Subsystem	Licensee option	Licensee option	Up to 32	Licensee option	(Core)	Studio quality audio; Supports multiple audio standards	License

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
ARC International www.arc.com	ARC Video Subsystem Family	ARCompact	Up to 700 worst case (90nm)	32	16, 32	1 to 5		Sleep mode, RAM controls	16/32 MUL/MAC DSP extensions Optional ARC XY subsystem	Optional FPX extensions, single and/or double precision	8- to 64-kbyte instruction/data (configurable)
ARC International www.arc.com	Energy Pro 20	ARCompact	500	32	16, 32	1 to 5	0.03 mW/MHz	Domain clock gating, Voltage domains, Dynamic voltage and frequency scaling, power management unit	16/32 MUL/MAC instructions Parallel execution of MUL, MAC and ALU Saturation, Zero overhead loop	Optional FPX extensions, single and/or double precision	Cacheless and closely coupled (single-cycle) memories
ARC International www.arc.com	Energy Pro 30	ARCompact	520	32	16, 32	1 to 5	0.05 mW/MHz	Function and architecture clock gating, Power domains and power shut off - Dynamic voltage and frequency scaling, pwr management unit	16/32 MUL/MAC instructions Parallel execution of MUL, MAC and ALU Saturation, Zero overhead loop	Optional FPX extensions, single and/or double precision	2- to 32-kbyte instruction/data (configurable)
ARC International www.arc.com	Sonic Focus Adaptive Dynamics										
ARC International www.arc.com	Sonic Focus Extrapolator										
ARC International www.arc.com	Sonic Focus X-Matrix										
ARM www.arm.com	ARM1176JZF-S	ARMv6Z	610 worst case (90G)	Quad AMBA 3 AXI	16 Thumb, 32 ARM, 8 Jazelle	1 (90nm) 0.8 with IEM	0.29 mW/MHz (90nm)	Standby, dormant, IEM	DSP, SIMD	Yes	4- to 64-kbyte (configurable)
ARM www.arm.com	ARM1176JZ-S	ARMv6Z	610 worst case (90G)	Quad AMBA 3 AXI	16 Thumb, 32 ARM, 8 Jazelle	1 (90nm) 0.8 with IEM	0.29 mW/MHz (90nm)	Standby, dormant, IEM	DSP, SIMD	Yes	4- to 64-kbyte (configurable)
ARM www.arm.com	ARM Cortex-A8	ARMv7A	650 to 1100 (65nmGP)	64/128 configurable AMBA 3 AXI	16 Thumb, 16/32 Thumb-2 Hybrid	1 (65 nmGP)	0.45 mW/MHz (with 32K/32K L1 caches)	Standby, dormant, IEM	SIMD, NEON	VFPv3	16- or 32-kbyte, L2: 0-, 64-kbyte or 2-Mbyte (configurable)
ARM www.arm.com	ARM Cortex-M3	ARMv7M	Up to 135 (0.13um)	3x AMBA AHB-Lite + AMBA APB	16 Thumb, 16/32 Thumb-2 Hybrid	1.2 (0.13)	0.14 mW/MHz (90nm)	Interrupt-based sleep, dormant and retention mode	Hardware division unit, single-cycle 32x32 multiply		
ARM www.arm.com	ARM Cortex-R4 (F)	ARMv7R	Up to 475 (90nm)	AMBA 3 AXI	16 Thumb, 32 ARM, 16/32 Thumb-2 Hybrid	1 (90nm)	0.26 mW/MHz	Standby, dormant	DSP, SIMD		0- to 64-kbyte (configurable)
ARM www.arm.com	ARM1026EJ-S	ARMv5TEJ	266 to 325 (worst case)	Dual AMBA AHB	16 Thumb, 32 ARM, 8 Jazelle	1 to 1.2 (0.13)	0.18 mW/MHz (90nm)	Yes	DSP	VFP10 co-processor	4- to 128-kbyte instruction/data (configurable)
ARM www.arm.com	ARM11 MPCore	ARMv6K	610	Single / Dual AMBA 3.0 AXI 64	16 Thumb, 32 ARM, 8 Jazelle	1 (90nm) 0.8 with IEM	0.27mW/MHz (90nm)	Standby, dormant, IEM, adaptive shutdown	DSP, SIMD	Yes, optional per processor	16- to 64-kbyte (configurable)
ARM www.arm.com	ARM1136JF-S	ARMv6	610	5 x AMBA AHB	16 Thumb, 32 ARM, 8 Jazelle	1 (90nm) 0.8 with IEM	0.18mW/MHz (90nm)	Standby, dormant	DSP, SIMD	Yes	4- to 64-kbyte instruction/data (configurable)
ARM www.arm.com	ARM1136J-S	ARMv6	610	5 x AMBA AHB	16 Thumb, 32 ARM, 8 Jazelle	1 (90nm) 0.8 with IEM	0.3 mW/MHz (0.13)	Standby, dormant	DSP, SIMD		4- to 64-kbyte instruction/data (configurable)
ARM www.arm.com	ARM1156T2F-S	ARMv6T2	610	Quad AMBA 3.0 AXI 64	16 Thumb, 32 ARM, 16/32 Thumb-2 Hybrid	1 (90nm) 0.8 with IEM	0.34mW/MHz (90nm)	Standby, dormant	DSP, SIMD	Yes	0- to 64-kbyte (configurable)
ARM www.arm.com	ARM1156T2-S	ARMv6T2	610	Quad AMBA 3.0 AXI 64	16 Thumb, 32 ARM, 16/32 Thumb-2 Hybrid	1 (90nm) 0.8 with IEM	0.34mW/MHz (90nm)	Standby, dormant	DSP, SIMD		0- to 64-kbyte (configurable)

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
Configurable 8- to 512-kbyte instruction, 8- to 256-kbyte data	Licensee option		IP Subsystem	Licensee option	Licensee option	Up to 32	Licensee option	(Core)	100% Standards compliant	License
1- to 512-kbyte Single-cycle instruction Closely Coupled Memory	Licensee option		IP core	Licensee option	Licensee option	Up to 32	Licensee option	(Core)	ARC Instruction Set extensions; API level - Power-aware MQX-EP RTOS	License
1- to 512-kbyte instruction, 2- to 256-kbyte data, both single cycle closely coupled memory	Licensee option		IP core	Licensee option	Licensee option	Up to 32	Licensee option	(Core)	ARC Instruction Set extensions; API level - Power-aware MQX-EP RTOS; 16 or 32 entry register file, extendible to 60; 26 general purpose registers, extendible to 54; 32-bit auxiliary register space	License
								(Core)		License
								(Core)		License
								(Core)		License
Configurable local: 0- to 64-kbyte	Licensee option	MMU	IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Intelligent Energy Manager, TrustZone, Jazelle (Java)	License
Configurable local: 0- to 64-kbyte	Licensee option	MMU	IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Intelligent Energy Manager, TrustZone, Jazelle (Java)	License
	Integrated L2 cache controller	MMU	IP core		Licensee option	Yes	Licensee option	(Core)	Thumb-2, NEON, Jazelle RCT, IEM, TrustZone, Superscalar pipeline, dynamic branch prediction	License
Licensee option	Licensee option	MPU	IP core	Integrated system tick, licensee option	Licensee option	Up to 244 distributor	Licensee option	(Core)	Wake Up Interrupt Controller for ultra low power	License
Configurable local: 0- to 8-Mbyte	Integrated DMA port	MPU	IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Thumb-2, cache parity protection, ECC support for TCM, Floating Point Unit	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option	MMU and MPU	IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Jazelle (Java), real-time trace	License
	Licensee option	MMU	IP core	Integrated timer and watchdog per core	Licensee option	Up to 255 distributor	Licensee option	(Core)	Cache coherence, Intelligent Energy Manager, Jazelle (Java)	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option	MMU	IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Jazelle (Java), multimedia	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option	MMU	IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Jazelle (Java), multimedia	License
Configurable local: 0- to 256-kbyte	Licensee option	MPU	IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Thumb-2, cache parity protection, ECC support for TCM	License
Configurable local: 0- to 256-kbyte	Licensee option	MPU	IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Thumb-2, cache parity protection, ECC support for TCM	License

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
ARM www.arm.com	ARM7EJ-S	ARMv5TEJ	260	AMBA AHB 32 (with wrapper)	16, 32	1 (90nm)	0.1 mW/MHz (90nm)	Yes	DSP	Optional VFP9 coprocessor	Can add external
ARM www.arm.com	ARM7TDMI	ARMv4T	Up to 236 worst case (90nm)	AMBA AHB 32 (with wrapper)	16, 32	1 (90nm)	0.03 mW/MHz (90nm)	Yes	Yes		Can add external
ARM www.arm.com	ARM7TDMI-S	ARMv4T	Up to 245 worst case (90nm)	AMBA AHB 32 (with wrapper)	16, 32	1 (90nm)	0.06mW/MHz (90 nm)	Yes	Yes		Can add external
ARM www.arm.com	ARM920T	ARMv4T	Up to 250 worst case	AMBA AHB 32 (with wrapper)	16, 32	1.2 (0.13)	0.25 mW/MHz (0.13)	Yes	Yes		16-kbyte instruction/data
ARM www.arm.com	ARM922T	ARMv4T	Up to 250 worst case	AMBA AHB 32 (with wrapper)	16, 32	1.2 (0.13)	0.25 mW/MHz (0.13 cache)	Yes	Yes		8-kbyte instruction/data
ARM www.arm.com	ARM926EJ-S	ARMv5TEJ	Up to 470 worst case (90nm)	Dual AMBA AHB	16, 32	1 (90nm)	0.11mW/MHz (90nm)	Yes	DSP	VFP9 coprocessor	4- to 128-kbyte instruction/data (configurable)
ARM www.arm.com	ARM946E-S	ARMv5TE	Up to 440 worst case (90nm)	AMBA AHB 32	16, 32	1 (90nm)	0.08mW/MHz (90)	Yes	DSP	VFP9 coprocessor	4-kbyte to 1-Mbyte instruction/data (configurable)
ARM www.arm.com	ARM966E-S	ARMv5TE	Up to 470 worst case (90nm)	Dual AMBA AHB 32	16, 32	1 (90nm)	0.07mW/MHz	Yes	DSP	VFP9 coprocessor	
ARM www.arm.com	ARM968E-S	ARMv5TE	Up to 530 worst case (90nm)	AMBA AHB-Lite	16, 32	1 (90nm)	0.06mW/MHz	Yes	DSP		
ARM www.arm.com	SC100	ARMv4T	Up to 80 worst case (0.18um)	32	16, 32	1.8 (0.18)	0.21 mW/MHz (0.18 no cache)	Yes	Yes		
ARM www.arm.com	SC200	ARMv5TEJ	Up to 110 worst case (0.18um)	32	16, 32	1.8 (0.18)	0.30 mW/MHz (0.18 cache)	Yes	DSP		Optional
ARM www.arm.com	SC300	ARMv7M	Up to 135 (0.13um)	3x AMBA AHB-Lite + AMBA APB	16 Thumb, 16/32 Thumb-2 Hybrid	1.2 (0.13)	0.14 mW/MHz (90nm)	Interrupt-based sleep, dormant and retention mode	Hardware division unit, single-cycle 32x32 multiply		
Atmel www.atmel.com	AP7 Application Processors	AVR32	150	32/16/8	16, 32	1.8/3.3	2.0 mW/MHz	7 sleep modes, Less than 400 uA	32X16 to 48x16 single cycle MAC		16-kbyte instruction/data
Atmel www.atmel.com	AT91SAM7A3	ARM7TDMI	60		16, 32	1.8 / 3 to 3.6	126 mW	315 µW, slow, standby, idle, individual peripheral clock enable	Yes		
Atmel www.atmel.com	AT91SAM7L	ARM7TDMI	36		16, 32	1.8 to 3.6	41 mW	100 nA, Slow, Idle, Wait, backup, off	Yes		
Atmel www.atmel.com	AT91SAM7S	ARM7TDMI	55		16, 32	3 to 3.6	50 to 55 mW	7.2 µA, slow, standby, idle, individual peripheral clock enable	Yes		
Atmel www.atmel.com	AT91SAM7SE	ARM7TDMI	48	23/32	16, 32	3 to 3.6	90 mW	85 µA, slow, standby, idle, individual peripheral clock enable	Yes		
Atmel www.atmel.com	AT91SAM7X (C)	ARM7TDMI	55		16, 32	3 to 3.6	88 mW	21 µA, slow, standby, idle, individual peripheral clock enable	Yes		

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
Licensee option	Licensee option		IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Jazelle (Java), real-time trace	License
Licensee option	Licensee option		IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Real-time trace	License
Licensee option	Licensee option		IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Real-time trace	License
Licensee option	Licensee option	MMU	IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Real-time trace	License
Licensee option	Licensee option	MMU	IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Real-time trace	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option	MMU	IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Jazelle (Java), real-time trace	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option	MPU	IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Real-time trace	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option		IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Real-time trace	License
Configurable local: 0- to 4-Mbyte	Licensee option		IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	Interleaved data TCM interface	License
Licensee option	Licensee option	Secure MPU	IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	SecurCore security features	License
Licensee option	Licensee option	Secure MPU	IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	SecurCore security features	License
Licensee option	Licensee option	Secure MPU	IP core	Licensee option	Licensee option	Yes	Licensee option	(Core)	SecurCore security features	License
32-kbyte SRAM	Yes	Yes, with ECC	CTBGA256, QFP208, CTBGA180	Four, 6 PWM	SPI, USART, SSC/AC97/I ² S, TWI, MMC/SD/SDIO, EBI, CF, Ethernet 10/100, USB 2.0 High Speed device, LCD driver	All peripherals and I/O	16-bit stereo DAC	-40 to +85	Pixel co-processor	From \$6.05
256-kbyte Flash, 32-kbyte SRAM		MPU	100 TQFP	Nine 16-bit, watchdog, eight PWM	2x CAN, 3x UART, TWI, USB, 2x SPI, 2x I ² S, 49 to 62 PIO	All PIO, all peripherals, eight levels	16-channel, 10-bit	-40 to +85		\$5.50 to \$8.00
64- to 128-kbyte Flash, 6-kbyte SRAM (2 kb as backup)			128-LQFP 144-LFBGA	Three 16-bit, real-time clock, watchdog, four PWM	3x UART, TWI, SPI, 80 PIO	All PIO, all peripherals, eight levels	Four-channel, 10-bit	-40 to +85	BOD, POR, High Drive, Security -bit, ISP, Segment LCD controller	\$4.50 to \$6.00
16- to 512-kbyte Flash, 4 to 64-kbyte SRAM			48 /64-TQFP 48/64-QFN	Three 16-bit, real-time, watchdog, four PWM	3x UART, TWI, USB, SPI, I ² S, 21/32 PIO	All PIO, all peripherals, eight levels	Eight-channel, 10-bit	-40 to +85	BOD, POR, High Drive, Security -bit, ISP	\$2.00 to \$6.40
32- to 512-kbyte Flash, 8 to 32-kbyte SRAM		MPU	128-LQFP 144-LFBGA	Three 16-bit, real-time, watchdog, four PWM	UART, TWI, USB, SPI, I ² S, 88 PIO	All PIO, all peripherals, eight levels	Eight-channel, 10-bit	-40 to +85	BOD, POR, High Drive, Security -bit, ISP	\$4.00 to \$8.00
128- to 512-kbyte Flash, 32 to 128-kbyte SRAM			100-LQFP 100-LFBGA	Three 16-bit, real-time, watchdog, four PWM	Ethernet, CAN, UART, TWI, USB, Two SPI, I ² S, 62 PIO	All PIO, all peripherals, eight levels	Eight-channel, 10-bit	-40 to +85	BOD, POR, High Drive, Security -bit, ISP Optional AES/TDES accelerator	\$4.85 to \$8.70

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Atmel www.atmel.com	AT91SAM9260	ARM926EJ-S	210	26/32	16, 32	1.65 to 1.95/ 3.0 to 3.6	230 mW	5 μ W, standby, shutdown, idle, slow, individual peripheral clock enable	Yes		8-kbyte instruction/data
Atmel www.atmel.com	AT91SAM9261 / AR91SAM9261S	ARM926EJ-S	240	26/32	16, 32	1.08 to 1.32/ 2.7 to 3.6	77 mW	3 μ W, standby, shutdown, idle, slow, individual peripheral clock enable	Yes		16-kbyte instruction/data
Atmel www.atmel.com	AT91SAM9263	ARM926EJ-S	240	two 26/32	16, 32	1.08 to 1.32/ 2.7 to 3.6	85 mW	4 μ W, standby, shutdown, idle, slow, individual peripheral clock enable	Yes		16-kbyte instruction/data
Atmel www.atmel.com	AT91SAM9G20	ARM926EJ-S	400	26/32	16, 32	0.9 to 1.1/ 3.0 to 3.6	85mW	9 μ W, standby, shutdown, idle, slow, individual peripheral clock enable	Yes		32-kbyte instruction/data
Atmel www.atmel.com	AT91SAM9R64 / AT91SAM9RL64	ARM926EJ-S	240	26/32	16, 32	1.08 to 1.32/ 3.0 to 3.6	56 mW	5 μ W, standby, shutdown, idle, slow, individual peripheral clock enable	Yes		4-kbyte instruction/data
Atmel www.atmel.com	AT91SAM9XE	ARM926EJ-S	210	26/32	16, 32	1.65 to 1.95/ 3.0 to 3.6	230 mW	5 μ A, idle, ultra low power, backup	Yes		16-kbyte instruction/ 8-kbyte data
Atmel www.atmel.com	Touch Technology Capacitive touch	Quantum				1.8 to 5.5					
Atmel www.atmel.com	UC3 Flash Microcontrollers	AVR32	66	32/16/8	16, 32	1.8/3.3	1.3 mW/MHz	6 sleep modes, Less than 1 μ A	32X16 to 48x16 single cycle MAC		
Beyond Semiconductor www.beyondsemi.com	Beyond BA12	BA1	Up to 250 worst case (130 nm)	wishbone 32/32	32	Process dependent	0.06 mW/MHz (130 nm)	Sleep mode, wake-up on interrupt	32 MUL, 64 MAC, hardware division		up to 16-kbyte instruction/data (configurable)
Beyond Semiconductor www.beyondsemi.com	Beyond BA14	BA1	Up to 720 worst case (90 nm)	AMBA AHB or wishbone 32/32	32	Process dependent	0.17 mW/MHz (130 nm)	Sleep mode, wake-up on interrupt	64 MUL, 64 MAC, hardware division	Optional single and/or double precision	up to 16-kbyte instruction/data up to 512-kbyte L2 (configurable)
Beyond Semiconductor www.beyondsemi.com	Beyond BA22	BA2	Up to 300 worst case (130 nm)	AMBA AHB or wishbone 32/32	16, 24, 32, 48	Process dependent	0.05 mW/MHz (130 nm)	Doze, dynamic frequency scaling, functional units power down, wake-up on interrupt	64 MUL, 64 MAC, hardware division	Optional single or double precision	up to 64-kbyte instruction/data 1 to 4-way, (configurable)
Broadcom Corporation www.broadcom.com	BCM5836	MIPS32	264	32/32	32	1.25/2.5/3.3	>1.5W	Power management	32x32		16-kbyte instruction/data, 1-kbyte pre-fetch
Cambridge Consultants www.CambridgeConsultants.com/ASIC	XAP3a	XAP	100	32/32	16, 32	1.08 (0.13)	30k gates 0.043 mW/MHz	Sleep or halt	32x32		External
Cambridge Consultants www.CambridgeConsultants.com/ASIC	XAP3b	XAP	180	32/32	16, 32	1.08 (0.13)	50k gates 0.041 mW/MHz	Sleep or halt	32x32		External
CAST www.cast-inc.com	APS2	RISC (78 instructions)	100 to 300	32/32	32		18 μ W/MHz	Sleep	Optional DSP coprocessor, barrel shifter and multiplier		Optional 8-kbyte instruction

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
Two banks of 4-kbyte SRAM	SDRAM, CF, Smart Media, NAND Flash, ECC, static memory	Yes	208 PQFP, 217 LFBGA	Six 16-bit, real-time, watchdog	Ethernet, USB host and device, MCI, UART, TWI, SPI, I ² S, 96 PIO	All PIO, all peripherals, eight levels	Four-channel 10-bit	-40 to +85	Image Sensor Interface	\$6.75
160-kbyte SRAM / 16 kbyte SRAM	SDRAM, Compact Flash, Smart Media, NAND Flash, static memory	Yes	217 LFBGA	Three 16-bit, real-time, watchdog	USB host and device, MCI, UART, TWI, SPI, I ² S, 96 PIO	All PIO, all peripherals, eight levels		-40 to +85	LCD Controller Real-Time trace	\$6.75 to \$8.70
96-kbyte SRAM	2x (SDRAM, CF, Smart Media, NAND Flash, static memory)	Yes	324 LFBGA	Three 16-bit, four PWM, real time, watchdog	Ethernet, USB host and device, CAN, 2x MCI, 4x UART, TWI, 2x SPI, 2x I ² S, 160 PIO	All PIO, all peripherals, eight levels		-40 to +85	Image Sensor Interface, LCD Controller, 2D graphic accelerator, Real-Time trace, AC97 controller	\$11.35
Two banks of 16-kbyte SRAM	SDRAM, CF, Smart Media, NAND Flash, ECC, static memory	Yes	217 LFBGA	Six 16-bit, real-time, watchdog	Ethernet, USB host and device, MCI, UART, TWI, SPI, I ² S, 96 PIO	All PIO, all peripherals, eight levels	Four-channel 10-bit	-40 to +85	Image Sensor Interface	\$7.25
64-kbyte SRAM	SDRAM, CF, Smart Media, NAND Flash, static memory	Yes	144 BGA, 217 LFBGA	Three 16-bit, four PWM, real time clock, watchdog	USB device HS, MCI, 5x UART, TWI, SPI, 2x I ² S, 118 PIO	All PIO, all peripherals, eight levels		-40 to +85	LCD controller, AC97 controller	\$6.35 to \$7.40
128- to 512-kbyte Flash, 16 to 32-kbyte SRAM	SDRAM, Compact Flash, Smart Media, NAND Flash, ECC, static memory	Yes	208 PQFP, 217 LFBGA	Six 16-bit, real-time, watchdog	Ethernet, USB host and device, MCI, 6x UART, 2x TWI, 2x SPI, I ² S, 96 PIO	All PIO, all peripherals, eight levels	Four-channel 10-bit	-40 to +85	Image Sensor Interface	\$7.90 to \$9.50
			QFN, TQFP, PDIP, and SOIC					-40 to +85	Touch Keys, Wheels, and Sliders	
128- to 512 Kb Flash 32- to 64 Kb SRAM	Yes	MPU	LQFP144, TQFP100, VQFN64, TQFP64, TQFP48	Six, 13 PWM	SPI, USART, SSC/I ² S, TWI, EBI, Ethernet 10/100, Device 2.0 Full Speed and On-The-Go (OTG) USB	All peripherals and I/O	16-bit audio DAC	-40 to +85		From \$2.89
Licensee option, Configurable local memory	Licensee option, multi port DDR 1/2/3, SDRAM, SRAM/Flash	Optional and configurable MMU	IP Core	32-bit with match and capture, OS Timer, realtime	Licensee option, Ethernet 10/100/1000, UART, VGA/DVI Display, AC97, PCI bridge, PS/2	Up to 32	Licensee option	(Core)	Available also as Verilog RTL source, JTAG debug, Optional Trace	License
Licensee option	Licensee option, multi port DDR 1/2/3, SDRAM, SRAM/Flash	Configurable MMU	IP Core	32-bit with match and capture, OS Timer, realtime	Licensee option, Ethernet 10/100/1000, UART, VGA/DVI Display, AC97, PCI bridge, PS/2	Up to 32	Licensee option	(Core)	Available also as Verilog RTL source, JTAG debug, Optional Trace, superscalar, dual issue out of order execution	License
Licensee option, Configurable local memory	Licensee option, multi port DDR 1/2/3, SDRAM, SRAM/Flash	Optional and configurable MMU	IP Core	32-bit with match and capture, OS Timer, realtime with separate power domain	Licensee option, Ethernet 10/100/1000, UART, VGA/DVI Display, AC97, PCI bridge, PS/2	Up to 32	Licensee option	(Core)	Available also as Verilog RTL source, JTAG debug, Optional Trace, High code density	License
8- to 512-Mbyte SDR/DDR DRAM, up to 32-Mbyte flash/SRAM	Distribute DMA, 8/16/32bit DRAM, 8/16bit external	32-entry TLB	340 PBGA	Two, watchdog	Two 10/100 Ethernet, two UART, PCMCIA, IDE, PCI 32bit/33Mhz, USB host/device, Audio, V.92 Modem, IR, GPIO	Many sources		0 to +70	EJTAG debug, VPN/IPSec hardware processor	
4-Gbyte	External	Yes	IP core	External	External	256		+125	0.76 DMIPS/MHz High code density	License
4-Gbyte	External	Yes	IP core	External	External	256		+125	0.66 DMIPS/MHz High code density	License
4-Gbyte	Optional		IP core	Timer	32-bit	Up to 256		N/A (Core)	Coprocessor interface (Barrel shifter and multiplier available)	License

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
CAST www.cast-inc.com	APS3	RISC (140 instructions)	100 to 300	32/32	16, 32		24 μ W/MHz	Sleep	Optional DSP coprocessor, barrel shifter and multiplier		Optional 8-kbyte instruction
Cavium Networks www.caviumnetworks.com	NITROX Soho CN201	MIPS32	150 to 166	32 (PCI) 8 or 16 (ELB)	32	1.8, 3.3	1.2				16-kbyte instruction/data
Cavium Networks www.caviumnetworks.com	NITROX Soho CN210	MIPS32	166, 200	32 (PCI) 8 or 16 (ELB)	32	1.8, 3.3	1.5				16-kbyte instruction/data
Cavium Networks www.caviumnetworks.com	NITROX Soho CN220	MIPS32	166, 200	32 (PCI) 8 or 16 (ELB)	32	1.0, 1.8, 3.3	2				16-kbyte instruction/data
Cavium Networks www.caviumnetworks.com	NITROX Soho CN225	MIPS32	166, 200	32 (PCI) 8 or 16 (ELB)	32	1.0, 1.8, 3.3	2.5				16-kbyte instruction/data
Cirrus Logic www.cirrus.com	EP7309	ARM720T	74	32	16, 32	2.5/3.3	90 mW	Less than 0.03 mW, power management			8-kbyte unified
Cirrus Logic www.cirrus.com	EP7311	ARM720T	74, 90	32	16, 32	2.5/3.3	108 mW	Less than 0.03 mW, power management			8-kbyte unified
Cirrus Logic www.cirrus.com	EP7312	ARM720T	74, 90	32	16, 32	2.5/3.3	108 mW	Less than 0.03 mW, power management			8-kbyte unified
Cirrus Logic www.cirrus.com	EP9301	ARM920T	166	16	16	1.8/3.3	550 mW	Less than 1 mW, power management			16-kbyte instruction/data
Cirrus Logic www.cirrus.com	EP9302	ARM920T	200	16	16	1.8/3.3	550 mW	Less than 1 mW, power management	200-MHz MaverickCrunch	200-MHz Maverick-Crunch	16-kbyte instruction/data
Cirrus Logic www.cirrus.com	EP9307	ARM920T	200	32	16, 32	1.8/3.3	550 mW	Less than 1 mW, power management	200-MHz MaverickCrunch	200-MHz Maverick-Crunch	16-kbyte instruction/data
Cirrus Logic www.cirrus.com	EP9312	ARM920T	200	32	16, 32	1.8/3.3	550 mW	Less than 1 mW, power management	200-MHz MaverickCrunch	200-MHz Maverick-Crunch	16-kbyte instruction/data
Cirrus Logic www.cirrus.com	EP9315	ARM920T	200	32	16, 32	1.8/3.3	550 mW	Less than 1 mW, power management	200-MHz MaverickCrunch	200-MHz Maverick-Crunch	16-kbyte instruction/data

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
4-Gbyte	Optional		IP core	Timer	32-bit	Up to 256		N/A (Core)	Coprocessor interface (Barrel shifter and multiplier available)	License
Up to 256-Mbyte DRAM, 32-Mbyte Flash	SDRAM	Simple block address translation mechanism	276 PBGA	Two	3 FE, Two UART, optional PIO	28 internal, 4 external		-40 to +85	Cryptographic co-processor for IPsec, FIPS-compliant RNG	Less than \$10
Up to 256-Mbyte DRAM, 32-Mbyte Flash	SDRAM	Simple block address translation mechanism	276 PBGA	Two	3 FE, Two UART, optional PIO	28 internal, 4 external		-40 to +85	Cryptographic co-processor for IPsec, FIPS-compliant RNG	Less than \$15
Up to 256-Mbyte DRAM, 32-Mbyte Flash	SDRAM	Simple block address translation mechanism	276 PBGA	Two	3 FE, Two UART, optional PIO	28 internal, 4 external		-40 to +85	Cryptographic protocol offload for IPsec, SSL and wireless protocols, FIPS-compliant RNG	Less than \$20
Up to 256-Mbyte DRAM, 32-Mbyte Flash	SDRAM	Simple block address translation mechanism	276 PBGA	Two	3 FE, Two UART, optional PIO	28 internal, 4 external		-40 to +85	Cryptographic protocol offload for IPsec, SSL and wireless protocols, FIPS-compliant RNG	Less than \$25
48-kbyte SRAM	8-, 16-, 32-bit SRAM/Flash/ROM	64-entry TLB	208 LQFP, 256 PBGA, 204 TFBGA	Two 16-bit	Two SSI, IrDA, two UART, two PWM, 27 GPIO	22		-40 to +85	LCD controller, 32-/128-bit unique MaverickKey ID, touchscreen interface, glueless digital audio, CODEC interface, JTAG	\$6.11
48-kbyte SRAM	8-, 16-, 32-bit SRAM/Flash/ROM, 32-bit SDRAM	64-entry TLB	208 LQFP, 256 PBGA, 204 TFBGA	Two 16-bit	Two SSI, IrDA, two UART, two PWM, 27 GPIO	22		-40 to +85	LCD controller, 32-/128-bit unique MaverickKey ID, touchscreen interface, JTAG	\$6.51
48-kbyte SRAM	8-, 16-, 32-bit SRAM/Flash/ROM, 32-bit SDRAM	64-entry TLB	208 LQFP, 256 PBGA, 204 TFBGA	Two 16-bit	Two SSI, IrDA, two UART, two PWM, 27 GPIO	22		-40 to +85	LCD controller, 32-/128-bit unique MaverickKey ID, touchscreen interface, glueless digital audio, CODEC interface, JTAG	\$7.54
	8-, 16-bit SRAM/Flash/ROM, 16-bit SDRAM, EPROM, 12-channel DMA	64-entry TLB	208 QFP	Two 16-bit, 32-bit, 40-bit, two PWM, watchdog	Two SSI, IrDA, six I ² S, SPI, two UART with HDLC, two USB 2.0 Host, AC'97, 10/100 Ethernet, 24 GPIO	64	12-bit	-40 to +85	32/128-bit unique MaverickKey ID, glueless digital audio, CODEC interface	\$8.27
	8-, 16-bit SRAM/Flash/ROM, 16-bit SDRAM, EPROM, 12-channel DMA	64-entry TLB	208 QFP	Two 16-bit, 32-bit, 40-bit, two PWM, watchdog	Two SSI, IrDA, six I ² S, SPI, two UART with HDLC, two USB 2.0 Host, AC'97, 10/100 Ethernet, 24 GPIO	64	12-bit	-40 to +85	32/128-bit unique MaverickKey ID, glueless digital audio, CODEC interface	\$9.96
	8-, 16-, 32-bit SRAM/Flash/ROM, 32-bit SDRAM, EPROM, 12-channel DMA	64-entry TLB	272 TFBGA	Two 16-bit, 32-bit, 40-bit, two PWM, watchdog	Two SSI, IrDA, six I ² S, SPI, three UART with HDLC, three USB 2.0 Host, AC'97, 10/100 Ethernet, 8x8 Keypad, 65 GPIO	64	12-bit	-40 to +85	CRT/LCD/NTSC/PAL display controller, touchscreen interface, 32/128-bit unique MaverickKey ID, glueless digital audio, CODEC interface	\$12.60
	8-, 16-, 32-bit SRAM/Flash/ROM, 32-bit SDRAM, EPROM, 12-channel DMA	64-entry TLB	352 PBGA	Two 16-bit, 32-bit, 40-bit, two PWM, watchdog	Two SSI, IrDA, six I ² S, SPI, three UART with HDLC, three USB 2.0 Host, AC'97, two IDE, 10/100 Ethernet, 8x8 Keypad, 65 GPIO	64	12-bit	-40 to +85	CRT/LCD/NTSC/PAL display controller, touchscreen interface, 32/128-bit unique MaverickKey ID, glueless digital audio, CODEC interface	\$15.78
	8-, 16-, 32-bit SRAM/Flash/ROM, 32-bit SDRAM, EPROM, 12-channel DMA	64-entry TLB	352 PBGA	Two 16-bit, 32-bit, 40-bit, two PWM, watchdog	Two SSI, IrDA, six I ² S, SPI, three UART with HDLC, three USB 2.0 Host, AC'97, two IDE, PCMCIA interface, 10/100 Ethernet, 8x8 Keypad, 65 GPIO	64	12-bit	-40 to +85	CRT/LCD/NTSC/PAL display controller, touchscreen interface, 32/128-bit unique MaverickKey ID, glueless digital audio, CODEC interface	\$17.48

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Connect One Semiconductors Inc. www.connectone.com	C02064	ARM	48	32	16,32	1.2	190mA	Sleep mode current: less than 200 uA			
Connect One Semiconductors Inc. www.connectone.com	CO2128	ARM	48	32	16,32	1.2	190mA	Sleep mode current: less than 200 uA			
Cradle Technologies www.cradle.com	CT3400	CRADLE	230	32/64	20/32 DSP/GPP	1.25	3.5W	2W	8x8/16x16/32x32 MACs, 20/40/80-bit accumulators	Yes	Two 32-kbyte instruction
Cradle Technologies www.cradle.com	CT3616	CRADLE	230 to 350	32/64	20/32 DSP/GPP	1.18 to 1.26	1.5 to 4.8W	1W	8x8/16x16/32x32 MACs, 20/40/80-bit accumulators	Yes	Two 32-kbyte instruction
Digi International www.digi.com	NS7520	RISC	55	28/32	16, 32	1.5/3.3	500 mW	Automatic Clock Scaling, low-power sleep mode	Yes		4/4-kbyte instruction/data
Digi International www.digi.com	NS9210	RISC	75, 150	17/16	16, 32	1.5/3.3	500 mW		Yes		4/4-kbyte instruction/data
Digi International www.digi.com	NS9215	RISC	75, 150	17/16	16, 32	1.5/3.3	500 mW	Automatic Clock Scaling, low-power sleep mode	Yes		4/4-kbyte instruction/data
Digi International www.digi.com	NS9360	RISC	177	32/32	16, 32	1.5/3.3	1.7W		Yes		8/4-kbyte instruction/data
Digi International www.digi.com	NS9750	RISC	200	32/32	16, 32	1.5/3.3	1.7W		Yes		8/4-kbyte instruction/data
Digi International www.digi.com	NS9775	RISC	200	32/32	16, 32	1.5/3.3	1.7W		Yes		8/4-kbyte instruction/data
Freescale www.freescale.com	ColdFire MCF520x	ColdFire	64, 80	32/16	16, 32, 48	1.5/2.5, 3.3		Stop, clock divides PLL bypass distributed clocking	Hardware divide, Enhanced MAC		8-kbyte (configurable)
Freescale www.freescale.com	ColdFire MCF521x	ColdFire	64, 80	external	16, 32, 48	3.3	0.218W	Yes	Hardware MAC		
Freescale www.freescale.com	ColdFire MCF522x	ColdFire	66, 80		16, 32, 48	3.3		Yes	Hardware divide, MAC		
Freescale www.freescale.com	ColdFire MCF523x	ColdFire	66, 80		16, 32, 48	3.3		Yes	Hardware divide, Enhanced MAC		
Freescale www.freescale.com	ColdFire MCF523x	ColdFire	80 to 150	32/24	16, 32, 48	1.5/3.3		Yes	Hardware divide, Enhanced MAC		8-kbyte (configurable)

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
256-kbyte	16 bit SRAM		64-pin LQFP, RoHS-compliant	16-bit watchdog	Two USARTs, Two Wire, SPI, Synchronous Serial Controller, USB v2.0 Host and Device, External Bus Interface, High-Speed Parallel Bus	16	10-bit	-40 to +85	10/100 BaseT ethernet MAC, Hardware encryption supporting 3DES, SHA-1/256, AES-128/192/256	\$6
256-kbyte	16 bit SRAM		128-pin LQFP, RoHS-compliant	16-bit watchdog	Two USARTs, Two Wire, SPI, Synchronous Serial Controller, USB v2.0 Host and Device, External Bus Interface, High-Speed Parallel Bus	16	10-bit	-40 to +85	10/100 BaseT Ethernet, hardware encryption supporting 3DES, SHA-1/256, AES-128/192/256	\$7
148-kbyte	64-bit SDRAM, two memory transfer engines		456 FG	8 DDS generators driving 32 32-bit Counter/Timers	128 I/O, 16 state machines, 4 high-speed (100 MHz) and low-speed devices	16 level or edge pin, 64 hardware semaphore, 32 counter		0 to +90	16 DSPs + 8 GPPs: 4 I/O channels: 128 hw semaphores: JTAG, RNG: BKPT, single-step	\$41
460-kbyte	32/64-bit DDR SDRAM, eight DMA		676 FG	8 DDS generators driving 32 32-bit Counter/Timers	144 I/O, 18 state machines, 8 high-speed (100 MHz) and low-speed devices	16 level or edge pin, 64 hardware semaphore, 32 counter		0 to +90	16 DSPs + 8 GPPs: 8 I/O channels: 128 hw semaphores: PCI, JTAG, RNG: BKPT, single-step	\$40 to \$90
	SRAM, SDRAM, EDO DRAM, Flash, 13-channel DMA		177 BGA	Two 27-bit, watchdog, bus	Two UART, two SPI, 16 PIO, 10/100 Ethernet	4 external		-40 to +85		starting at \$7.95
	SDRAM, static RAM, Flash	Yes	177 BGA	10 32-bit timers and PWM	Four UART, SPI, I2C, Up to 54 GPIO, 10/100 Ethernet	4 external	12-bit ADC	-40 to +85	AES acceleration, Flexible Interface Modules	\$7.95
	SDRAM, static RAM, Flash	Yes	265 BGA	10 32-bit timers and PWM	Two UART, two SPI, up to 108 GPIO, 10/100 Ethernet	4 external	12-bit ADC	-40 to +85	AES acceleration, Flexible Interface Modules	\$9.95
	SDRAM, static	Yes	272 BGA	16 programmable 16- or 32-bit, watchdog, system bus monitor, system bus arbiter	50 GPIO, four programmable serial (UART, SPI master /slave), USB host/device, 10/100 Ethernet, 1284, I2C	4 external		-40 to +85	Four parallel JBIG decoders for single-pass and four-pass color and monochrome laser printers, LCD controller	starting at \$10.95
	SDRAM, static	Yes	352 BGA	16 programmable 16- or 32-bit, watchdog, system bus monitor, system bus arbiter	50 GPIO, four programmable serial (UART, SPI master /slave), USB host/device, 10/100 Ethernet, 1284, I2C	4 external		-40 to +85	LCD controller, PCI/CardBus	starting at \$14.95
	SDRAM, static	Yes	352 BGA	16 programmable 16- or 32-bit, watchdog, system bus monitor, system bus arbiter	50 GPIO, four programmable serial (UART, HDLC, SPI master /slave), USB host/device, 10/100 Ethernet, 1284, I2C	4 external		-40 to +85	Four parallel JBIG decoders for single-pass and four-pass color and monochrome laser printers, LCD controller, PCI/CardBus	
16-kbyte SRAM	DDR or SDR SDRAM		MAPBGA, QFP, LQFP	Four-channel 32-bit with DMA	Three UART, QSPI, I2C, 10/100 Ethernet	Yes		-40 to +85	Background debug	\$4.99 to \$7.69
16- to 32-kbyte SRAM, 128- to 256-kbyte Flash	Flash, SRAM		MAPBGA, LQFP	Four 32-bit with DMA, four 16-bit	CAN 2.0B (FlexCAN) with 16 message buffers, QSPI, three UART, I2C, GPIO	Yes	Eight-channel, 12 bit	-40 to +85	Background debug	\$4.99 to \$7.69
16-kbyte SRAM, 128-kbyte Flash or 32-kbyte SRAM, 256-kbyte Flash	4-channel DMA		81 MAPBGA, 64/100 LQFP	4-channel, 16- and 32 bit, 4-channel 16-bit PWM; two Periodic Interrupt Timer	USB OTG Full-Speed, three UARTs, I2C, QSPI, up to 52 GPIOs	Yes	Eight-channel, 12 bit	-40 to +85	Real Time Clock, Background Debug	\$5.49 to \$6.99
32-kbyte SRAM, 128- to 256-kbyte Flash	4-channel DMA		121 MAPBGA, 80/112 LQFP	4-channel, 16- and 32 bit, 4-channel 16-bit PWM; two Periodic Interrupt Timer	10/100 Fast Ethernet, three UARTs, I2C, optional CAN 2.0B, up to 73 GPIOs	Yes	Eight-channel, 12 bit	-40 to +85	Ethernet PHY, Optional Encryption, Real Time Clock, Background Debug	\$7.99 to \$11.32
64-kbyte SRAM	SRAM, SDRAM		QFP, MAPBGA	Four 32-bit with DMA, four 16- or 32-channel eTPU	One or two CAN, Optional 10/100 Ethernet, I2C, three UART, QSPI	Yes		-40 to +85	Optional encryption, background debug	\$10 to \$15

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Freescale www.freescale.com	ColdFire MCF527x	ColdFire	100 to 166	32/16	16, 32, 48	1.5/3.3 (2.5 DDR)		Yes	Hardware divide, Enhanced MAC		8- or 16-kbyte (configurable)
Freescale www.freescale.com	ColdFire MCF528x	ColdFire	66, 80	32	16, 32, 48	3.3		Yes	Hardware divide, Enhanced MAC		2-kbyte instruction/data
Freescale www.freescale.com	ColdFire MCF52xx	ColdFire	25 to 140	32/32 or 16	16, 32, 48	1.8/3.3/5	183 mW (MCF5249)	Yes	Hardware divide, MAC/EMAC		Up to 4-kbyte instruction, or configurable 8-kbyte
Freescale www.freescale.com	ColdFire MCF5307	ColdFire	66, 90	32/32	16, 32, 48	3.3	950 mW		Hardware divide, MAC		8-kbyte unified
Freescale www.freescale.com	ColdFire MCF532x	ColdFire	240	32/32 or 16 or 8	16, 32, 48	1.5/3.3		Yes	Hardware divide, Enhanced MAC		16-kbyte instruction/data
Freescale www.freescale.com	ColdFire MCF537x	ColdFire	180, 240	32/32 or 16 or 8	16, 32, 48	1.5/3.3		Yes	Hardware divide, Enhanced MAC		16-kbyte instruction/data
Freescale www.freescale.com	ColdFire MCF5407	ColdFire	162, 220	32/32	16, 32, 48	1.8/3.3	670 mW		Hardware divide, MAC		16/8-kbyte instruction/data
Freescale www.freescale.com	ColdFire MCF548x MCF547x	ColdFire	166, 200, 266	32/32	16, 32, 48	1.5/3.3 (2.5 DDR)		Yes	Hardware divide, Enhanced MAC	Yes	32-kbyte instruction/data
Freescale www.freescale.com	MAC7100	ARM	40	20/16	16 or 32	2.5/ 3.3 to 5.0					
Freescale www.freescale.com	MCF51QE128	ColdFire	50	25		1.8 to 3.6	6 mA	Ultra low power wait, stop			
Freescale www.freescale.com	MP8560 PowerQUICC III	Power Architecture	667 to 1000	64/64	32	1.2	7.4W	Doze, nap, sleep		Yes	32-kbyte instruction/data, L2: 256-kbyte unified
Freescale www.freescale.com	MP8568 PowerQUICC III 8568, 8567	Power Architecture	800 to 1333	64/64	32	1.2		Doze, nap, sleep		Yes	32-kbyte instruction/data, L2: 512-Kbyte unified
Freescale www.freescale.com	MPC521e	Power Architecture	400	32/64	64	1.4 / 3.3	Less than 2W	Doze, Nap, Sleep, Deep Sleep, Hibernation <25 uA		Yes	32-kbyte instruction/data, eight-way set-associative

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64-kbyte SRAM	DDR or SDR SDRAM		MAPBGA, QFP	Four 32-bit, four programmable interrupt timers, watchdog	One or two 10/100 Ethernet, I ² C, three UART, QSPI, USB	Yes		0 to +70 -40 to +85	Optional encryption, background debug	\$7.50 to \$12.25
64-kbyte SRAM; up to 512-kbyte Flash	4-channel DMA; SDR SDRAM		256 MAPBGA	4-channel, 16- and 32-bit, 4-channel 16-bit PWM; two Periodic Interrupt Timer	One 10/100 Ethernet, One CAN 2.0B, I ² C, three UART, QSPI, up to 150 GPIOs	Yes	Eight-channel, 10-bit	-40 to +85	Background Debug	\$14.66 to \$17.45
Up to 96-kbyte SRAM	EDO, FPM, SDRAM		QFP, BGA	Two to eight 16-bit, four 32-bit, four programmable interval	FlexCAN, 10/100 Ethernet, up to two I ² C, up to three UART, QSPI, USB, SPDIF, TDM	Yes	Eight- to 10-channel, 10- to 12-bit	0 to +70 -40 to +85	Background debug, IDE interface	\$6.99 to \$17.99
4-kbyte SRAM	EDO, FPM, SDRAM		QFP	Two 16-bit	I ² C, two UART	Yes		0 to +70 -40 to +85	Background debug	\$11.35 to \$14.95
32-kbyte SRAM	16-channel DMA; DDR or SDR SDRAM		196/256 MAPBGA	4-channel 32-bit, 2- or 4-channel 16-bit PWM; four Periodic Interrupt Timer	Optional 10/100 Ethernet, Optional CAN 2.0B, Full Speed USB Host & Full-Speed/High-Speed USB OTG, I ² C, three UART, QSPI, up to 97 GPIO	Yes		-40 to +85	SVGA LCD, Optional Encryption, High Speed OTG via ULPI Interface, Background Debug	\$10 to \$14
32-kbyte SRAM	16-channel DMA; DDR or SDR SDRAM		196 MAPBGA, 160 QFP	4-channel 32-bit, 4-channel 16-bit PWM, four Periodic Interrupt Timer	One 10/100 Ethernet, Optional Full Speed USB Host & Full-Speed/High-Speed USB OTG, I ² C, three UART, QSPI, up to 62 GPIO	Yes		-40 to +85	Optional Encryption, High Speed OTG via ULPI Interface, Background Debug	\$11.00 to \$12.50
4-kbyte SRAM	EDO, FPM, SDRAM		QFP	Two 16-bit	I ² C, UART, USART	Yes		0 to +70 -40 to +85	Background debug	\$18.95 to \$22.95
32-kbyte SRAM	DDR, SDR SDRAM	Yes	388 PBGA	Four 32-bit, two 32-bit slice, watchdog	I ² C, DSPI, UART, USART, four PSC. Up to two 10/100 Ethernet, up to two CAN 2.0B, optional USB 2.0 with PHY, IrDA, modem	Yes		0 to +70 -40 to +85	Optional encryption, background debug, pin compatibility	\$16.95 to \$26.47
1-Mbyte Flash, 32-kbyte data Flash, 48-kbyte SRAM	DMA		112/144 LQFP, 208 MAPBGA	16-channel eMIOS	Four eSCI with 13-bit break for LIN, two DSPI, four CAN, I ² C		32-channel dual 10-bit (5V)	-40 to +125	Nexus IEEE-ISTO 5001-2003 Class 2, PLL	\$14.20 to \$20.87
64 to 128K, 4 to 8-kbyte RAM			80 LQFP, 64 LQFP	16-bit; 6-channel, two 3-channel	2 SCI, 2 I ² C, 2 SPI		24 channel; 12-bit ADC	-40 to +85	Internal Clock Source, 70 GPIO, Low power 32 kHz oscillator	\$3.80
64-kbyte DPRAM	DDR-1 SDRAM, SDRAM, DRAM, SRAM, Flash	64-entry TLB, four-way set-associative, L2; 16-entry TLB, fully associative, 256-entry TLB, two-way set-associative	783 FCBGA	Four 16-bit or two 32-bit, real-time	Two 10/100/1000 and three 10/100 Ethernet, ATM, transparent; two 128-channel of HDLC or transparent; four serial for Ethernet, HDLC, UART, BISYNC, transparent; I ² C, SPI, PCI/PCI-X, local bus, RapidIO, Local Bus PCI/PCI-X, 8 (RapidIO)	16 programmable, 16 levels, 12 external, 4 message, 22 other internal sources		-40 to +105 (junction)	e500 core, hardware coherency, time slot assigner, eight TDM interfaces, transmission convergence layer for ATM, IMA, four baud rate generators, debug interface	Starts at \$81
64-kbyte DPRAM	DDR-1/2 SDRAM, SDRAM, DRAM, SRAM, Flash	64-entry TLB, four-way set-associative, L2; 256-entry TLB, two-way set-associative, 16-entry TLB, fully associative	1023 FCBGA	Four 16-bit or two 32-bit	Two enhanced 10/100/1000 Ethernet. QUICC Engine supporting Eight 10/100, three 10/100/1000, two UTOPIA for ATM/POS, eight TDM, 2xSPI, 32-bit PCI. DUART, Dual I ² C, 32-bit PCI, PCI-Express, local bus, GPIO, SRIIO, Local Bus	16 programmable, 16 levels, 12 external, 4 message, 22 other internal sources		0 to +105 -40 to +105 (junction)	e500 core, hardware coherency, security engine (Ipsec, SSL, XOR), Table Lookup Unit (TLU)	Starts at \$99
128-kbyte SRAM	64-channel	64-entry instruction and data TLB, two-way set associative	TePBGA 27x27mm, 1mm pitch	8 / 8	PSC (UART, SPI, AC97, I ² S, multi-ch audio), I ² C, CAN, J1850, SPDIF, Ethernet, PCI-2.3, USB2.0 OTG, SATA, PATA, MMC/SD/SDIO, NAND Flash, LCD Display	Yes		-40 to 125C junction	Integrated audio acceleration core and PowerVR MBX/VGP 3D graphics core.	

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Freescale www.freescale.com	MPC5200 (760 MIPS)	Power Architecture	266, 400	32	32	1.5/3.3	1.4W	Doze, nap, sleep, deep sleep. 50 mW		Double precision	16-kbyte instruction/data, four-way set-associative
Freescale www.freescale.com	MPC5200B (885 MIPS)	Power Architecture	266, 400, 466	32	32	1.5/3.3	1.5W	Doze, nap, sleep, deep sleep. 50 mW		Double precision	16-kbyte instruction/data, four-way set-associative
Freescale www.freescale.com	MPC5500	Power Architecture	40, 80, 132	32/32	32	1.5/3.3/5.0			SPE (SIMD)	Yes	Up to 32-kbyte unified
Freescale www.freescale.com	MPC5510 Family (two cores)	Power Architecture	48, 66, 80	32/32	32	5.0	0.8W	multiple stop modes, periodic wake-up from internal osc.			
Freescale www.freescale.com	MPC5602S	Power Architecture	Up to 64	32/32	32	1.2/5		multiple stop modes, periodic wake-up from internal osc.			
Freescale www.freescale.com	MPC5604S	Power Architecture	Up to 64	32/32	32	1.2/5		multiple stop modes, periodic wake-up from internal osc.			
Freescale www.freescale.com	MPC5606S	Power Architecture	Up to 64	32/32	32	1.2/5		multiple stop modes, periodic wake-up from internal osc.			
Freescale www.freescale.com	MPC560xB	Power Architecture	Up to 64	32/32	32	1.2 /5	0.6W	multiple stop modes, periodic wake-up from internal osc.			
Freescale www.freescale.com	MPC563xM	Power Architecture	40, 60, 80	32/32	32	5			SPE (SIMD)		
Freescale www.freescale.com	MPC603	Power Architecture	200, 266, 300	32/64	64	2.5/3.3	4.0W/6.1W (300 MHz)	Doze, stop		Yes	16-kbyte instruction/data, four-way set-associative
Freescale www.freescale.com	MPC7447A	Power Architecture	600, 733, 867, 1000, 1167, 1267, 1333, 1420	36/65	64	1.3/2.5	21W/30W (1420 MHz)	Nap, sleep, deep sleep		Yes	32-kbyte instruction/data, eight-way set-associative
Freescale www.freescale.com	MPC7448	Power Architecture	600 to 1700	36/64	32	1.0 to 1.3/1.8,2.5,3.3	21W	Nap, sleep, deep sleep	128-bit Altivec vector processor	IEEE 754-1985 single and double precision	32-kbyte instruction/data, eight-way set-associative, L2: 1-Mbyte eight-way set associative with ECC
Freescale www.freescale.com	MPC8245 PowerQUICC	Power Architecture	266, 300, 333, 350, 400	64	32	1.8/2	2.8W	Doze, stop		Yes	16-kbyte instruction/data, four-way set-associative
Freescale www.freescale.com	MPC8260 PowerQUICC II 8260, 8250, 8255, 8264, 8265, 8266	Power Architecture	266, 300	64	32	1.8 to 2.2	2.4W	Doze, stop		Yes	16-kbyte instruction/data, four-way set-associative

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
16-kbyte virtual DMA, dedicated I/O buffers	DDR, SDR SDRAM	64-entry TLB, two-way set associative	272 TEPBGA	Eight	Flash/RAM/ROM, two USB, 10/100 baseT, six PSC, two CAN, J1850, two I ² C, I ² S, SPI, up to 56 GPIO	Standard and critical, four external		0 to +70 -40 to +85	PCI, ATA/IDE	
16-kbyte virtual DMA, dedicated I/O buffers	DDR, SDR SDRAM	64-entry TLB, two-way set associative	272 TEPBGA	Eight	Flash/RAM/ROM, two USB, 10/100 baseT, six PSC, two CAN, J1850, two I ² C, I ² S, SPI, up to 56 GPIO	Standard and critical, four external		0 to +70 -40 to +85 -40 to +105	PCI, ATA/IDE	\$16.19 to \$17.61
Up to 3-Mbyte Flash, 128-kbyte SRAM, 24-kbyte eTPU RAM	DMA	Yes	324/416 TePBGA, 208 Map BGA	24-channel eMIOS, up to 64 channel eTPU (programmable)	Up to two eSCI, up to four DSPI, up to five CAN, Ethernet	Yes	40-channel dual 12-bit (5V)	-40 to +125	Nexus IEEE-ISTO 5001-2003 Class 3+, FM-PLL	\$19.99 to \$119.97
Up to 1.5-MByte Flash, 80-kbyte RAM	eDMA	MMU, MPU	144LQFP, 176LQFP, 208MAPBGA	24-channel eMIOS	Up to 8 eSCI (with LIN master protocol capability)	yes	40-channel 12-bit QADC	0 to +85C 0 to +105C 0 to +125C	Nexus 2+	\$15 to \$40
256-kbyte Flash, 24-kbyte RAM	16-channel	MPU	100 LQFP, 144 LQFP	Various	CAN, two SCI, two SPI, two I ² C	Yes	16-channel 10bit	-40 to +85C -40 to +105C	Instrumentation Gauge driver. LCD driver. Sound Generator.	
512-kbyte Flash, 48-kbyte RAM	16-channel	MPU	100 LQFP, 144 LQFP	Various	CAN, two SCI, two SPI, two I ² C	Yes	16-channel 10bit	-40 to +85C -40 to +105C	Instrumentation Gauge driver. LCD driver. Sound Generator.	
1-Mbyte Flash, 48-kbyte RAM, 160-kbyte Graphics RAM	16-channel	MPU	144 LQFP, 176 LQFP	Various	Two CAN, two SCI, three SPI, four I ² C	Yes	16-channel 10bit	-40 to +85C -40 to +105C	TFT Display driver. Instrumentation Gauge driver. LCD driver. Sound Generator.	
Up to 512-kbyte Flash, 32-kbyte RAM		MPU	100LQFP, 144 LQFP	56-channel eMIOS		yes	36-channel, 10-bit	-40 to +85C -40 to +105C -40 to +125C	Nexus 2+	\$15 to \$40
768-kbyte to 1.5-Mbyte Flash, 48- to 94-kbyte SRAM,	DMA	YES	100 LQFP, 144 LQFP, 176 LQFP, 208 MAPBGA	Up to 16 channel eMIOS, 32 channel eTPU (programmable)	two eSCI, two DSPI, two CAN,	Yes	32-channel dual 12-bit (5V)	-40 to +125	IEEE-ISTO 5001-2003 standard Class 2+ (eTPU2 Class 1)	\$15
		64-entry TLB, two-way set associative	CBGA, PBGA					0 to +105		Starts at \$25
512-kbyte L2		128-entry TLB, two-way set associative	HiTCE					0 to +105	AltiVec	Starts at \$45
		128-entry TLB, two-way set associative	HCTE					-40 to +105	AltiVec	Starts at \$45
	EPROM, Flash, DRAM, SDRAM, SRAM	64-entry TLB, two-way set associative	352 TBGA	Four 16-bit or two 32-bit	I ² C, SPI, PCI, local bus			0 to +105 -40 to +105 (junction)		Starts at \$23
32-kbyte DPRAM	EDO, EPROM, Flash, DRAM, SDRAM, SRAM	64-entry TLB, two-way set associative	480 TBGA	Four 16-bit or two 32-bit, real-time	Three controllers for ATM, 10/100 Ethernet, or transparent; I ² C, two 128-channel transparent or HDLC controllers; four controllers for Ethernet, UTOPIA, HDLC, UART, transparent, or BiSync; two UART or transparent channel, SPI, PCI, local bus	Eight IRQ, 24 external sources		0 to +105 -40 to +105 (junction)	Timeslot assigner, eight TDM interfaces, transmission convergence layer for ATM, IMA, parallel I/O, eight baud rate generators, debug interface	Starts at \$33

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Freescale www.freescale.com	MPC8272 PowerQUICC II 8272, 8271, 8248, 8247	Power Architecture	266, 300, 400	64	32	1.5	1.3W	Doze, stop		Yes	16-kbyte instruction/data, four-way set- associative
Freescale www.freescale.com	MPC8280 PowerQUICC II 8280, 8275, 8270	Power Architecture	266, 333, 450	64	32	1.5	1.55W	Doze, stop		Yes	16-kbyte instruction/data, four-way set- associative
Freescale www.freescale.com	MPC8313 PowerQUICC II Pro	Power Architecture	266,333, 400	32/64	32	1.0/3.3	1.02W	Sleep, doze, power-down		Yes	16-kbyte instruction/data
Freescale www.freescale.com	MPC8315 PowerQUICC II Pro 8315, 8314	Power Architecture	266,333, 400	32/64	32	1.0/3.3	1.16W	Sleep, doze, power-down		Yes	16-kbyte instruction/data
Freescale www.freescale.com	MPC8323E PowerQUICC II Pro 8323E, 8323, 8321E, 8321	Power Architecture	266, 333	64	32	1.0	2.0W	Nap, doze, sleep			16-kbyte instruction/data, four-way set- associative with parity
Freescale www.freescale.com	MPC8349E PowerQUICC II Pro 8349E, 8347E, 8343E	Power Architecture	266, 400, 533, 667	64	32	1.2 to 1.3	4.5W	Nap, doze, sleep		Yes	32-kbyte instruction/data, eight-way set- associative with parity
Freescale www.freescale.com	MPC8360E PowerQUICC II Pro 8360E, 8358E	Power Architecture	266, 400, 533, 667	64	32	1.2 to 1.3/ 3.3 (2.5 DDR1) (1.8 DDR2)	7.0W (1.3V)	Nap, doze, sleep		Yes	32-kbyte instruction/data, eight-way set- associative with parity
Freescale www.freescale.com	MPC837xE PowerQUICC II Pro 8379E, 8378E, 8377E	Power Architecture	400, 533, 667	64	32		3.5W	Nap, doze, sleep		Yes	32-kbyte instruction/data, eight-way set- associative with parity
Freescale www.freescale.com	MPC8536 PowerQUICC III	Power Architecture	600 to 1.5GHz		32	1.0 or 1.1	6.7W	Doze, Nap, Sleep modes for dynamic power management		Double precision	32-kbyte instruction/data

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
20-kbyte DPRAM	EDO, EPROM, Flash, SDRAM, SRAM	64-entry TLB, two-way set associative	516 PBGA	Four 16-bit or two 32-bit, real-time	Two controllers for ATM, 10/100 Ethernet, or transparent; I ² C, SPI, PCI, three controllers for HDLC, UART, transparent, BiSync, or QMC; USB, two serial transparent or UART - channel	Eight IRQ, 24 external sources		0 to +105 -40 to +105 (junction)	Integrated security engine (IPsec, SSL, etc), timeslot assigner, two TDM interfaces supporting 64 HDLC channels, eight baud rate generators, debug interface	Starts at \$17
64-kbyte DPRAM	EDO, EPROM, Flash, SDRAM, SRAM	64-entry TLB, two-way set associative	480 TBGA, 516 PBGA	Four 16-bit or two 32-bit, real-time	Three controllers for ATM, 10/100 Ethernet, or transparent; two 128 channels of transparent or HDLC; four serial for Ethernet, HDLC, UART, BiSync, transparent; two serial for transparent or UART, I ² C, SPI, PCI, local bus, USB	Eight IRQ, 24 external sources		0 to +105 -40 to +105 (junction)	Timeslot assigner, eight TDM interfaces, transmission convergence layer for ATM, IMA, eight baud rate generators, debug interface	Starts at \$67
	4-channel	64-entry TLB, two-way set associative	516 TEPBGAll	periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks	2 10/100/1000 Ethernet, Hi-Speed USB, dual 32-bit/66MHz PCI, 32-bit Local Bus, DUART, dual I ² C, SPI,	5 external interrupts, internal sources		0 to +105 -40 to +105 (junction)	Security engine (IPsec, SSL), 64 multiplexed PIO, debug interface, Ethernet featuring IEEE 1588 and SGMII mode	Starts \$13.50
	4-channel	64-entry TLB, two-way set associative	620 TEPBGAll	periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks	Up to 2 10/100/1000 Ethernet, Hi-Speed USB, dual 32-bit/66MHz PCI, 32-bit Local Bus, DUART, dual I ² C, SPI, up to 2 SATA controllers, 2 x1 PCI Express	5 external interrupts, internal sources		0 to +105 -40 to +105 (junction)	Security engine (IPsec, SSL), 64 multiplexed PIO, debug interface, TDM, Ethernet featuring IEEE 1588 and SGMII mode	Starts \$17.50
	DDR-1, DDR-2 SDRAM, SDRAM, DRAM, SRAM, Flash	64-entry TLB, two-way set associative	516 PBGA	Four 16-bit or two 32-bit, real-time	Up to three 10/100 Ethernet, up to four TDM, UTOPIA, USB 2.0 (full/low speed), 32-bit PCI (up to 66MHz), 16-bit Local Bus (up to 66MHz), DUART, I ² C, (2) SPI	Eight IRQ		0 to +105 (junction)	Security engine (IPsec, SSL/TLS, SRTP, and 802.11i)	Starts at \$13
	DDR-1 SDRAM, SDRAM, DRAM, SRAM, Flash	64-entry TLB, two-way set associative	620 PBGA, 672 TBGA	Eight 16-bit or four 32 bit or two 64-bit, real-time	Two 10/100/1000 Ethernet, dual Hi-Speed USB, dual 32-bit/66MHz PCI, 32-bit Local Bus, DUART, dual I ² C, SPI	Eight IRQ, 35 external sources		0 to +105 -40 to +105 (junction)	Security engine (IPsec, SSL), 64 multiplexed PIO, debug interface	Starts at \$21
	DDR-1/2 SDRAM, SDRAM, DRAM, SRAM, Flash, 4chl DMA	64-entry TLB, two-way set associative	668 PBGA, 740 TBGA	Eight 16-bit or four 32 bit or two 64-bit, real-time	Eight 10/100, two 10/100/1000, two UTOPIA for ATM/POS, eight TDM, USB, and 2xSPI; single 32-bit PCI, dual I ² C, DUART, Local Bus	Eight IRQ		0 to +105 -40 to +105 (junction)	Security engine (IPsec, SSL), IEEE1588 time synchronization protocol	Starts at \$27
	DDR-2 DDR-1 SDRAM, SDRAM, DRAM, SRAM, Flash	64-entry TLB, two-way set associative	689 TePBGA		Two 10/100/1000 Ethernet, Hi-Speed USB, dual 32-bit/66MHz PCI, 32-bit Local Bus, DUART, dual I ² C, SPI, up to 4 SATA controllers, 2 x1 PCI Express			0 to +125 -40 to +125 (junction)	Security engine (IPsec, SSL), 64 multiplexed PIO, debug interface	Starts at \$27
512-kbyte L2	DDR2/3 up to 667MHz, 4-channel DMA	4-Kbyte to 4-Gbyte page sizes.	783 FC PBGA	watchdog timer, performance monitor timers, Four global high resolution timers	2 Gb Ethernet controllers (SGMII, RGMII, RTB, MII), SPI, 2x I ² C, DUART, PCI, triple PCIe, dual SATA	Supports 12 discrete external interrupts, 4 message interrupts with 32-bit messages	64-bit dual address cycle (DAC) support	0 to +105	Advanced Power Management	Starts at \$63

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Freescale www.freescale.com	MPC8540 PowerQUICC III	Power Architecture	667 to 1000	64/64	32	1.2	7.4W	Doze, nap, sleep		Yes	32-kbyte instruction/data, L2: 256-kbyte unified
Freescale www.freescale.com	MPC8541 PowerQUICC III	Power Architecture	533 to 1000	32	32	1.2	5.4W	Doze, nap, sleep		Yes	32-kbyte instruction/data, L2: 256-kbyte unified
Freescale www.freescale.com	MPC8548 PowerQUICC III 8548, 8547, 8545, 8543	Power Architecture	800 to 1333	64/64	32	1.2		Doze, nap, sleep		Yes	32-kbyte instruction/data, L2: 512-Kbyte unified
Freescale www.freescale.com	MPC8555 PowerQUICC III	Power Architecture	533 to 1000	32	32	1.2	5.4W	Doze, nap, sleep		Yes	32-kbyte instruction/data, L2: 256-kbyte unified
Freescale www.freescale.com	MPC8572 Dual Core PowerQUICC III	Power Architecture	1067 to 1500	64/64	32	1.1, 1.8, 1.5, 3.3, 2.5	17.3W	Doze, nap, sleep		Yes	32-kbyte instruction/data, L2: 1 Mbyte unified shared between cores
Freescale www.freescale.com	MPC8610	Power Architecture	667 to 1333	36/64 (internal)	32	1.0/1.25; 1.8/2.5/3.3	10W	Nap, sleep	128-bit Altivec vector processor (per core)	IEEE 754-1985 single and double precision (per core)	32-kbyte instruction/data eight-way set-associative (per core), L2: 1-Mbyte eight-way set-associative with ECC
Freescale www.freescale.com	MPC862 PowerQUICC I 862P, 862T, 857T, 857DSL	Power Architecture	50, 66, 80, 100	32	32	3.3/5	1.35W	Sleep, doze, power-down	16x16 MAC		4- to 16-kbyte instruction, 4- to 8-kbyte data

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
64-kbyte DPRAM	DDR-1 SDRAM, SDRAM, DRAM, SRAM, Flash	64-entry TLB, four-way set-associative, L2: 16-entry TLB, fully associative, 256-entry TLB, two-way set-associative	783 FCBGA	Four 16-bit or two 32-bit, real-time	Two 10/100/1000 Ethernet, DUART, Local Bus PCI/PCI-X), 8 (RapidIO)	16 programmable, 16 levels, 12 external, 4 message, 22 other internal sources		-40 to +105 (junction)	e500 core, hardware coherency, four baud rate generators, debug interface	Starts at \$85
64-kbyte DPRAM	DDR-1 SDRAM, SDRAM, DRAM, SRAM, Flash	64-entry TLB, four-way set-associative, L2: 256-entry TLB, two-way set-associative, 16-entry TLB, fully associative	783 FCBGA	Four 16-bit or two 32-bit, real-time	Two 10/100 and two 10/100/1000 Ethernet, ATM, transparent; QMCI; USB, three serial for UART, BISYNC, HDLC, transparent; two serial for UART; I ² C, SPI, Local Bus PCI, 32/64 (PCI)	16 programmable, 16 levels, 12 external, 4 message, 22 other internal sources		-40 to +105 (junction)	e500 core, hardware coherency, security engine (IPsec, SSL), time slot assigner, three TDM interfaces, four baud rate generators, debug interface	Starts at \$66
64-kbyte DPRAM	DDR-1/2 SDRAM, SDRAM, DRAM, SRAM, Flash	64-entry TLB, four-way set-associative, L2: 256-entry TLB, two-way set-associative, 16-entry TLB, fully associative	783 FCBGA	Four 16-bit or two 32-bit	Four 10/100/1000 Ethernet, DUART, Dual I ² C, two 32-bit PCI, PCI-Express, local bus, GPIO, 10/100 Ethernet, SRIO, Local Bus PCI/PCI-X, 8 (RapidIO)	16 programmable, 16 levels, 12 external, 4 message, 22 other internal sources		-40 to +105 (junction)	e500 core, hardware coherency, security engine (IPsec, SSL, XOR)	Starts at \$62
64-kbyte DPRAM	DDR-1 SDRAM, SDRAM, DRAM, SRAM, Flash	64-entry TLB, four-way set-associative, L2: 256-entry TLB, two-way set-associative, 16-entry TLB, fully associative	783 FCBGA	Four 16-bit or two 32-bit, real-time	Two 10/100 and two 10/100/1000 Ethernet, ATM, transparent; QMCI; USB, three serial for Ethernet, HDLC, UART, BISYNC, transparent; two serial for UART; I ² C, SPI, Local Bus PCI, 32/64 (PCI)	16 programmable, 16 levels, 12 external, 4 message, 22 other internal sources		-40 to +105 (junction)	e500 core, hardware coherency, security engine (IPsec, SSL), time slot assigner, three TDM interfaces, four baud rate generators, debug interface	Starts at \$94
1-Mbyte L2 can be used as SRAM	Dual 64b DDR-2/3 to 800MHz with ECC; DRAM, SRAM, NAND and NOR Flash; dual 4-channel DMA controller	64-entry TLB, four-way set-associative, L2: 256-entry TLB, two-way set-associative, 16-entry TLB, fully associative (per core)	1023 FC-PBGA	Eight 32-bit timers	Four 10/100/1000 Ethernet with SGMII, one 10/100 Ethernet, local bus, x8 SerDes for 3 PCI Express or one SRIO,	16 levels, 12 external, 16 message, 8 inter-processor, 64 other internal sources		0 to +125 -40 to +125 (junction)	e500 core, hardware coherency, security engine (IPsec, SSL, XOR), pattern matching engine, table lookup engine	Starts at \$157
256-kbyte of L2	4-channel DMA; single 64 bit DDR2 with ECC and 32-Gbyte range	Separate 128-entry TLB for instruction and data (per core), hardware reload, two-way set associative; 8 block address translations for both instruction and data	Flip Chip - Plastic BGA, 29x29mm, 783 pin, in either lead or lead-free.	Watch dog and 2-global timers	32-bit local bus; DUART, 2 I2S/AC97 audio ports, 2 - Fast/Serial IrDa channels.,	12 external, 48 internal, interprocess and messaging		0 to +105 -40 to +105	x8 and x4 PCI Express; LCD Controller, PCI 2.2 ,	Starts at \$75
8-kbyte DPRAM	EDO, EPROM, Flash, DRAM, SDRAM, SRAM	32-entry TLB, fully associative	357 PBGA	Four 16-bit or two 32-bit	10/100 Ethernet, four serial for Ethernet, UTOPIA, HDLC, Async HDLC, UART, BiSync, transparent; two serial for UART, transparent; I ² C, SPI, PCMCIA	Eight IRQ, 12 port pins, 23 internal sources		0 to +105 -40 to +115 (junction)	Timeslot assigner, four baud rate generators, debug interface	Starts at \$18

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Freescale www.freescale.com	MPC8640	Power Architecture	1000 to 1250	36/64 (internal)	32	0.95/1.05/1.1; 1.8/2.5/3.3	13.0W	Nap, sleep	128-bit Altivec vector processor	IEEE 754-1985 single and double precision	32-kbyte instruction/data, eight-way set-associative, L2: 1-Mbyte eight-way set associative with ECC
Freescale www.freescale.com	MPC8640D	Power Architecture	1000 to 1250 two cores	36/64 (internal)	32	0.95/1.05/1.1; 1.8/2.5/3.3	21W	Nap, sleep	128-bit Altivec vector processor (per core)	IEEE 754-1985 single and double precision (per core)	32-kbyte instruction/data eight-way set-associative (per core), L2: 1-Mbyte eight-way set-associative with ECC
Freescale www.freescale.com	MPC8641	Power Architecture	1000 to 1333	36/64 (internal)	32	0.95/1.05/1.1; 1.8/2.5/3.3	16.3W	Nap, sleep	128-bit Altivec vector processor	IEEE 754-1985 single and double precision	32-kbyte instruction/data, eight-way set-associative, L2: 1-Mbyte eight-way set associative with ECC
Freescale www.freescale.com	MPC8641D	Power Architecture	1000 to 1500 two cores	36/64 (internal)	32	0.95/1.05/1.1; 1.8/2.5/3.3	32.1W	Nap, sleep	128-bit Altivec vector processor (per core)	IEEE 754-1985 single and double precision (per core)	32-kbyte instruction/data eight-way set-associative (per core), L2: 1-Mbyte eight-way set-associative with ECC
Freescale www.freescale.com	MPC866 PowerQUICC I 866P, 866T, 852T, 859T, 859DSL	Power Architecture	50, 66, 80, 100, 133	32	32	1.8/3.3	0.26W	Normal low	16x16 MAC		4- to 16-kbyte instruction, 4- to 8-kbyte data
Freescale www.freescale.com	MPC885 PowerQUICC I 885, 880, 875, 870	Power Architecture	66, 80, 133	32	32	1.8/3.3	0.43W	Normal low	16x16 MAC		8-kbyte instruction/data

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
1-Mbyte of L2	4-channel DMA; dual 64-bit DDR2 with ECC and 32-Gbyte range	Separate 128-entry TLB for instruction and data, hardware reload, two-way set associative; 8 block address translations for both instruction and data	HiTCE, 33x33mm, 1023 pin, in either lead or lead-free.	8 global	32-bit local bus; DUART	12 external, 48 internal		0 to +105 -40 to +105	Dual x8 PCI Express; Quad 10/100/1000 Ethernet controllers with TCP/UDP offload and quality of service features.	Starts at \$125
1-Mbyte of L2 per core	4-channel DMA; dual 64-bit DDR2 with ECC and 32-Gbyte range	Separate 128-entry TLB for instruction and data (per core), hardware reload, two-way set associative; 8 block address translations for both instruction and data	HiTCE, 33x33mm, 1023 pin, in either lead or lead-free.	8 global	32-bit local bus; DUART	12 external, 48 internal, interprocess and messaging		0 to +105 -40 to +105	Dual core; Dual x8 PCI Express; Quad 10/100/1000 Ethernet controllers with TCP/UDP offload and quality of service features	Starts at \$95
	4-channel DMA; dual 64-bit DDR2 with ECC and 32-Gbyte range	Separate 128-entry TLB for instruction and data, hardware reload, two-way set associative; 8 block address translations for both instruction and data	HiTCE, 33x33mm, 1023 pin, in either lead or lead-free.	8 global	32-bit local bus; DUART	12 external, 48 internal		0 to +105 -40 to 105 (industrial)	Dual x8 PCI Express; Quad 10/100/1000 Ethernet controllers with TCP/UDP offload and quality of service features.	Starts at \$237
	4-channel DMA; dual 64-bit DDR2 with ECC and 32-Gbyte range	Separate 128-entry TLB for instruction and data (per core), hardware reload, two-way set associative; 8 block address translations for both instruction and data	HiTCE, 33x33mm, 1023 pin, in either lead or lead-free.	8 global	32-bit local bus; DUART	12 external, 48 internal, interprocess and messaging		0 to +105	Dual core; Dual x8 PCI Express; Quad 10/100/1000 Ethernet controllers with TCP/UDP offload and quality of service features	Starts at \$264
8-kbyte DPRAM	EDO, EPROM, Flash, DRAM, SDRAM, SRAM	32-entry TLB, fully associative	256/357 PBGA	Four 16-bit or two 32-bit	10/100 Ethernet, four serial for Ethernet, UTOPIA, HDLC, Async HDLC, UART, BiSync, transparent; two serial for UART, transparent; I ² C, SPI, PCMCIA	Eight IRQ, 12 port pins, 23 internal sources		0 to +95 -40 to +100 (junction)	Timeslot assigner, four baud rate generators, debug interface	Starts at \$7
8-kbyte DPRAM	EDO, EPROM, Flash, DRAM, SDRAM, SRAM	32-entry TLB, fully associative	256/357 PBGA	Four 16-bit or two 32-bit	USB, two 10/100 Ethernet, three serial for Ethernet, UTOPIA, HDLC, Async HDLC, UART, BiSync, transparent; two serial for UART, transparent; I ² C, SPI, PCMCIA	Six IRQ, 12 port pins, 23 internal sources		0 to +95 -40 to +100 (junction)	Security engine (IPsec, SSL), time slot assigner, four baud rate generators, debug interface	Starts at \$7

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Freescale www.freescale.com	QorIQ P1, dual core P1020	Power Architecture	533 to 800	64/64	32			Doze, nap, sleep		Yes	32-kbyte instruction/data, L2: 512kB unified shared between cores
Freescale www.freescale.com	QorIQ P1, single core P1010	Power Architecture	400 to 667	64/64	32			Doze, nap, sleep		Yes	32-kbyte instruction/data, L2: 512kB unified shared between cores
Freescale www.freescale.com	QorIQ P1, single core P1011	Power Architecture	533 to 800	64/64	32			Doze, nap, sleep		Yes	32-kbyte instruction/data, L2: 512kB unified shared between cores
Freescale www.freescale.com	QorIQ P2, dual core P2020	Power Architecture	800 to 1200	64/64	32			Doze, nap, sleep		Yes	32-kbyte instruction/data, L2: 512kB unified shared between cores
Freescale www.freescale.com	QorIQ P2, single core P2010	Power Architecture	800 to 1200	64/64	32			Doze, nap, sleep		Yes	32-kbyte instruction/data, L2: 512kB unified shared between cores
Freescale www.freescale.com	QorIQ P4, eight core P4080	Power Architecture	1200 to 1500 eight cores	36/128 Internal CoreNet	32	0.9, 1.0, 1.1/ 1.8, 2.5, 3.3	24W	Sleep, Nap, Doze, fine-grained static power management, dynamic changes to CPU operating frequencies and voltages		IEEE 754-1985 single and double precision (per core)	32-kbyte instruction/data 8-way set-associative, L2: 128 kbyte 8-way set-associative with ECC backside; L3: 2 Mbyte 32-way set associative with ECC frontside shared CoreNet Platform Cache
Fujitsu Microelectronics America us.fujitsu.com/micro	FR30	FR	25 to 50, 32.768 kHz	32/32, external: 24/16	16	2.3 to 5.5	270 mW	Sleep, stop, sub clock mode, timer	32x32 DSP macro with barrel shifter and bit search		Up to 4-kbyte instruction

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
256-kbyte L2 can be used as SRAM	32b DDR-2/3 with ECC; DRAM, SD/MMC, SRAM, NAND and NOR Flash; dual channel DMA controller	64-entry TLB, four-way set-associative, L2; 256-entry TLB, two-way set-associative, 16-entry TLB, fully associative (per core)	689-in wirebond TEPBGA2	Eight 32-bit timers	Three 10/100/1000 with SGMII, x4 SerDes for 2 PCI Express, 2 SRIO, and 2 SGMII; 2 USB2.0; local bus; SPI	16 levels, 12 external, 16 message, 8 inter-processor, 64 other internal sources		0 to +125 -40 to +125 (junction)	e500 core, hardware coherency, security engine (Ipsec, SSL, XOR)	
	32b DDR-2/3 with ECC; DRAM, SD/MMC, SRAM, NAND and NOR Flash; dual 4-channel DMA controller	64-entry TLB, four-way set-associative, L2; 256-entry TLB, two-way set-associative, 16-entry TLB, fully associative	689-in wirebond TEPBGA2	Eight 32-bit timers	Three 10/100/1000 with SGMII, x4 SerDes for 2 PCI Express, 2 SRIO, and 2 SGMII; 2 USB2.0; local bus; SPI	16 levels, 12 external, 16 message, 64 other internal sources		0 to +125 -40 to +125 (junction)	e500 core, hardware coherency, security engine (Ipsec, SSL, XOR)	
256-kbyte L2 can be used as SRAM	32b DDR-2/3 with ECC; DRAM, SD/MMC, SRAM, NAND and NOR Flash; dual 4-channel DMA controller	64-entry TLB, four-way set-associative, L2; 256-entry TLB, two-way set-associative, 16-entry TLB, fully associative	689-in wirebond TEPBGA2	Eight 32-bit timers	Three 10/100/1000 with SGMII, x4 SerDes for 2 PCI Express, 2 SRIO, and 2 SGMII; 2 USB2.0; local bus; SPI	16 levels, 12 external, 16 message, 64 other internal sources		0 to +125 -40 to +125 (junction)	e500 core, hardware coherency, security engine (Ipsec, SSL, XOR)	
512-kbyte L2 can be used as SRAM	64b DDR-2/3 with ECC; DRAM, SD/MMC, SRAM, NAND and NOR Flash; dual 4-channel DMA controller	64-entry TLB, four-way set-associative, L2; 256-entry TLB, two-way set-associative, 16-entry TLB, fully associative (per core)	689-in wirebond TEPBGA2	Eight 32-bit timers	Three 10/100/1000 with SGMII, x4 SerDes for 3 PCI Express, 2 SRIO, and 2 SGMII; USB2.0; local bus; SPI	16 levels, 12 external, 16 message, 8 interprocessor, 64 other internal sources		0 to +125 -40 to +125 (junction)	e500 core, hardware coherency, security engine (Ipsec, SSL, XOR)	
512-kbyte L2 can be used as SRAM	64b DDR-2/3 with ECC; DRAM, SD/MMC, SRAM, NAND and NOR Flash; dual 4-channel DMA controller	64-entry TLB, four-way set-associative, L2; 256-entry TLB, two-way set-associative, 16-entry TLB, fully associative	689-in wirebond TEPBGA2	Eight 32-bit timers	Three 10/100/1000 with SGMII, x4 SerDes for 3 PCI Express, 2 SRIO, and 2 SGMII; USB2.0; local bus; SPI	16 levels, 12 external, 16 message, 64 other internal sources		0 to +125 -40 to +125 (junction)	e500 core, hardware coherency, security engine (Ipsec, SSL, XOR)	
External dual 16-Gbyte DDR2/DDR3, Flash		64 TLB with 512-entry 4K pages for instruction/data (per core), hardware reload, 8-way set associative; 8 block address translations for instruction/data	FC-BGA, 1295 pin	Eight 32-bit timers	Eight 10/100/1000 Ethernet with SGMII, two 10GbE with XAUI, two parallel 10/100/1000 Ethernets, enhanced local bus, SerDes for 3 PCI Express v2.0 or two Serial Rapid IO controllers, up to 18 SerDes 5GHz	12 external, 48 internal, interprocess and messaging		0 to +105	e500mc cores; Decorated Storage APU, CoreNet coherency fabric, embedded Hypervisor, Frame/Queue/Buffer Managers, security (IPSec, SSL, XOR), RegEx pattern matching, debug via SerDes based Aroua or JTAG, DUARTs, 4x I2C, 2x USB with ULPI	
Up to 512-kbyte Flash, up to 160-kbyte SRAM	DRAM, DMAC		100/120/144/160 QFP/LQFP	16-bit reload, free running, PWC, timebase, PPG, PWM	SIO, CAN, UART, I ² C, up to 120 PIO	Up to 24 external	Four-, eight-, or 16-channel, 8/10-bit; three-channel, 8-bit DAC	0 to +70 -40 to +85	Comparator, input capture, output compare	From \$5

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Fujitsu Microelectronics America us.fujitsu.com/micro	FR50	FR	32 to 64, 32.768 kHz	32/32, external: 24/16	16	2.3 to 5.5	300 mW	Sleep, stop, sub clock mode, timer	32x32 with barrel shifter and bit search		Up to 4-kbyte instruction
Fujitsu Microelectronics America us.fujitsu.com/micro	FR60	FR	50 to 68, 32.768 kHz	32/32, external: 24/16	16	2.3 to 5.5	450 mW	Sleep, stop, sub clock mode, timer	32x32 with barrel shifter and bit search		Up to 4-kbyte instruction
Fujitsu Microelectronics America us.fujitsu.com/micro	FR60lite	FR	33	32/32, external: 24/16	16	3 to 5.5	250 mW	Sleep, stop, sub clock mode, timer	32x32 with barrel shifter and bit search		Up to 4-kbyte instruction
Fujitsu Microelectronics America us.fujitsu.com/micro	FR-ASSP	FR	30 to 50	32/32, external: 24/16	16	3	200 mW	Sleep, stop, sub clock mode, timer	32x32 with barrel shifter and bit search		Up to 4-kbyte instruction
GainSpan Corporation www.gainspan.com	GS1010	ARM7	44	Internal: 32	32	1.8 / 1.8, 2.5, 3.3	40 mW	5 uA (3.6V) 2 uA (1.8V)	Yes		
Hyperstone www.hyperstone.com	hyNet S	E1-32XSR RISC	up to 180	26/32	Variable 16, 32, 48	1.8/3.3	1.0W	Powerdown, sleep, doze	32x32 16x16	Software instructions	2-kbyte instruction/data
Hyperstone www.hyperstone.com	hyNet XS	E1-32XSR RISC	up to 180	26/32	Variable 16, 32, 48	1.8/3.3	1.7W	Powerdown, sleep, doze	32x32 16x16	Software instructions	2-kbyte instruction/data
Hyperstone www.hyperstone.com	E1-32XSR (E1-16XSR)	RISC	up to 120	26/32 (22/16)	Variable 16, 32, 48	2.5/3.3	40 mA	Powerdown, sleep	32x32 16x16	Software instructions	128-byte instruction
Hyperstone www.hyperstone.com	F3 CF/PATA NAND Flash Controller	E1-32XSR RISC	up to 70	NAND Flash Interface	Variable 16, 32, 48	2.5/3.3, 5.0	50 mA	Automatic powerdown			128-byte instruction
Hyperstone www.hyperstone.com	F4 CF/PATA NAND Flash Controller	E1-32XSR RISC	up to 70	NAND Flash Interface	Variable 16, 32, 48	2.5/3.3, 5.0	50 mA	Automatic powerdown			128-byte instruction
Hyperstone www.hyperstone.com	S6 SD/MMC NAND Flash Controller	E1-32XSR RISC	up to 60	NAND Flash Interface SD/MMC Interface	Variable 16, 32, 48	1.8/1.65 to 3.6	40	Sleep			128-byte instruction
Hyperstone www.hyperstone.com	S7B SD/MMC NAND Flash Controller	E1-32XSR RISC	up to 60	NAND Flash Interface SD/MMC Interface	Variable 16, 32, 48	1.8/1.65 to 3.6	40	Sleep			128-byte instruction
IBM ibm.com/technology	PowerPC 405 embedded core	Power Architecture	366 to 400 (worst case)	64/128	32	1.1 (90 nm)	0.12 mW/MHz	Yes	DSP instructions		16-kbyte instruction/data with parity

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
Up to 784-kbyte Flash, up to 36-kbyte SRAM	DMAC		120/208 QFP, LQFP	16-bit reload, free running, PWC, timebase, PPG, PWM	SIO, CAN, LIN, UART, I ² C	Up to 24 external	Eight- or 16-channel, 8/10-bit; three-channel, 8-bit DAC	-40 to +85	Input capture, output compare, sound generator, stepper motor, comparator	From \$6
Up to 1-Mbyte Flash, up to 512-kbyte font Flash, up to 160-kbyte SRAM	SDRAM, DMAC, USB, Memory stick		100/120/144/176 LQFP, QFP	16-bit reload, free running, PWC, timebase, PPG, PWM	SIO, CAN, LIN, UART, I ² C	Up to 24 external	Eight- or 16-channel, 8/10-bit; 8-bit DAC	0 to +70 -40 to +85	Comparator, input capture, output compare, OSDC, CCD, ac/dc inverter control, FlexRay	From \$6
Up to 512-kbyte Flash, up to 16-kbyte SRAM	DMAC		100/120/144 LQFP/QFP	16-bit reload, free running, PWC, timebase, PPG, PWM	SIO, CAN, LIN-UART, I ² C	Up to 24 external	Eight- or 16-channel 8/10-bit, 8-bit DAC	0 to +70 -40 to +85	Embedded LCDC, CAN, stepper Motor, LIN-UART, input capture, output compare	From \$4.25
Up to 256-kbyte Flash, up to 64-kbyte SRAM	DMAC		144 LQFP/QFP, 240 FBGA	16-bit reload, free running, timebase, PPG	10/100 Ethernet, SIO, UART, I ² C, USB	Up to 24 external	Eight- or 16-channel, 8/10-bit; 8-bit DAC	-10 to +70 -40 to +85	Authentication hardware accelerator (IPV4/IPV6 with DES/3DES/AES)	\$10 to \$20
224-kbyte SRAM, 384-kbyte Flash	Integrated	Internal	102 QFN	2 16-bit timers, 3 PWM, 48-bit RTC, 3 34-bit wakeup counters	SPI, 2 UART, 3 PWM, I ² C, 2 ADC, 32 GPIO, JTAG, 802.11, RTC	Any GPIO can be an interrupt	2 external ADC inputs, internal battery voltage + temperature, 10 bit, 32Ksps	-40 to +85	802.11b/g radio, 2 ARM7 TDMI, integrated power amplifier, also supports external power amplifier + Tx/Rx switch	
16-kbyte RAM, 64-kbyte SRAM, 16-kbyte shared SRAM, 8-kbyte boot ROM	SDRAM, SRAM, FLASH, 6 channel DMA	64-entry TLB, 32 instruction, 32 data	256 TFBGA	32-bit, watchdog, realtime	10/100 Ethernet Up to 58 GPIO Configurable serial controller with 16 pins	Four external, internal sources, NMI		0 to +85	PCI Bus Interface with arbiter, DCT Co-Processor, Built in Ethernet Repeating Hub, PI Interface, IEEE 1588 Clock synchronization Core	\$11.83
16-kbyte RAM, 128-kbyte SRAM, 32-kbyte shared SRAM, 8-kbyte boot ROM	SDRAM, SRAM, FLASH	64-entry TLB, 32 instruction, 32 data	256 TFBGA	32-bit, watchdog, realtime	Two 10/100 Ethernet and PHY, USB 2.0 OTG CAN Up to 58 GPIO Configurable serial controller with 16 pins	Four external, internal sources, NMI		0 to +85	PCM Interface, 6 Channel DMA, Utopia Level 2, IEEE 1588 Clock Synchronization Core	\$19.63
16-kbyte SRAM	SDRAM, SRAM, FLASH		144(100) LQFP	32-bit, watchdog	Three GPIO	Four external		0 to +85		\$5.40 (\$4.95)
20-kbyte SRAM, 8-kbyte boot ROM	NAND FLASH All Vendors		100 TQFP, 128 LQFP,	32-bit, watchdog				0 to +85	CF/PATA interface, Core/Flash Voltage Regulator Built in, Bootable Firmware Stored in Flash, 2x 512Byte sector buffers per channel, 4 symbol Reed-Solomon ECC.	\$3.12
20-kbyte SRAM, 8-kbyte boot ROM	NAND FLASH All Vendors		100 TQFP, 128 LQFP,	32-bit, watchdog				0 to +85	CF/PATA interface, Core/Flash Voltage Regulator Built in, Bootable Firmware Stored in Flash, 2x 4kByte sector buffers per channel, 4 symbol Reed-Solomon ECC.	
20-kbyte SRAM, 16-kbyte boot ROM	NAND FLASH All Vendors		50 LGA 128 LQFP	32-bit, watchdog				0 to +85	SD2.0/MMC4.2 Interface, Dual Voltage Mode, Bootable firmware stored in flash, 2x 4kByte sector buffers per channel, 4 symbol Reed-Solomon ECC.	\$2.34
20-kbyte SRAM, 16-kbyte boot ROM	NAND FLASH All Vendors		50 LGA 128 LQFP	32-bit, watchdog				0 to +85	SD2.0/MMC4.3 Interface, Dual Voltage Mode, Bootable firmware stored in flash, 2x 4kByte sector buffers per channel, 6/14bit BCH ECC.	TBD
Licensee option	Licensee option	64-entry UTLB, 4-entry ITLB, 8-entry DTLB	IP Core	64-bit time base, programmable interval timer, fixed interval timer, watchdog timer	Licensee option			-40 to +105	Scalar, 5-stage pipeline	License

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
IBM ibm.com/technology	PowerPC 440 embedded core	Power Architecture	533 to 667 (worst case)	128	32	1.1 (90 nm)	1 W/MHz	Yes	DSP instructions	Yes, optional	32-kbyte instruction/data with parity
IBM ibm.com/technology	PowerPC 750Cxr	Power Architecture	300 to 533	32/ 32 and 64	64	1.7 to 1.95/ 1.8, 2.5	7.8W (533 MHz)	Nap, doze, sleep		Yes	32-kbyte instruction/data, eight-way set associative
IBM ibm.com/technology	PowerPC 750FL	Power Architecture	600 to 733	32/ 32 and 64	64	1.3 to 1.5/ 1.8, 2.5, 3.3	5.1W (733 MHz)	Nap, doze, sleep		Yes	32-kbyte instruction/data, eight-way set associative
IBM ibm.com/technology	PowerPC 750FX	Power Architecture	600 to 800	32/ 32 and 64	64	1.2 to 1.5/ 1.8, 2.5, 3.3	6.0W (800 MHz)	Nap, doze, sleep		Yes	32-kbyte instruction/data, eight-way set associative
IBM ibm.com/technology	PowerPC 750GL	Power Architecture	800 to 933	32/ 32 and 64	64	1.2 to 1.55/ 1.8, 2.5, 3.3	6.5W (933 MHz)	Nap, doze, sleep		Yes	32-kbyte instruction/data, eight-way set associative
IBM ibm.com/technology	PowerPC 750GX	Power Architecture	933 to 1000	32/ 32 and 64	64	1.4 to 1.55/ 1.8, 2.5, 3.3	8.3W (1 GHz)	Nap, doze, sleep		Yes	32-kbyte instruction/data, eight-way set associative
IDT www.idt.com	RC32332	MIPS II	100, 133, 150	23/32	32	2.5/3.3 or 3.3/3/3	0.95 or 1.7W	Wait	32x32		8/2-kbyte instruction/data, two-way set associative
IDT www.idt.com	RC32333	MIPS II	100, 133, 150	23/32	32	2.5/3.3 or 3.3/3/3	0.95 or 1.7W	Wait	32x32		8/2-kbyte instruction/data, two-way set associative
IDT www.idt.com	RC32334	MIPS II	100, 133, 150	26/32	32	3.3/3.3	1.7W	Wait	32x32		8/2-kbyte instruction/data, two-way set associative
IDT www.idt.com	RC32336	MIPS II	150	22/32	32	2.5/3.3	2.38W	Wait	32x32		8/2-kbyte instruction/data, two-way set associative
IDT www.idt.com	RC32351	MIPS II	100, 133	26/32	32	2.5/3.3	1.26W	Wait	32x32		8/2-kbyte instruction/data, two-way set associative
IDT www.idt.com	RC32355	MIPS II	133, 150, 180	26/32	32	2.5/3.3	1.73W	Wait	32x32		8/2-kbyte instruction/data, two-way set associative
IDT www.idt.com	RC32365	MIPS II	150	22/32	32	2.5/3.3	2.38W	Wait	32x32		8/2-kbyte instruction/data, two-way set associative
IDT www.idt.com	RC32434	MIPS32	266, 300, 350, 400	26/8	32	1.2/3.3	1.54W	Wait	32x32		8-kbyte instruction/data, four-way set associative
IDT www.idt.com	RC32438	MIPS32	200, 233, 266	26/16	32	1.2/3.3	2.0W	Wait	32x32		16-kbyte instruction/data, four-way set associative

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
Licensee option	Licensee option	64-entry UTLB, 4-entry ITLB, 8-entry DTLB	IP Core	64-bit time base, 32-bit programmable interval timer, fixed interval timer, watchdog timer	Licensee option			-40 to +105	Dual issue, superscalar, 7 stage pipeline	License
256-kbyte L2		128-entry TLB, 2-way set associative	256 PBGA, 27 mm					0 to +95		
512-kbyte L2		64-entry TLB, 2-way set associative	292 CBGA, 21 mm					-40 to +105		
512-kbyte L2		64-entry TLB, 2-way set associative	292 CBGA, 21 mm					-40 to +105		
1-Mbyte L2		64-entry TLB, 2-way set associative	292 CBGA, 21 mm					-40 to +105		
1-Mbyte L2		64-entry TLB, 2-way set associative	292 CBGA, 21 mm					-40 to +105		
	32-bit SDRAM, 8-, 16-, 32-bit SRAM, Flash, ROM, dual-port	32-entry TLB	208 QFP	Four 32-bit	UART (16550-compatible), v2.1 PCI 32-bits, eight PIO	Four, more via PIO		-40 to +85 0 to +70 (case)	EJTAG debug	\$10 to \$15.25
	32-bit SDRAM, 8-, 16-, 32-bit SRAM, Flash, ROM, dual-port	32-entry TLB	208 QFP	Four 32-bit	UART (16550-compatible), v2.1 PCI 32-bits, eight PIO	Four, more via PIO		-40 to +85 0 to +70 (case)	EJTAG debug	\$10 to \$15.25
	32-bit SDRAM, 8-, 16-, 32-bit SRAM, Flash, ROM, dual-port	32-entry TLB	256 PBGA	Four 32-bit	Dual UART (16550 compatible), v2.1 PCI bridge, 16 PIO	Four, more via PIO		-40 to +85 0 to +70 (case)	EJTAG debug	\$15 to \$19.25
	32-bit SDRAM, 8-, 16-, 32-bit SRAM, Flash, ROM, dual-port, six-channel DMA	16-entry TLB	256 CABGA	Three 32-bit	UART (16550-compatible), SPI, 16 GPIO, v2.2 PCI 32-bits, v2.1 PCMCIA, two 10/100 Ethernet	Four, more via PIO		0 to +70	EJTAG debug	\$15
	32-bit SDRAM, 8-, 16-, 32-bit SRAM, Flash, ROM, dual-port	16-entry TLB	208 QFP	Three 32-bit	Two UART (16550-compatible), USB 1.1, ATM (Utopia1/2), 10/100 Ethernet, 32 PIO	Four, more via PIO		0 to +70	EJTAG debug	\$15 to \$15.75
	32-bit SDRAM, 8-, 16-, 32-bit SRAM, Flash, ROM, dual-port	16-entry TLB	208 QFP	Three 32-bit	Two UART (16550-compatible), USB 1.1, I ² C, TDM, ATM (Utopia1/2), 10/100 Ethernet, 32 PIO	Four, more via PIO		-40 to +85 0 to +70 (case)	EJTAG debug	\$17.50 to \$20.90
	32-bit SDRAM, 8-, 16-, 32-bit SRAM, Flash, ROM, dual-port, six-channel DMA	16-entry TLB	256 CABGA	Three 32-bit	UART (16550-compatible), I ² C, SPI, 16 GPIO, v2.2 PCI 32-bits, v2.1 PCMCIA, two 10/100 Ethernet	Four, more via PIO		-40 to +85 0 to +70 (case)	Hardware IPsec acceleration (DES, 3DES, AES), random number generator, EJTAG debug	\$15 to \$16
	16-bit DDR, 8-bit SRAM, ROM, Flash, dual-port	16-dual-entry TLB	256 CABGA	Three 32-bit	UART (16550-compatible), I ² C, SPI, 10/100 Ethernet, v2.2 PCI 32-bit, 14 GPIO	Four, more via PIO		-40 to +85 0 to +70 (case)	Enhanced JTAG and ICE interfaces, authentication unit with NVRAM.	\$15.50 to \$23
	16-, 32-bit DDR, 8-, 16-bit SRAM, ROM, Flash, dual-port	16-dual-entry TLB	416 BGA	Three 32-bit	Dual UART (16550-compatible), I ² C, SPI, two 10/100 Ethernet, v2.2 PCI 32-bit, 32 GPIO	Four, more via PIO		-40 to +85 0 to +70 (case)	Enhanced JTAG and ICE interfaces, bus-monitor logic	\$25 to \$35

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Imsys Technologies www.imsystech.com	IM3200	IM3k	133, 167, 200	8, up to 83 external	Variable multiple of 8 (8, 16, 24, 32, ...)	1.8/3.3	50 mW (core), 105 mW (core + Ethernet)	Stand-by 1mW, 2.5uA (RTC only)	8x8, MAC with 24-bit accumulate; 32/64bit mul/div (microcode)	IEEE-754-compliant, single/double-precision (microcode)	Two 256-byte stack caches
Imsys Technologies www.imsystech.com	IM3900	IM3k	133, 167, 200	8, up to 83 external	Variable multiple of 8 (8, 16, 24, 32, ...)	1.8/3.3	50 mW (core), 105 mW (core + Ethernet)	Stand-by 1mW, 2.5uA (RTC only)	8x8, MAC with 24-bit accumulate; 32/64bit mul/div (microcode)	IEEE-754-compliant, single/double-precision (microcode)	Two 256-byte stack caches
Infineon Technologies www.infineon.com/microcontrollers	TC1115	TriCore v1.3	150	32/16/8	16, 32	1.5/3.3	744 mW	3 mW, idle, sleep, deep sleep	Dual MAC, bit-reverse, signed-fraction, modulo, saturation, pre/post-increment, rounding	Single-precision	16/4-kbyte instruction/data
Infineon Technologies www.infineon.com/microcontrollers	TC1130	TriCore v1.3	150	32/16/8	16, 32	1.5/3.3	744 mW	3 mW, idle, sleep, deep sleep	Dual MAC, bit-reverse, signed-fraction, modulo, saturation, pre/post-increment, rounding	Single-precision	16/4-kbyte instruction/data
Infineon Technologies www.infineon.com/microcontrollers	TC116x	TriCore v1.3	80	32/16/8	16, 32	1.5/3.3	650 mW		Dual MAC, bit-reverse, signed-fraction, modulo, saturation, pre/post-increment, rounding	Single-precision	16-kbyte instruction, two-way set associative
Infineon Technologies www.infineon.com/microcontrollers	TC1764/2	TriCore v1.3	80	32/16/8	16, 32	1.5/3.3	650 mW		Dual MAC, bit-reverse, signed-fraction, modulo, saturation, pre/post-increment, rounding	Single-precision	16-kbyte instruction, two-way set associative
Infineon Technologies www.infineon.com/microcontrollers	TC1796	TriCore V1.2	150	32/16/8	16, 32	1.5/3.3	1.2W	Idle, sleep, deep sleep	Dual MAC, bit-reverse, signed-fraction, modulo, saturation, pre/post-increment, rounding	Single-precision	16-kbyte instruction, two-way set associative
Innovasic Semiconductor www.innovasic.com	fido1100	CPU32 (68000) Modified	66	32/16,8	32	3.3/3.3,5.0	500 mW	Single-Context Sleep, CPU Auto Sleep, CPU Idle, CPU Hard Sleep (<2mW), Peripheral Sleep,	32 x 32 Multiply, Divide		32-kbyte deterministic
Intel www.intel.com	Dual-Core Intel Xeon Processor	x86	1660		32		99			Yes	2-Mbyte
Intel www.intel.com	Intel Atom Processor N270	x86	1600		32		2.5			Yes	512-kbyte
Intel www.intel.com	Intel Atom Processor Z510	x86	1100		32		2			Yes	512-kbyte
Intel www.intel.com	Intel Atom Processor Z530	x86	1600		32		2			Yes	512-kbyte
Intel www.intel.com	Intel Celeron M Processor 320	x86	1300		32		24.5			Yes	512-kbyte
Intel www.intel.com	Intel Celeron M Processor 350	x86	1300		32		21			Yes	1-Mbyte
Intel www.intel.com	Intel Celeron M Processor 360	x86	1400		32		21			Yes	1-Mbyte
Intel www.intel.com	Intel Celeron M Processor 370	x86	1500		32		21			Yes	1-Mbyte
Intel www.intel.com	Intel Celeron M Processor 373	x86	1000		32		5.5			Yes	512-kbyte
Intel www.intel.com	Intel Celeron M Processor 380	x86	1600		32		21			Yes	1-Mbyte
Intel www.intel.com	Intel Celeron M Processor 383	x86	1000		32		5.5			Yes	1-Mbyte

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
40-kbyte ROM, 80-kbyte RAM, for microcode	8-channel DMA, 8-bit SDRAM (up to 4GB), serial/parallel Flash, MMC and SD		180 SSBGA	Up to 10 timers, 5/10/15-bit, prescaling, configurable	Two 10/100 Ethernet MII/RMI, three UARTs, I ² C / SPI master and slave, nine 8-bit ports, configurable serial/parallel interfaces to flash, MMC/SD	32 levels, 8 external, 256 service routine levels		-40 to +85	Single-pwr supply option; TCP/IP, IEEE1588 time stamping, RTOS, cryptography, battery-backed RTC	\$12.95
40-kbyte ROM, 80-kbyte RAM, for microcode	8-channel DMA, 8-bit SDRAM (up to 4GB), serial/parallel Flash, MMC and SD		180 SSBGA	Up to 10 timers, 5/10/15-bit, prescaling, configurable	Two 10/100 Ethernet MII/RMI, three UARTs, I ² C / SPI master and slave, nine 8-bit ports, configurable serial/parallel interfaces to flash, MMC/SD	32 levels, 8 external, 256 service routine levels	8-channel 16-bit; 2-channel 16-bit DAC	-40 to +85	Single-pwr supply option; Java VM, TCP/IP, RTOS, cryptography, graphics+LCD interface, battery-backed RTC	\$12.95
144-kbyte SRAM	8-, 16-, 32-bit, glueless, burst mode, SDRAM, PC100, PC133	Yes	208 PLBGA	Three 32-bit, four 16-bit, watchdog, system timer	Four CAN, three UART, two SPI, two I ² C, two MLI, four 16-bit port, 8-bit port	78		0 to +85	Two motor-control peripheral	\$12
144-kbyte SRAM	8-, 16-, 32-bit, glueless, burst mode, SDRAM, PC100, PC133	Yes	208 PLBGA	Three 32-bit, four 16-bit, watchdog, system timer	Four CAN, 10/100 MII Ethernet, USB 1.1, three UART, two SPI, two I ² C, two MLI, four 16-bit port, 8-bit port	95		0 to +85	Two motor-control peripheral	\$14.75
192-kbyte SRAM	8-, 16-, 32-bit, glueless, burst mode		176 TQFP	Sixty-four 24-bit, 192 16-bit	MultiCAN (2-4 Nodes), two SSC/SPI, two ASC, two MLI, two MSC, 127 PIO	181 IRQ	Dual 16-channel, 8/10/12-bit; Fast four-channel 10-bit	-40 to +85	Peripheral-control processor, prescaler, duty cycle, phase discrimination, digital PLL	\$12 to \$15
92-kbyte SRAM	8-, 16-, 32-bit, glueless, burst mode		176 TQFP	Thirty-six 24-bit, 12 16-bit	MultiCAN (2 Nodes), two SSC/SPI, two ASC, two MLI, two MSC, 127 PIO	181 IRQ	Dual 16-channel, 8/10/12-bit; Fast four-channel 10-bit	-40 to +85	Peripheral-control processor, prescaler, duty cycle, phase discrimination, digital PLL	\$15 to \$17
192-kbyte SRAM	8-, 16-, 32-bit, glueless, burst mode		416 PBGA	Sixty-four 24-bit, 192 16-bit	MultiCAN (4 Nodes), two SSC/SPI, two ASC, two MLI, two MSC, 127 PIO	181 IRQ	Dual 16-channel, 8/10/12-bit; Fast four-channel 10-bit	-40 to +85	Peripheral-control processor, prescaler, duty cycle, phase discrimination, digital PLL	\$20
24-kbyte Internal SRAM, up to 4-Gbyte external	Internal Perhiperal DMA, SDRAM Controller	Deterministic Memory Protection Unit	208PQFP, 208TQFP, 208BGA	Two 16-bit programmable Timer/Counter/PWM Units, watchdog, system timer, context timers	Four Universal Interface Controllers programmable for 10/100 Ethernet with MAC Filtering, CAN, UART, SPI, SMBus, GPIO, custom.	8 external, numerous internal	8 channel, 10-bit	-40 to +85	5 independent hardware contexts, 1-cycle context switching, time and space partitioning support, hardware endian conversion, Peripheral Management Unit	Under \$10.00
Varies by Chipset			PPGA478						65 nm	
Varies by Chipset			PBGA437						45 nm	\$40
Varies by Chipset			PBGA441						45 nm	\$20
Varies by Chipset			PBGA441						45 nm	\$70
Varies by Chipset			H-PBGA479						130 nm	
Varies by Chipset			H-PBGA479						90 nm	
Varies by Chipset			PPGA478						90 nm	
Varies by Chipset			H-PBGA479						90 nm	
Varies by Chipset			PPGA478						90 nm	
Varies by Chipset			H-PBGA479						90 nm	

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Intel www.intel.com	Intel Celeron M Processor 410	x86	1460		32		35			Yes	1-Mbyte
Intel www.intel.com	Intel Celeron M Processor 420	x86	1600		32		35			Yes	1-Mbyte
Intel www.intel.com	Intel Celeron M Processor 423	x86	1060		32		5.5			Yes	1-Mbyte
Intel www.intel.com	Intel Celeron M Processor 430	x86	1730		32		35			Yes	1-Mbyte
Intel www.intel.com	Intel Celeron M Processor 440	x86	1860		32		27			Yes	1-Mbyte
Intel www.intel.com	Intel Celeron M Processor 443	x86	1200		32		5.5			Yes	1-Mbyte
Intel www.intel.com	Intel Celeron M Processor 450	x86	2000		32		35			Yes	1-Mbyte
Intel www.intel.com	Intel Celeron Processor	x86	1660		32		27			Yes	1-Mbyte
Intel www.intel.com	Intel Celeron Processor	x86	1200		32		32.1			Yes	256-kbyte
Intel www.intel.com	Intel Celeron Processor	x86	2500		32		61			Yes	128-kbyte
Intel www.intel.com	Intel Celeron Processor	x86	850		32		26.7			Yes	128-kbyte
Intel www.intel.com	Intel Core Duo Processor L2300	x86	1500		32		15			Yes	2-Mbyte
Intel www.intel.com	Intel Core Duo Processor L2400	x86	1660		32		15			Yes	2-Mbyte
Intel www.intel.com	Intel Core Duo Processor L2500	x86	1830		32		27			Yes	2-Mbyte
Intel www.intel.com	Intel Core Duo Processor T2300	x86	1660		32		31			Yes	2-Mbyte
Intel www.intel.com	Intel Core Duo Processor T2300E	x86	1660		32		35			Yes	2-Mbyte
Intel www.intel.com	Intel Core Duo Processor T2400	x86	1830		32		27			Yes	2-Mbyte
Intel www.intel.com	Intel Core Duo Processor T2500	x86	2000		32		31			Yes	2-Mbyte
Intel www.intel.com	Intel Core Duo Processor T2600	x86	2160		32		31			Yes	2-Mbyte
Intel www.intel.com	Intel Core Duo Processor T2700	x86	2330		32		35			Yes	2-Mbyte
Intel www.intel.com	Intel Core Duo Processor U2400	x86	1060		32		5.5			Yes	2-Mbyte
Intel www.intel.com	Intel Core Duo Processor U2500	x86	1200		32		9			Yes	2-Mbyte
Intel www.intel.com	Intel Core Solo Processor T1300	x86	1660		32		27			Yes	2-Mbyte
Intel www.intel.com	Intel Core Solo Processor T1400	x86	1830		32		27			Yes	2-Mbyte
Intel www.intel.com	Intel Core Solo Processor U1300	x86	1060		32		27			Yes	2-Mbyte
Intel www.intel.com	Intel Core Solo Processor U1400	x86	1200		32		6			Yes	2-Mbyte
Intel www.intel.com	Intel Core Solo Processor U1500	x86	1330		32		5.5			Yes	2-Mbyte
Intel www.intel.com	Intel Xeon Processor	x86	2400		32		65			Yes	512-kbyte
Intel www.intel.com	Mobile Intel Celeron Processor	x86	2400		32		59.8			Yes	256-kbyte
Intel www.intel.com	Mobile Intel Pentium 4 Processor - M	x86	2200		32		35			Yes	512-kbyte
Intel www.intel.com	Pentium 4 Processor	x86	2800		32		68.4			Yes	512-kbyte
Intel www.intel.com	Pentium M Processor	x86	1600		32		24.5			Yes	1-Mbyte

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
Varies by Chipset			PPGA478						65 nm	
Varies by Chipset			PPGA478						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PPGA478						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PPGA478						65 nm	
Varies by Chipset			PPGA478						65 nm	
Varies by Chipset			PPGA370						130 nm	
Varies by Chipset			PPGA478						130 nm	
Varies by Chipset			PPGA370						180 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PPGA478						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PPGA478						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PPGA478						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PBGA479						65 nm	
Varies by Chipset			PPGA604						130 nm	
Varies by Chipset			PPGA478						130 nm	
Varies by Chipset			PPGA478						130 nm	
Varies by Chipset			PPGA478						130 nm	
Varies by Chipset			H-PBGA479						130 nm	

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Intel www.intel.com	Pentium M Processor 713	x86	1100		32		12			Yes	1-Mbyte
Intel www.intel.com	Pentium M Processor 730	x86	1600		32		27			Yes	2-Mbyte
Intel www.intel.com	Pentium M Processor 733	x86	1100		32		5.5			Yes	2-Mbyte
Intel www.intel.com	Pentium M Processor 738	x86	1400		32		10			Yes	2-Mbyte
Intel www.intel.com	Pentium M Processor 740	x86	1730		32		27			Yes	2-Mbyte
Intel www.intel.com	Pentium M Processor 745	x86	1800		32		21			Yes	2-Mbyte
Intel www.intel.com	Pentium M Processor 750	x86	1860		32		27			Yes	2-Mbyte
Intel www.intel.com	Pentium M Processor 753	x86	1200		32		5.5			Yes	2-Mbyte
Intel www.intel.com	Pentium M Processor 760	x86	2000		32		27			Yes	2-Mbyte
Intel www.intel.com	Pentium M Processor 770	x86	2130		32		27			Yes	2-Mbyte
Intel www.intel.com	Pentium M Processor 773	x86	1300		32		5.5			Yes	2-Mbyte
Intel www.intel.com	Pentium M Processor 778	x86	1600		32		27			Yes	2-Mbyte
Intel www.intel.com	Pentium M Processor 780	x86	2260		32		27			Yes	2-Mbyte
IPFlex www.ipflex.com	DAPDNA-2	IPFlex	166	128	32	2.5, 3.3	2 to 3W				8-kword instruction/data
IPFlex www.ipflex.com	DAPDNA-IMS	IPFlex	200, 266	128	16, 32	1.2, 1.8, 3.3					8-kword instruction/data
Kawasaki Microelectronics www.k-micro.us	CatEye dual 24Kf (Pro)	MIPS32	400 to 600	32/64	32	Process dependent	Design dependent	Sleep, Powerdown		IEEE-754 compliant (24Kf)	0/8/16/32/64-kbyte instruction/data; up to 1-MByte scratchpad
Kawasaki Microelectronics www.k-micro.us	Topaz 24Kf (Pro)	MIPS32	200 to 500	32/64	32	Process dependent	Design dependent	Sleep, Powerdown		IEEE-754 compliant (24Kf)	0/8/16/32/64-kbyte instruction/data; up to 1-MByte scratchpad
Lattice Semiconductor www.latticesemi.com	LatticeMico32	LatticeMico32 Open Source	Over 150, device dependant	32/32	32	Device dependant	Device dependant	Fully static	32x32 mult, Wishbone bus (OpenCores)		1-, 2-, 4-, 8-, 16-, 32-kbyte instruction/data, 1 or 2 set associative (optional)
Luminary Micro www.luminarymicro.com	LM3S101	ARM Cortex-M3	20	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S102	ARM Cortex-M3	20	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1110	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1133	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1138	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		

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Varies by Chipset			H-PBGA479						130 nm	
Varies by Chipset			PPGA478						90 nm	
Varies by Chipset			H-PBGA479						90 nm	
Varies by Chipset			H-PBGA479						90 nm	
Varies by Chipset			H-PBGA479						90 nm	
Varies by Chipset			PPGA478						90 nm	
Varies by Chipset			H-PBGA479						90 nm	
Varies by Chipset			H-PBGA479						90 nm	
Varies by Chipset			H-PBGA479						90 nm	
Varies by Chipset			H-PBGA479						90 nm	
Varies by Chipset			H-PBGA479						90 nm	
Varies by Chipset			H-PBGA479						90 nm	
Varies by Chipset			PPGA479						90 nm	
608-kbyte including buffers	DDR		1156 FCBGA	32-bit, watchdog	PCI, UART, SPI, GPIO, Direct I/O (original)	16		-40 to +125	376 32-bit processing elements including 56 multipliers, dynamically reconfigurable	\$350
608-kbyte including buffers	DDR2		1156 TEPBGA	32-bit, watchdog	PCI-express (4 lane), UART, SPI, GPIO, Direct I/O (original)	16		-40 to +125		
Configurable	DMA DDR2	16, 32, 64-entry jTLB with variable page size, optional FMT	Design dependent	8-16 bit	16750 UART	17		0 to +70	Dual Gbit Ethernet MAC, USB host & device,	Under \$20
Configurable	DMA DDR2	16, 32, 64-entry jTLB with variable page size, optional FMT	Design dependent	8-16 bit	16749 UART	17		0 to +70	Security engine	Under \$15
Device dependant	DDR, DDR2, SRAM, On-chip		IP Core	32-bit	I2C IP (OpenCores), SPI IP, GPIO IP, UART IP	32		(Core)	Open Source, 32 general purpose registers, built-in debug support	
Single-cycle 8-kbyte Flash, 2-kbyte SRAM	On-chip memory controller		28 SOIC	1 24-bit timer, 2 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	1 UART, 1 SSI, from 2 to 18 GPIO	14 interrupts with 8 priority levels on up to 18 pins	2 Analog Comparators	-40 to +85	1 CCP, LDO Voltage Regulator	
Single-cycle 8-kbyte Flash, 2-kbyte SRAM	On-chip memory controller		28 SOIC	1 24-bit timer, 2 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	1 UART, 1 SSI, 1 I ² C, from 0 to 18 GPIO	14 interrupts with 8 priority levels on up to 18 pins	1 Analog Comparator	-40 to +85	2 CCP, LDO Voltage Regulator	
Single-cycle 64-kbyte Flash, 16-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, from 20 to 41 GPIO	23 interrupts with 8 priority levels on up to 41 pins	2 Analog Comparators	-40 to +85	2 CCP, - QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 64-kbyte Flash, 16-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 1 I ² C, from 9 to 44 GPIO	33 interrupts with 8 priority levels on up to 44 pins	1 Analog Comparator, 2 10-bit (+/- 1LSB) ADC Channels	-40 to +85	2 Motion Control PWM Outputs, Dead-Band Generator, 8 CCP, - QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 64-kbyte Flash, 16-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 2 I ² C, from 9 to 46 GPIO	34 interrupts with 8 priority levels on up to 46 pins	3 Analog Comparators, 8 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 CCP, - QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Luminary Micro www.luminarymicro.com	LM3S1150	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1162	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1165	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1332	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1435	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1439	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1512	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1538	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1620	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1635	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1637	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
Single-cycle 64-kbyte Flash, 16-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 1 I ² C, from 7 to 52 GPIO	34 interrupts with 8 priority levels on up to 52 pins	3 Analog Comparators	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, 1 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 64-kbyte Flash, 16-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 1 I ² C, from 4 to 46 GPIO	37 interrupts with 8 priority levels on up to 46 pins	3 Analog Comparators, 2 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, - QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 64-kbyte Flash, 16-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 1 I ² C, from 4 to 43 GPIO	35 interrupts with 8 priority levels on up to 43 pins	1 Analog Comparator, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 8 CCP, - QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 96-kbyte Flash, 16-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, from 29 to 57 GPIO	30 interrupts with 8 priority levels on up to 57 pins	3 Analog Comparators, 3 10-bit (+/- 1LSB) ADC Channels	-40 to +85	- Motion Control PWM Outputs, Dead-Band Generator, 8 CCP, - QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 96-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, from 21 to 46 GPIO	29 interrupts with 8 priority levels on up to 46 pins	1 Analog Comparator, 2 10-bit (+/- 1LSB) ADC Channels	-40 to +85	2 Motion Control PWM Outputs, Dead-Band Generator, 4 CCP, - QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 96-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 2 SSI, 1 I ² C, from 14 to 52 GPIO	33 interrupts with 8 priority levels on up to 52 pins	1 Analog Comparator, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, 1 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 96-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 2 I ² C, from 15 to 58 GPIO	35 interrupts with 8 priority levels on up to 58 pins	3 Analog Comparators, 2 10-bit (+/- 1LSB) ADC Channels	-40 to +85	- Motion Control PWM Outputs, Dead-Band Generator, 8 CCP, 1 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 96-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 2 I ² C, from 9 to 43 GPIO	32 interrupts with 8 priority levels on up to 43 pins	8 10-bit (+/- 1LSB) ADC Channels	-40 to +85	- Motion Control PWM Outputs, Dead-Band Generator, 8 CCP, 1 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 128-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 2 SSI, 1 I ² C, from 11 to 52 GPIO	31 interrupts with 8 priority levels on up to 52 pins	3 Analog Comparators	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 4 CCP, 1 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 128-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 2 I ² C, from 12 to 56 GPIO	37 interrupts with 8 priority levels on up to 56 pins	2 Analog Comparators, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 8 CCP, - QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 128-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 1 SSI, 1 I ² C, from 7 to 43 GPIO	35 interrupts with 8 priority levels on up to 43 pins	1 Analog Comparator, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, 1 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Luminary Micro www.luminarymicro.com	LM3S1751	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1850	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1937	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1958	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1960	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S1968	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S2110	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S2139	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S2410	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S2412	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S2432	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S2533	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
Single-cycle 128-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 1 I ² C, from 21 to 56 GPIO	32 interrupts with 8 priority levels on up to 56 pins	1 Analog Comparator, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	4 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, - QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, from 17 to 56 GPIO	30 interrupts with 8 priority levels on up to 56 pins	3 Analog Comparators	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, 1 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, from 27 to 56 GPIO	31 interrupts with 8 priority levels on up to 56 pins	1 Analog Comparator, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 4 CCP, - QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 2 I ² C, from 21 to 52 GPIO	31 interrupts with 8 priority levels on up to 52 pins	8 10-bit (+/- 1LSB) ADC Channels	-40 to +85	- Motion Control PWM Outputs, Dead-Band Generator, 8 CCP, - QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 2 I ² C, from 7 to 60 GPIO	36 interrupts with 8 priority levels on up to 60 pins	3 Analog Comparators	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 8 CCP, 2 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 2 I ² C, from 5 to 52 GPIO	40 interrupts with 8 priority levels on up to 52 pins	3 Analog Comparators, 8 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 4 CCP, 2 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 64-kbyte Flash, 16-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	1 UART, 1 SSI, 1 I ² C, 1 CAN, from 11 to 40 GPIO	26 interrupts with 8 priority levels on up to 40 pins	3 Analog Comparators	-40 to +85	2 Motion Control PWM Outputs, Dead-Band Generator, 4 CCP, LDO Voltage Regulator	
Single-cycle 64-kbyte Flash, 16-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, 1 CAN, from 26 to 56 GPIO	29 interrupts with 8 priority levels on up to 56 pins	3 Analog Comparators, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 CCP, LDO Voltage Regulator	
Single-cycle 96-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	1 UART, 1 SSI, 1 I ² C, 1 CAN, from 37 to 60 GPIO	22 interrupts with 8 priority levels on up to 60 pins	2 Analog Comparators	-40 to +85	4 CCP, LDO Voltage Regulator	
Single-cycle 96-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, 1 CAN, from 20 to 49 GPIO	30 interrupts with 8 priority levels on up to 49 pins	2 Analog Comparators, 3 10-bit (+/- 1LSB) ADC Channels	-40 to +85	2 Motion Control PWM Outputs, Dead-Band Generator, 4 CCP, LDO Voltage Regulator	
Single-cycle 96-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, 1 CAN, from 4 to 34 GPIO	30 interrupts with 8 priority levels on up to 34 pins	2 Analog Comparators, 3 10-bit (+/- 1LSB) ADC Channels	-40 to +85	2 Motion Control PWM Outputs, Dead-Band Generator, 4 CCP, LDO Voltage Regulator	
Single-cycle 96-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, 1 CAN, from 11 to 48 GPIO	36 interrupts with 8 priority levels on up to 48 pins	3 Analog Comparators, 3 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, Battery-Backed Hibernate Module, LDO Voltage Regulator	

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Luminary Micro www.luminarymicro.com	LM3S2620	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S2637	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S2651	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S2730	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S2739	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S2939	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S2948	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S2950	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S2965	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S301	ARM Cortex-M3	20	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S310	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S315	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
Single-cycle 128-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	1 UART, 1 SSI, 1 I ² C, 2 CAN, from 12 to 52 GPIO	32 interrupts with 8 priority levels on up to 52 pins	3 Analog Comparators	-40 to +85	4 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, 1 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 128-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, 1 CAN, from 15 to 46 GPIO	32 interrupts with 8 priority levels on up to 46 pins	3 Analog Comparators, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 CCP, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 128-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 1 I ² C, 1 CAN, from 16 to 53 GPIO	35 interrupts with 8 priority levels on up to 53 pins	1 Analog Comparator, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	4 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 128-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	1 UART, 1 SSI, 1 I ² C, 1 CAN, from 37 to 60 GPIO	22 interrupts with 8 priority levels on up to 60 pins	2 Analog Comparators	-40 to +85	4 CCP, LDO Voltage Regulator	
Single-cycle 128-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, 1 CAN, from 20 to 56 GPIO	33 interrupts with 8 priority levels on up to 56 pins	1 Analog Comparator, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, 1 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 1 SSI, 1 I ² C, 1 CAN, from 18 to 57 GPIO	35 interrupts with 8 priority levels on up to 57 pins	3 Analog Comparators, 3 10-bit (+/- 1LSB) ADC Channels	-40 to +85	4 Motion Control PWM Outputs, Dead-Band Generator, 4 CCP, 1 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 1 I ² C, 2 CAN, from 12 to 52 GPIO	35 interrupts with 8 priority levels on up to 52 pins	3 Analog Comparators, 8 10-bit (+/- 1LSB) ADC Channels	-40 to +85	- Motion Control PWM Outputs, Dead-Band Generator, 8 CCP, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 1 I ² C, 2 CAN, from 10 to 60 GPIO	36 interrupts with 8 priority levels on up to 60 pins	3 Analog Comparators	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, 1 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 2 I ² C, 2 CAN, from 3 to 56 GPIO	42 interrupts with 8 priority levels on up to 56 pins	3 Analog Comparators, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, 2 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 16-kbyte Flash, 2-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 2 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	1 UART, 1 SSI, from 12 to 33 GPIO	22 interrupts with 8 priority levels on up to 33 pins	2 Analog Comparators, 3 10-bit (+/- 1LSB) ADC Channels	-40 to +85	2 Motion Control PWM Outputs, Dead-Band Generator, 2 CCP, LDO Voltage Regulator	
Single-cycle 16-kbyte Flash, 4-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, from 3 to 36 GPIO	24 interrupts with 8 priority levels on up to 36 pins	3 Analog Comparators	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, LDO Voltage Regulator	
Single-cycle 16-kbyte Flash, 4-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, from 7 to 32 GPIO	24 interrupts with 8 priority levels on up to 32 pins	1 Analog Comparator, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	2 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, LDO Voltage Regulator	

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Luminary Micro www.luminarymicro.com	LM3S316	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S317	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S328	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S601	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S610	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S6100	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S611	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S6110	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S612	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S613	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S615	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S617	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S618	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
Single-cycle 16-kbyte Flash, 4-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, from 3 to 32 GPIO	26 interrupts with 8 priority levels on up to 32 pins	1 Analog Comparator, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	4 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, LDO Voltage Regulator	
Single-cycle 16-kbyte Flash, 4-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, from 3 to 30 GPIO	25 interrupts with 8 priority levels on up to 30 pins	3 Analog Comparators, 6 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, LDO Voltage Regulator	
Single-cycle 16-kbyte Flash, 4-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, from 7 to 28 GPIO	22 interrupts with 8 priority levels on up to 28 pins	8 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 CCP, LDO Voltage Regulator	
Single-cycle 32-kbyte Flash, 8-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, from 0 to 36 GPIO	26 interrupts with 8 priority levels on up to 36 pins	3 Analog Comparators	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, 1 QE1, LDO Voltage Regulator	
Single-cycle 32-kbyte Flash, 8-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, from 6 to 34 GPIO	26 interrupts with 8 priority levels on up to 34 pins	2 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, LDO Voltage Regulator	
Single-cycle 64-kbyte Flash, 16-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	1 UART, 1 SSI, Ethernet MAC+PHY, from 10 to 30 GPIO	20 interrupts with 8 priority levels on up to 30 pins	1 Analog Comparator	-40 to +85	4 CCP, LDO Voltage Regulator	
Single-cycle 32-kbyte Flash, 8-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, from 4 to 32 GPIO	26 interrupts with 8 priority levels on up to 32 pins	4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, LDO Voltage Regulator	
Single-cycle 64-kbyte Flash, 16-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	1 UART, 1 SSI, Ethernet MAC+PHY, from 8 to 35 GPIO	24 interrupts with 8 priority levels on up to 35 pins	3 Analog Comparators	-40 to +85	2 Motion Control PWM Outputs, Dead-Band Generator, 4 CCP, LDO Voltage Regulator	
Single-cycle 32-kbyte Flash, 8-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, from 7 to 34 GPIO	25 interrupts with 8 priority levels on up to 34 pins	1 Analog Comparator, 2 10-bit (+/- 1LSB) ADC Channels	-40 to +85	2 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, LDO Voltage Regulator	
Single-cycle 32-kbyte Flash, 8-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, from 3 to 32 GPIO	26 interrupts with 8 priority levels on up to 32 pins	1 Analog Comparator, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	4 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, LDO Voltage Regulator	
Single-cycle 32-kbyte Flash, 8-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, from 0 to 34 GPIO	29 interrupts with 8 priority levels on up to 34 pins	3 Analog Comparators, 2 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, LDO Voltage Regulator	
Single-cycle 32-kbyte Flash, 8-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, from 1 to 30 GPIO	26 interrupts with 8 priority levels on up to 30 pins	1 Analog Comparator, 6 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, LDO Voltage Regulator	
Single-cycle 32-kbyte Flash, 8-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, from 0 to 30 GPIO	27 interrupts with 8 priority levels on up to 30 pins	1 Analog Comparator, 6 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 4 CCP, 1 QE1, LDO Voltage Regulator	

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Luminary Micro www.luminarymicro.com	LM3S628	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S6420	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S6422	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S6432	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S6537	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S6610	ARM Cortex-M3	25	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S6633	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S6637	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S6730	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S6753	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S6938	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S6950	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
Single-cycle 32-kbyte Flash, 8-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, from 9 to 28 GPIO	22 interrupts with 8 priority levels on up to 28 pins	8 10-bit (+/- 1LSB) ADC Channels	-40 to +85	4 CCP, LDO Voltage Regulator	
Single-cycle 96-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	1 UART, 1 SSI, Ethernet MAC+PHY, from 23 to 46 GPIO	21 interrupts with 8 priority levels on up to 46 pins	2 Analog Comparators	-40 to +85	4 CCP, LDO Voltage Regulator	
Single-cycle 96-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	1 UART, 1 SSI, Ethernet MAC+PHY, from 12 to 34 GPIO	25 interrupts with 8 priority levels on up to 34 pins	2 Analog Comparators, 2 10-bit (+/- 1LSB) ADC Channels	-40 to +85	4 CCP, LDO Voltage Regulator	
Single-cycle 96-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, Ethernet MAC+PHY, from 14 to 43 GPIO	29 interrupts with 8 priority levels on up to 43 pins	2 Analog Comparators, 3 10-bit (+/- 1LSB) ADC Channels	-40 to +85	2 Motion Control PWM Outputs, Dead-Band Generator, 4 CCP, LDO Voltage Regulator	
Single-cycle 96-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, Ethernet MAC+PHY, from 6 to 41 GPIO	34 interrupts with 8 priority levels on up to 41 pins	2 Analog Comparators, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 128-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 1 SSI, 1 I ² C, Ethernet MAC+PHY, from 5 to 46 GPIO	32 interrupts with 8 priority levels on up to 46 pins	3 Analog Comparators	-40 to +85	4 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, 1 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 128-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, Ethernet MAC+PHY, from 15 to 41 GPIO	27 interrupts with 8 priority levels on up to 41 pins	1 Analog Comparator, 3 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 CCP, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 128-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, Ethernet MAC+PHY, from 11 to 41 GPIO	31 interrupts with 8 priority levels on up to 41 pins	3 Analog Comparators, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 CCP, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 128-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	1 UART, 1 SSI, Ethernet MAC+PHY, from 23 to 46 GPIO	21 interrupts with 8 priority levels on up to 46 pins	2 Analog Comparators	-40 to +85	4 CCP, LDO Voltage Regulator	
Single-cycle 128-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, Ethernet MAC+PHY, from 5 to 41 GPIO	35 interrupts with 8 priority levels on up to 41 pins	2 Analog Comparators, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 4 CCP, 1 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 1 SSI, 1 I ² C, Ethernet MAC+PHY, from 7 to 38 GPIO	32 interrupts with 8 priority levels on up to 38 pins	3 Analog Comparators, 8 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 CCP, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 1 I ² C, Ethernet MAC+PHY, from 1 to 46 GPIO	34 interrupts with 8 priority levels on up to 46 pins	3 Analog Comparators	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, 1 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Luminary Micro www.luminarymicro.com	LM3S6952	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S6965	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S801	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S811	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S812	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S815	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S817	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S818	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S828	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S8530	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S8538	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S8630	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S8730	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 1 SSI, 1 PC, Ethernet MAC+PHY, from 6 to 43 GPIO	34 interrupts with 8 priority levels on up to 43 pins	3 Analog Comparators, 3 10-bit (+/- 1LSB) ADC Channels	-40 to +85	4 Motion Control PWM Outputs, Dead-Band Generator, 4 CCP, 1 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 1 SSI, 2 PC, Ethernet MAC+PHY, from 0 to 42 GPIO	38 interrupts with 8 priority levels on up to 42 pins	2 Analog Comparators, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 4 CCP, 2 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 64-kbyte Flash, 8-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 PC, from 0 to 36 GPIO	26 interrupts with 8 priority levels on up to 36 pins	3 Analog Comparators	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, 1 QEI, LDO Voltage Regulator	
Single-cycle 64-kbyte Flash, 8-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 PC, from 1 to 32 GPIO	27 interrupts with 8 priority levels on up to 32 pins	1 Analog Comparator, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, LDO Voltage Regulator	
Single-cycle 64-kbyte Flash, 8-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 PC, from 7 to 34 GPIO	25 interrupts with 8 priority levels on up to 34 pins	1 Analog Comparator, 2 10-bit (+/- 1LSB) ADC Channels	-40 to +85	2 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, LDO Voltage Regulator	
Single-cycle 64-kbyte Flash, 8-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 PC, from 0 to 34 GPIO	29 interrupts with 8 priority levels on up to 34 pins	3 Analog Comparators, 2 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, LDO Voltage Regulator	
Single-cycle 64-kbyte Flash, 8-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 PC, from 1 to 30 GPIO	26 interrupts with 8 priority levels on up to 30 pins	6 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 6 CCP, LDO Voltage Regulator	
Single-cycle 64-kbyte Flash, 8-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 PC, from 0 to 30 GPIO	27 interrupts with 8 priority levels on up to 30 pins	6 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 4 CCP, 1 QEI, LDO Voltage Regulator	
Single-cycle 64-kbyte Flash, 8-kbyte SRAM	On-chip memory controller	MPU	48 LQFP	1 24-bit timer, 3 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 PC, from 7 to 28 GPIO	22 interrupts with 8 priority levels on up to 28 pins	8 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 CCP, LDO Voltage Regulator	
Single-cycle 96-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	1 UART, 2 SSI, 1 PC, Ethernet MAC+PHY, 3 CAN, from 8 to 35 GPIO	26 interrupts with 8 priority levels on up to 35 pins		-40 to +85	2 CCP, LDO Voltage Regulator	
Single-cycle 96-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 PC, Ethernet MAC+PHY, 1 CAN, from 7 to 36 GPIO	31 interrupts with 8 priority levels on up to 36 pins	3 Analog Comparators, 8 10-bit (+/- 1LSB) ADC Channels	-40 to +85	4 CCP, LDO Voltage Regulator	
Single-cycle 128-kbyte Flash, 32-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 PC, Ethernet MAC+PHY, 1 CAN, from 10 to 31 GPIO	25 interrupts with 8 priority levels on up to 31 pins		-40 to +85	2 CCP, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 128-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 PC, Ethernet MAC+PHY, 1 CAN, from 11 to 32 GPIO	25 interrupts with 8 priority levels on up to 32 pins		-40 to +85	2 CCP, Battery-Backed Hibernate Module, LDO Voltage Regulator	

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Luminary Micro www.luminarymicro.com	LM3S8733	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S8738	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S8930	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S8933	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S8938	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S8962	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Luminary Micro www.luminarymicro.com	LM3S8970	ARM Cortex-M3	50	internal: 32	16, 32	2.5/3.3		Sleep, Deep Sleep, Battery-Backed Hibernate	Single-cycle 32-bit multiply, 32-bit hardware divide		
Microchip Technology www.microchip.com	PIC32	MIPS RISC Harvard	40 or 80	32/32 (Internal Buses) 16/16 Parallel Master Port (External)	32	2.3 to 3.6	181 mW	Idle, individual peripheral enable/disable, low power sleep,	32x32 Multiply/Divide Unit, single cycle 32x16 and 16x16 multiply, two cycle 32x32 multiply with 64-bit result	Math Software Library Support for Single & Double precision	Prefetch module with 256-Byte Cache (speeds execution from Flash)
MIPS Technologies www.mips.com	1004Kc 1004Kf Coherent Processing System IP Cores	MIPS32	750+ (65nm PTSI)	32/64/256	32	Process dependent	Process dependent	Wait	SIMD, 8x8, 16x16, 32x32	IEEE-754 compliant (1004KEf)	Per Core: 0/8/16/32/64-kbyte instruction/data; up to 1-MByte scratchpad
MIPS Technologies www.mips.com	24Kc (Pro) 24Kf (Pro) IP Cores	MIPS32	800+ (65nm PTSI)	32/64	32	Process dependent	Process dependent	Wait	32x32	IEEE-754 compliant (24Kf)	0/8/16/32/64-kbyte instruction/data; up to 1-MByte scratchpad

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
Single-cycle 128-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, Ethernet MAC+PHY, 1 CAN, from 5 to 35 GPIO	32 interrupts with 8 priority levels on up to 35 pins	3 Analog Comparators, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	4 CCP, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 128-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 2 SSI, 1 I ² C, Ethernet MAC+PHY, 1 CAN, from 4 to 38 GPIO	32 interrupts with 8 priority levels on up to 38 pins	1 Analog Comparator, 8 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 CCP, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	1 UART, 1 SSI, 1 I ² C, Ethernet MAC+PHY, 2 CAN, from 13 to 34 GPIO	25 interrupts with 8 priority levels on up to 34 pins		-40 to +85	2 CCP, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, Ethernet MAC+PHY, 1 CAN, from 6 to 36 GPIO	32 interrupts with 8 priority levels on up to 36 pins	3 Analog Comparators, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	4 CCP, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	3 UART, 1 SSI, 2 I ² C, Ethernet MAC+PHY, 1 CAN, from 3 to 38 GPIO	34 interrupts with 8 priority levels on up to 38 pins	3 Analog Comparators, 8 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 CCP, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 1 SSI, 1 I ² C, Ethernet MAC+PHY, 1 CAN, from 5 to 42 GPIO	36 interrupts with 8 priority levels on up to 42 pins	1 Analog Comparator, 4 10-bit (+/- 1LSB) ADC Channels	-40 to +85	6 Motion Control PWM Outputs, Dead-Band Generator, 2 CCP, 2 QEI, Battery-Backed Hibernate Module, LDO Voltage Regulator	
Single-cycle 256-kbyte Flash, 64-kbyte SRAM	On-chip memory controller	MPU	100 LQFP	1 24-bit timer, 4 Timer/PWM/CCP Modules, each 32-bit or 2x16-bit	2 UART, 2 SSI, 1 I ² C, Ethernet MAC+PHY, 3 CAN, from 17 to 46 GPIO	28 interrupts with 8 priority levels on up to 46 pins		-40 to +85	2 CCP, Battery-Backed Hibernate Module, LDO Voltage Regulator	
32- to 512-kbyte Flash 8- to 32-kbyte RAM	6 channel DMA controller, 4 channels programmable, 2 channels dedicated for USB OTG	Fixed Mapping Translation, Kernel and User Modes, Code Protection	64 and 100 TQFP	Up to Five 16-bit Timers, can pair them for 2x32-bit, Up to 5 channels of input capture/output compare or PWM, watchdog, Real-Time Clock & Calendar	USB Device, Host, Dual Role and OTG, 2 SPI, 2 I ² C, 2 UARTs, 8/16-bit PMP, up to 85 GPIO	Up to 96 sources, 7 priority levels, 4 sub-priority levels, 5 external interrupt pins, single and multi-vector modes	Up to 16-channels, 500Ksps, 10-bit resolution	-40 to +85	12Kbyte Boot Flash, code execution from RAM, Atomic Bit operations on peripherals, I/Os toggle every cycle at up to 80MHz, 2 sets of 32 general purpose registers, brown out and low voltage detect, JTAG Debug and Programming, hardware instruction trace,	\$2.95 to \$5.54
Configurable	Not included, but IP core designed for use with DMA, mem controller blocks	16, 32, 64-entry jTLB with variable page size, optional FMT	IP core			Global Interrupt Controller (cross core/thread interrupt handling)	(core) Available separately	(Core)	First multi-threaded cache coherent multiprocessor licensable IP core. Scalable from 1-4 cores (each core similar to 34K) + cache coherence + IO coherence + global interrupt controller	License
Configurable	Not included, but IP core designed for use with DMA, mem controller blocks	16, 32, 64-entry jTLB with variable page size, optional FMT	IP core				(core) Available separately	(Core)	Synthesizable core, OCP interface, CorExtend user defined instructions	License

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
MIPS Technologies www.mips.com	24KEc (Pro) 24KEf (Pro) IP Cores	MIPS32 with DSP ASE	800+ (65nm PTSI)	32/64	32	Process dependent	Process dependent	Wait	SIMD, 8x8, 16x16, 32x32	IEEE-754 compliant (24KEf)	0/8/16/32/64-kbyte instruction/data; up to 1-MByte scratchpad
MIPS Technologies www.mips.com	34Kc (Pro) 34Kf (Pro) IP Core	MIPS32 with DSP ASE and MT ASE	750+ (65nm PTSI)	32/64	32	Process dependent	Process dependent	Wait	SIMD, 8x8, 16x16, 32x32	IEEE-754 compliant (34Kf)	0/8/16/32/64-kbyte instruction/data; up to 1-MByte scratchpad
MIPS Technologies www.mips.com	4Kc 4Km 4Kp IP Cores	MIPS32	500+ (65nm PTSI)	32/32	32	Process dependent	Process dependent	Wait	One-cycle 16x16, 32x16, two-cycle 32x32		0- to 16-kbyte instruction/data
MIPS Technologies www.mips.com	4KEc (Pro) 4KEm (Pro) 4KEp (Pro) IP Cores	MIPS32	500+ (65nm PTSI)	32/32	32	Process dependent	Process dependent	Wait	One-cycle 16x16, 32x16, two-cycle 32x32		0- to 64-kbyte instruction/data
MIPS Technologies www.mips.com	4KSd IP Core	MIPS32 with SmartMIPS ASE	500+ (65nm PTSI)	32/32	32	Process dependent	Process dependent	Wait	One-cycle 16x16, 32x16, two-cycle 32x32		0- to 64-kbyte instruction/data
MIPS Technologies www.mips.com	74Kc 74Kf IP Cores	MIPS32 with DSP ASE Rev 2	1100+ (65nm PTSI)	32/64	128	Process dependent	Process dependent	Wait	SIMD, 8x8, 16x16, 32x32	IEEE-754 compliant (74Kf)	8/16/32/64-kbyte instruction/data; up to 1-MByte scratchpad
MIPS Technologies www.mips.com	M4K M4K Pro IP Cores	MIPS32	500+ (65nm PTSI)	32/32, SRAM	32	Process dependent	Process dependent	Wait	One-cycle 16x16, 32x16, two-cycle 32x32		
NEC Electronics America www.am.necel.com	78K0R/lx3	NEC 78K0R	20		16	2.7 to 5.5			16x16 ->32 multiply		
NEC Electronics America www.am.necel.com	V850E/Dx3	NEC V850	48	32	32, 16	4.5 to 5.5		Halt, Idle, Watch, Sub-Watch, Stop	16x16, 32x32 multiply		
NEC Electronics America www.am.necel.com	V850E/IF3	NEC V850	64		32, 16	3.5 to 5.5	64 mA	Halt, Idle, Stop; 40uA	16x16->32, 32x32->64multiply		
NEC Electronics America www.am.necel.com	V850E/IG3	NEC V850	64	16/16	32, 16	3.5 to 5.5	64 mA	Halt, Idle, Stop; 40uA	16x16->32, 32x32->64multiply		
NEC Electronics America www.am.necel.com	V850E/PHO3	NEC V850	128	22/32 non-multiplexed	32, 16	1.5/3.3		Halt	16x16, 32x32 multiply	Yes	
NEC Electronics America www.am.necel.com	V850ES/Fx3	NEC V850	32, 48	24/16	32, 16	3.3 to 5.5	63 mA	Halt, Idle 1/2, sub-idle, Stop; 7.5uA	16x16 ->32 multiply		
NEC Electronics America www.am.necel.com	V850ES/Fx3-L	NEC V850	20	24/16	32, 16	3.3 to 5.5	25 mA	Halt, Idle 1/2, sub-idle, Stop; 7.5uA	16x16 ->32 multiply		

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
Configurable	Not included, but IP core designed for use with DMA, mem controller blocks	16, 32, 64-entry jTLB with variable page size, optional FMT	IP core				(core) Available separately	(Core)	Synthesizable core, OCP interface, CorExtend user defined instructions, DSP ASE	License
Configurable	Not included, but IP core designed for use with DMA, mem controller blocks	16, 32, 64-entry jTLB with variable page size, optional FMT	IP core				(core) Available separately	(Core)	First multi-threaded core family, OCP interface, CorExtend user defined instructions, DSP ASE, MT ASE	License
Configurable	Not included, but IP core designed for use with DMA, mem controller blocks	16 dual-entry jTLB with variable page size or FMT mechanism	IP core				(core) Available separately	(Core)	Synthesizable core	License
Configurable	Not included, but IP core designed for use with DMA, mem controller blocks	16/32 dual-entry jTLB with variable page size or FMT mechanism	IP core				(core) Available separately	(Core)	Synthesizable core, CorExtend user-instructions	License
Configurable	Not included, but IP core designed for use with DMA, mem controller blocks	16/32 dual-entry jTLB with variable page size or FMT mechanism	IP core				(core) Available separately	(Core)	Synthesizable core, code compression, SmartMIPS ASE, crypto-acceleration, CorExtend user-instructions	License
Configurable	Not included, but IP core designed for use with DMA, mem controller blocks	16, 32, 64-entry jTLB with variable page size, optional FMT	IP core				(core) Available separately	(Core)	Embedded industry's first synthesizable core to achieve speeds greater than 1 GHz; 17-stage, dual issue pipeline, out-of-order dispatch	License
Configurable			IP core				(core) Available separately	(Core)	Synthesizable core, cacheless design for multiprocessor designs	License
16-kbyte to 64-kbyte Flash 1-kbyte to 3-kbyte RAM	2-Channel DMA		30, 38 SSOP 44, 48, 52, 64 LQFP	12 16-bit, PWM, watchdog	CSI, UART, I ² C	up to 8 external, up to 34 internal	6 to 12 channel, 10-bit	-40 to +85	Op Amp, Comparator, POC, LVI, HW multiplier/divider	
128-kbyte to 2-Mbyte Flash, 6-kbyte to 84-kbyte RAM	4-channel DMA		100/144/208 QFP	16-bit, PWM, stepper motor controller, sound generator, watchdog	CSI, UART, LIN, CAN, I ² C	4 to 8 external, 47 to 91 internal	8- to 16-channel, 10-bit	-40 to +85	Stepper motor driver, sound generator, power-on clear, low-voltage indicator, LCD controller	
128-to 256-kbyte Flash, 8-to12-kbyte RAM	4-channel DMA		80 LQFP	16-bit, WDT, PWM, Timer for Inverter n+TMQOP) x 2-channel	UART, CSI, I ² C	15 external, 73 internal	Dual 5-channel 12-bit; 4-channel 10-bit	-40 to +85	On-chip OP AMP and comparators, POC, LVI.	
128-to 256-kbyte Flash, 8-to12-kbyte RAM	4-channel DMA		100 LQFP/(FP) LQFP	16-bit, WDT, PWM, Timer for Inverter n+TMQOP) x 2-channel	UART, CSI, I ² C	21 external, 74 internal	Dual 5-channel 12-bit; 8-channel 10-bit	-40 to +85	On-chip OP AMP and comparators, POC, LVI.	
1-Mbyte Flash 60-kbyte RAM	8-channel DMA		357 BGA Bare Die	16-bit, PWM, 3-phase motor controller, watchdog	CSI, UART, LIN, CAN, FlexRay	14 external, 103 internal	Two 10-channel 10-bit	-40 to 125	Dedicated 3-phase motor control timer with accelerator features, features for SIL level achievement	
Up to 1-Mbyte Flash, 60-kbyte RAM	4-channel DMA		64-176 LQFP	16-bit, watchdog, PWM	UART, CSI, I ² C, LIN, CAN, FCAN	up to 17 external, 101 internal	up to 48-channel, 10-bit ADC	-40 to +125	Up to five built-in CAN controllers, POC, LVI	
Up to 256-kbyte Flash, 16-kbyte RAM			64-100 LQFP	16-bit, watchdog, PWM	UART, CSI, I ² C, LIN, CAN	up to 12 external, 42 internal	up to 16-channel, 10-bit	-40 to +125	POC, LVI	

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NEC Electronics America www.am.necel.com	V850ES/Hx2	NEC V850	20	16/16	32, 16	3.5 to 5.5	40 mA (5V)	Halt, idle1, idle2, sub, sub-idle, stop; 6uA	16x16		
NEC Electronics America www.am.necel.com	V850ES/Hx3	NEC V850	32	16/16	32, 16	3.3 to 5.5	40 mA	Halt, Idle1/2, Sub-clock, Sub-Idle, Stop; 10.5uA	16 x16 -> 32; 32 x 32 -> 64		
NEC Electronics America www.am.necel.com	V850ES/IE2	NEC V850	32		32, 16	3.5 to 5.5	55 mA (5V)	Halt, Idle, Stop	16X16, 32x32		
NEC Electronics America www.am.necel.com	V850ES/Jx2	NEC V850	20	24/16	32, 16	2.85 to 3.6	30 mA (3V)	Halt, idle1, idle2, sub, sub-idle, stop; 6uA	16x16		
NEC Electronics America www.am.necel.com	V850ES/Jx3	NEC V850	32	24/16	32, 16	2.85 to 3.6	40 mA	Halt, Idle1/2, Sub-clock, Sub-Idle, Stop; 8uA	16 x16 -> 32; 32 x 32 -> 64		
NEC Electronics America www.am.necel.com	V850ES/Jx3-H	NEC V850	48	24/16	32, 16	2.85 to 3.6	60 mA	Halt, Idle1/2, Sub-clock, Sub-Idle, Stop; 10uA	16 x16 -> 32; 32 x 32 -> 64		
NEC Electronics America www.am.necel.com	V850ES/Jx3-L	NEC V850	20	22/16	32, 16	2.2 to 3.6	12 mA	Halt, Idle1/2, Sub-clock, Sub-Idle, Stop; 1.5uA	16 x16 -> 32; 32 x 32 -> 64		
NEC Electronics America www.am.necel.com	V850ES/Kx2	NEC V850	20	24/16	32, 16	2.7 to 5.5	55 mA (5V)	Halt, idle, sub, sub-idle, stop, 0.1uA	16x16		
NEC Electronics America www.am.necel.com	V850ES/Sx3	NEC V850	32	24/16	32, 16	3.0 to 3.6	57 mA	Halt, idle1, idle 2, sub-idle, stop 9uA	16x16		
NEC Electronics America www.am.necel.com	V850ESJx3-U	NEC V850	48	24/16	32, 16	2.85 to 3.6	60 mA	Halt, Idle1/2, Sub-clock, Sub-Idle, Stop; 10uA	16 x16 -> 32; 32 x 32 -> 64		
NXP Semiconductors www.nxp.com/microcontrollers	LPC2000, LH7 (BlueStreak)	ARM7	85	23/32	16, 32 Thumb/ARM	1.8/3.3	< 100 mW	Idle, powerdown, <1 uA	32X32 multiply and MAC		8-kbyte
NXP Semiconductors www.nxp.com/microcontrollers	LPC2900	ARM968	80	24/32	32	1.8/3.3		Idle, powerdown, <1 uA	32X32 multiply and MAC		16-kbyte instruction/data tightly coupled memories
NXP Semiconductors www.nxp.com/microcontrollers	LPC3000, LH7A (BlueStreak)	ARM9	266	23/32	32 Thumb/ARM/Java	0.9, 1.2, 1.8/3.3	Less than 100 mW	Idle, sleep, powerdown	Vector Floating Point Processor 32X32 multiply and MAC	SIMD operation. IEEE754, square root and format conversion	32-kbyte instruction/data four-way lockable
Oki Semiconductor www.okisemi.com/us	ML671000	ARM7TDMI	24	23/16	16, 32	3.3	60 mA	Halt, stop	32x8 with 64-bit result		
Oki Semiconductor www.okisemi.com/us	ML674000	ARM7TDMI	33	24/16	16, 32	2.5/3.3	35 mA	Halt, stop	32x8 with 64-bit result		

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
64- to 512-kbyte Flash; 6- to 20-kbyte SRAM	up to 4-channel DMA		64/100/144 LQFP, 80 TQFP	Watch timer, watchdog, up to 8 16-bit PWM	Up to 4 UART, 3 CSI	15 external, 51 internal	10- to 24-channel 10-bit	-40 to +85	POC, LVI, CLM	\$5.00 to \$9.00
128-kbyte to 512-kbyte Flash; 8 to 32-kbyte RAM	4-channel DMA		64/80100/144-LQFP	up to 9 16-bit, 14 16-bit PWM, watchdog	UART/LIN, CSI, I ² C	up to 15 external, 63 internal	up to 24-channel 10-bit	-40 to +85	POC, LVI, CLM, CRC	
64- to 128-kbyte Flash			LQFP	6-channel 16-bit, 6-Phase 16-bit for motor control PWM, watchdog,	UART, CSI	42 maskable, non-maskable	Two four-channel 10-bit	-40 to +85	POC, LVI	\$5.50 to \$7.00
128- to 640-kbyte Flash, 12- to 48-kbyte SRAM	4-channel DMA		100/144 LQFP, 100 QFP	Watch timer, watchdog, up to 12 16-bit PWM	Up to 4 UART, 5 CSI, 2 I ² C	9 external, 60 internal	12- to 16-channel 10-bit; two-channel 8-bit DAC	-40 to +85	LVI, CLM	\$6.50 to \$11.00
384-kbyte to 1-Mbyte Flash; 32 to 60-kbyte RAM	4-channel DMA		100/144-LQFP	up to 11 16-bit, 12 16-bit PWM, watchdog	UART/LIN, CSI, I ² C	9 external, 60 internal	up to 16-channel 10-bit; 2-channel 8-bit DAC	-40 to +85	LVI, CLM, CRC	
256/384/512-kbyte Flash; 40/48/56-kbyte RAM	4-channel DMA		100/128-LQFP	13 16-bit, realtime, watchdog, 12 16-bit PWM	USB2.0 Function, UART/LIN, CSI, I ² C	20 external, 69 internal	12-channel 10-bit; 2-channel 8-bit DAC	-40 to +85	LVI, CLM, CRC	
128/256-Mbyte Flash; 8/16-kbyte RAM	4-channel DMA		80/100-LQFP	Eight 16-bit, watchdog, nine 16-bit PWM	UART/LIN, CSI, I ² C	8 external, 47 internal	up to 12-channel 10-bit; 2-channel 8-bit DAC	-40 to +85	LVI, CLM, CRC	
128- to 256-kbyte Flash, 4- to 16-kbyte SRAM			64/100/144 LQFP, 80/100 QFP	Watch timer, 2 watchdog, up to 7 16-bit, 5 8-bit PWM	Up to 4 UART, 5 CSI, I ² C	9 external, 47 internal	Eight 10-bit; two 8-bit DAC	-40 to +85		\$5.00 to \$7.00
256-kbyte to 1-Mbyte Flash, 24- to 60-kbyte RAM	4-channel		100/144 QFP	16-bit, PWM, watchdog	UART, CSI, I ² C, CAN, (IEBus)	8 or 9 external, 51 to 68 internal	12- to 16-channel, 10-bit	-40 to +85	Low-voltage indicator, D/A converter, key return	
384/512-kbyte Flash; 48/56-kbyte RAM	4-channel DMA		100/128-LQFP	13 16-bit, realtime, watchdog, 12 16-bit PWM	USB2.0 Host/Function, UART/LIN, CSI, I ² C	20 external, 69 internal	12-channel 10-bit; 2-channel 8-bit DAC	-40 to +85	LVI, CLM, CRC	
Up to 98-kbyte RAM, up to 1-Mbyte Flash	DMA, NOR, DRAM, SRAM,	Yes on LH795xx series	48 to 208 QFP, BGA	Up to 6 with Match and Capture, PWM, realtime, watchdog	USB FS & HS, Ethernet, CAN, SPI, I ² C, SD Card, SSP, UARTs, I ² S, etc.	Up to 32, four external	Up to 16-channel, 10-bit ADC and 10-bit DACs	-40 to +125 -40 to +105 -40 to +85	Zero-wait-state 128-bits wide Flash with 8-bit ECC, Ethernet, LCD, USB-OTG, On-chip Real-Time Monitor, Real-Time Trace interface.	From \$1.47
Up to 48-kbyte RAM, up to 768 Kbyte Flash	NOR Flash, SRAM		100 to 144 LQFP	4 x 6-channel PWM plus 4x 32-bit timers each with four capture-and-compare register, 32-bit watchdog	2 x 16C550 UARTs, 3 x SPIs, Up to 6 x CAN 2.0B controllers, 2 x LIN 2.0 master controllers	Up to 32, four external	Two 10-bit, 8-channel ADCs	-40 to +85	Reset Generator, Clock-Generation, and Power Management units, clock frequency and power of individual modules. 0.4 MHz ring oscillator. ARM test and debug interface with real-time in-circuit emulator. Boundary-scan test supported	From \$6.79
64-kbyte RAM in addition to caches, 16-kbyte Boot loader ROM.	DMA. Single-level and Multi-level NAND Flash, SDRAM and DDR1 Mobile DRAM.	Full MMU, Linux/WinCE port available	256 LFBGA, 256 BGA, 320 BGA	32-bit with match and capture, OS Timer, watchdog, realtime with separate power domain	Seven UARTs, SPI, I ² C, USB, SD Card, GPIO, Keyboard	Up to 60, over 20 external	10-bit SAR	-40 to +105 -40 to +85	LCD, Ethernet, 6-kbyte emulation trace buffer, standard E-ICE JTAG interface.	From \$7
4-kbyte SRAM	SRAM, DRAM, MASK ROM, Flash, DMA		128 QFP	Multifunction, PWM, watchdog	Rx/Tx UART, 16550 UART, USB 2.0 device with PHY, 64 GPIO	13, nine external		-10 to +70		\$6.50
8-kbyte SRAM, up to 4-kbyte boot ROM	SRAM, DRAM, SDRAM, EDO-DRAM, MASK ROM, Flash, DMA		128 TQFP, 144 LFBGA	Multifunction, PWM, watchdog	16550 UART, RX/TX UART, 32 GPIO	18, five external	Eight-channel, 10 bit	-40 to +85	Selectable clock gears	From \$4

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Oki Semiconductor www.okisemi.com/us	ML674001 ML67Q4002 ML67Q4003	ARM7TDMI	33	24/16	16, 32	2.5/3.3	40 mA	Halt, stop	32x8 with 64-bit result		
Oki Semiconductor www.okisemi.com/us	ML675001 ML67Q5002 ML67Q5003	ARM7TDMI	60	24/16	16, 32	2.5/3.3	70 mA	Halt, stop	32x8 with 64-bit result		8-kbyte unified, four-way set associative, write back
Oki Semiconductor www.okisemi.com/us	ML67Q4050 ML67Q4051	ARM7TDMI	33.33	23/ 8, 16, 32	16, 32	2.5/2.5 to 3.3	50 mA	Halt, stop, clock gears	32x8 with 64-bit result		
Oki Semiconductor www.okisemi.com/us	ML67Q4060 ML67Q4061	ARM7TDMI	33.33		16, 32	2.5/2.5 to 3.3	50 mA	Halt, stop, clock gears	32x8 with 64-bit result		
Oki Semiconductor www.okisemi.com/us	ML696201 ML696Q6203	ARM946E	120	23/16, 8 memory mapped I/O	16, 32	1.5/3.3	200 mA	Halt, stop, clock gears	32x16 with 64-bit result		8-kbyte instruction/data
PMC-Sierra www.pmc-sierra.com	MSP2006	MIPS 32	167	32	32	1.8/3.3	600 mW	Powerdown			32-kbyte instruction/data, four-way set associative, line-lockable
PMC-Sierra www.pmc-sierra.com	MSP2020	MIPS 32	167	32	32	1.8/3.3	1.3W	Powerdown			16-kbyte instruction/data, four-way set associative, line-lockable
PMC-Sierra www.pmc-sierra.com	MSP4120	MIPS 32	167	32	32	1.8/3.3	1.22W	Powerdown	MAC/MAD/MADU, multiply (three-operand and cycle)		16-kbyte instruction/data, four-way set associative, line-lockable
PMC-Sierra www.pmc-sierra.com	MSP4200	MIPS 32	167	32	32	1.8/3.3	1.22W	Powerdown	MAC/MAD/MADU, multiply (three-operand and cycle)		16-kbyte instruction/data, four-way set associative, line-lockable
PMC-Sierra www.pmc-sierra.com	MSP8110	MIPS 32	400	32/64	32	1.0	1.5W	Standby	High performance Multiply/Divide Unit; single cycle repeat rate for 32x32 MAC		64-kbyte instruction/data, four-way set associative, line-lockable
PMC-Sierra www.pmc-sierra.com	MSP8120	MIPS 32	400	32/64	32	1.0	1.5W	Standby	High performance Multiply/Divide Unit; single cycle repeat rate for 32x32 MAC		64-kbyte instruction/data, four-way set associative, line-lockable

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
32-kbyte SRAM, up to 512-kbyte Flash, up to 4-kbyte boot ROM	SRAM, DRAM, SDRAM, EDO-RAM, MASK ROM, Flash, DMA		144 LQFP, 144 LFBGA	Multifunction, PWM, watchdog	16550 UART, RX/TX UART, SSIO, I ² C, 42 GPIO	24, five external	Four-channel, 10-bit	-40 to +85	Selectable clock gears	From \$4
32-kbyte SRAM, up to 512-kbyte Flash, up to 4-kbyte boot ROM	SRAM, DRAM, SDRAM, EDO-RAM, MASK ROM, Flash, DMA		144 LQFP, 144 LFBGA	Multifunction, PWM, watchdog	16550 UART, RX/TX UART, SSIO, I ² C, 42 GPIO	24, five external	Four-channel 10-bit	-40 to +85	Selectable clock gears, PLL	From \$5
16-kbyte SRAM, 64- or 128-kbyte Flash	SRAM, MASK ROM, Flash, PSDRAM, DMA, 23-bit address, 8/16/32-bit data		144 LQFP	Eight, system, watchdog, six multifunction, PWM, real-time, auto reload, input capture, output compare	Two 16550 UART with FIFO and 9-bit support, multimaster I ² C (or SIO), two SPI with FIFO, I ² S with FIFO, up to 108 GPIO	41, five external, external FIQ	Four-channel, 10-bit	-40 to +85	Selectable clock gears, PLL, 2.5V Core and I/O operation, direct CODEC interfaces, ring oscillator, debug with boundary scan and JTAG	From \$5
16-kbyte SRAM, 64- or 128-kbyte Flash	DMA		64 WCSP, 64 TQFP, 84 LFBGA	Eight, system, watchdog, six multifunction, PWM, real-time, auto reload, input capture, output compare	Two 16550 UART with FIFO and 9-bit support, multimaster I ² C (or SIO), two SPI with FIFO, I ² S with FIFO, up to 40 GPIO	32, five external, external FIQ	Four-channel, 10-bit	-40 to +85	Selectable clock gears, PLL, 2.5V Core and I/O operation, direct CODEC interfaces, ring oscillator, debug with boundary scan and JTAG	From \$4
128-kbyte SRAM, 16-kbyte boot, 0- or 512-kbyte Flash	SRAM, Flash, SDRAM, EDO, MASK ROM, PSDRAM; 8-bit mem mapped I/O		272 LFBGA	Six, three flexible, PWM, system, real-time, watchdog	USB 2.0 HS device with PHY, single master I ² C, I ² S, two SSIO, up to 88 GPIO	23 internal, five external	Four-channel, 10-bit	-30 to +70	IDE Controller UDMA66, NAND Flash Controller, External/Internal DMA	From \$12.50
16-kbyte SRAM	133MHz, 32-bit SDRAM, glueless interface for up to 256-Mbyte SDRAM	Fixed mapping (Included in the MIPS core)	276 LFBGA	Three independent programmable 32-bit, watchdog	Two UART, TDM, 32-bit, 33-MHz-compliant PCI, 55 GPIO	Six		-45 to +85	Two-wire, block copy engine, ELB bus, EJTAG debugger	\$6
16-kbyte SRAM Scratchpad	133MHz, 32-bit SDRAM, glueless interface for up to 256-Mbyte SDRAM	Fixed mapping (Included in the MIPS core)	276 BGA	Three independent programmable 32-bit, watchdog	Two UART, TDM, 32-bit, 33-MHz-compliant PCI, SPI, MPI, 55 GPIO	Six		-45 to +85	Two-wire, block copy engine, ELB bus, Security Engine (ESP, DES/3DES core, random number generator), EJTAG debugger	\$10
DSP on-chip memory: 80 Kwords (16-bit) of instruction and data SRAM	133MHz, 32-bit SDRAM, glueless interface for up to 256-Mbyte SDRAM	Fixed mapping (Included in the MIPS core)	289 BGA	Three independent programmable 32-bit, watchdog	Two UART, TDM, SPI, MPI, 16 GPIO	Four		0 to +70	Two-wire, block copy engine, ELB bus, IOM2 support, GCI support, EJTAG debugger	\$8.30
DSP on-chip memory: 80 Kwords (16-bit) of instruction and data SRAM	133MHz, 32-bit SDRAM, glueless interface for up to 256-Mbyte SDRAM	Fixed mapping (Included in the MIPS core)	289 BGA	Three independent programmable 32-bit, watchdog	Two UART, TDM, PCI 2.2 compatible, SPI, MPI, 16 GPIO	Four		0 to +70	Two-wire, block copy engine, ELB bus, IOM2 support, GCI support, EJTAG debugger	\$9
32-kbyte SRAM Scratchpad	166MHz, DDRI/DDR II SDRAM	32 dual-entry TLB	416 PBGA	Two independent programmable 32-bit, watchdog	Two UART, TDM, 32-bit 66-MHz-compliant PCI, SPI, MPI, 2 MII/RMII, USB 2.0, 2 TWI, 20 GPIO	Eight		-40 to +85	Two-wire, block copy engine, ELB bus, EJTAG debugger	\$18
32-kbyte SRAM Scratchpad	166MHz, DDRI/DDR II SDRAM	32 dual-entry TLB	416 PBGA	Two independent programmable 32-bit, watchdog	Two UART, TDM, 32-bit 66-MHz-compliant PCI, SPI, MPI, 2 MII/RMII, USB 2.0, 2 TWI, 20 GPIO	Eight		-40 to +85	Two-wire, block copy engine, ELB bus, EJTAG debugger, Security Engine (MD5, SHA01, DES/3DES core, IPsec compliant, RNG)	\$19

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Renesas Technology www.renesas.com	M32C/85	M16C	32	24/16	16	3 to 5.5		Four modes	16x16 multiply		
Renesas Technology www.renesas.com	M32C/87A	M16C	32	24/16	16	3 to 5.5		Four modes	16x16 multiply		
Renesas Technology www.renesas.com	M32C/87B	M16C	32	24/16	16	3 to 5.5		Four modes	16x16 multiply		
Renesas Technology www.renesas.com	M33C/80	M16C	32	24/16	16	3 to 5.5		Four modes	16x16 multiply		
Renesas Technology www.renesas.com	H8X/1582 (H8SX)	H8X	48	32/32	8, 16, 32	4.5 to 5.5		Five modes	8x8, 16x16 32x32 multiply, 16x16+32, 16x16+42		
Renesas Technology www.renesas.com	H8X/1622 (H8SX)	H8X	50	32/32	8, 16, 32	3 to 3.6		Five modes	8x8, 16x16 32x32 multiply, 16x16+32, 16x16+42		
Renesas Technology www.renesas.com	H8X/1638 (H8SX)	H8X	50	32/32	8, 16, 32	3 to 3.6		Five modes	8x8, 16x16 32x32 multiply, 16x16+32, 16x16+42		
Renesas Technology www.renesas.com	H8X/1648 (H8SX)	H8X	50	32/32	8, 16, 32	3 to 3.6		Five modes	8x8, 16x16 32x32 multiply, 16x16+32, 16x16+42		
Renesas Technology www.renesas.com	H8X/1650 (H8SX)	H8X	50	32/32	8, 16, 32	3 to 3.6		Six modes	8x8, 16x16 32x32 multiply, 16x16+32, 16x16+42		
Renesas Technology www.renesas.com	H8X/1651 (H8SX)	H8X	50	32/32	8, 16, 32	3 to 3.6		Six modes	8x8, 16x16 32x32 multiply, 16x16+32, 16x16+42		
Renesas Technology www.renesas.com	H8X/1657 (H8SX)	H8X	35	32/32	8, 16, 32	3 to 3.6		Six modes	8x8, 16x16 32x32 multiply, 16x16+32, 16x16+42		
Renesas Technology www.renesas.com	H8X/1658R (H8SX)	H8X	50	32/32	8, 16, 32	3 to 3.6		Seven modes	8x8, 16x16 32x32 multiply, 16x16+32, 16x16+42		
Renesas Technology www.renesas.com	H8X/1668R (H8SX)	H8X	50	32/32	8, 16, 32	3 to 3.6		Five modes	8x8, 16x16 32x32 multiply, 16x16+32, 16x16+42		
Renesas Technology www.renesas.com	M32C/83	M16C	32	24/16	16	3 to 5.5		Four modes	16x16 multiply		
Renesas Technology www.renesas.com	M32C/84	M16C	32	24/16	16	3 to 5.5		Four modes	16x16 multiply		

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
320-kbyte,384-kbyte, 512-kbyte Flash, 24-kbyte RAM	4		100 QFP, 144 LQFP	Eleven 16-bit, watchdog	5 Serial,5 I2C,2 CAN, 124 GPIO	8	34-channel 10-bit,2-channel 8-bit DAC	-20 to 85	X-Y converter, 3-phase PWM, CRC, DMAC II, 5-ch IEBus, Intelligent IO (8-ch 16-bit IC; 8-ch 16-bit OC; HDLC)	\$17.50
384-kbyte, 512-kbyte, 768-kbyte, 1024-kbyte Flash, 24-kbyte, 31-kbyte, 48-kbyte RAM	4		100 QFP, 100 LQFP, 144LQFP	Eleven 16-bit, watchdog	7 Serial,IrDA,5 I2C, CAN, 124 GPIO	11	34-channel 10-bit,2-channel 8-bit DAC	-20 to 85	X-Y converter, 3-phase PWM, CRC, DMAC II, 5-ch IEBus, Intelligent IO (8-ch 16-bit IC; 16-ch 16-bit OC; HDLC)	\$16.43
384-kbyte,512-kbyte, 768-kbyte, 102-kbyte Flash, and 24-kbyte, 31-kbyte, 48-kbyte RAM	4		100 LQFP, 100 QFP,144LQFP	Eleven 16-bit, watchdog	7 Serial,IrDA,5 I2C,124 GPIO	11	34-channel 10-bit,2-channel 8-bit DAC	-20 to 85	X-Y converter, 3-phase PWM, CRC, DMAC II, 5-ch IEBus, Intelligent IO (8-ch 16-bit IC; 16-ch 16-bit OC; HDLC)	\$16.08
ROMless, 8-kbyte RAM	4		100 QFP 100LQFP	Eleven 16-bit, watchdog	5 Serial,5 I2C, 48 GPIO	8	10-channel 10-bit, 2-channel 8-bit DAC	-20 to 85	X-Y converter, 3-phase PWM, CRC, DMAC II, 2-ch HDLC, 5-ch IEBus, External ROM version with built-in Boot loader	\$5.25
256-kbyte Flash, 12-kbyte RAM	4		120 LQFP	Twelve 16-bit, watchdog, 8-bit waveform generator	2 Serial,3 SSU, Samrt Card, DTC, 99 GPIO	17	16-channel 10-bit	-20 to 85		\$14.29
256-kbyte Flash, 24-kbyte RAM	2		145 TFLGA, 144LQFP	Four 8-bit, Six 16-bit, watchdog, 16-bit Waveform generator	5 Serial,Smart Card, 2 I2C, DTC, 91 GPIO	17	8-channel 10-bit, 2-channel 8-bit DAC	-40 to 85	UBC, 6-ch 16-bit Sigma-Delta ADC	\$8.75
256-kbyte, 512-kbyte, 1024-kbyte Flash and 24-kbyte, 40-kbyte, 56-kbyte RAM	4		120 LQFP	Eight 8-bit, Twelve 16-bit, watchdog, 32-bit Waveform Generator	7 Serial,IrDA,Smart Card,2 I2C, DTC, 91 GPIO	17	8-channel 10-bit, 2-channel 8-bit DAC	-20 to 75	UBC, Boundary scan	\$9.88
256-kbyte, 512-kbyte, 1024-kbyte Flash, 24-kbyte, 40-kbyte and 56-kbyte RAM	4		144 LQFP	Eight 8-bit, Twelve 16-bit, watchdog, 32-bit Waveform Generator	7 Serial, IrDA,Smart Card,4 I2C, DTC,110 GPIO	17	12-channel 10-bit, 2-channel 8-bit DAC	-20 to 75	UBC, Boundary scan	\$10.48
ROMless, 24-kbyte RAM			120 LQFP	Four 8-bit, Six 16-bit, watchdog, 16-bit Waveform generator	4 Serial, Smart Card, DTC,90 GPIO	13	8-channel 10-bit, 2-channel 8-bit DAC	-40 to 85	HSS	\$4.83
ROMless, 40-kbyte RAM	4		120 LQFP	Four 8-bit, Six 16-bit, watchdog, 16-bit Waveform generator	4 Serial, IrDA, Smart Card, DTC,90 GPIO	13	8-channel 10-bit, 2-channel 8-bit DAC	-20 to 75	HSS	\$5.24
512-kbyte, 768-kbyte Flash, 24-kbyte RAM	4		120 TQFP	Four 8-bit, Six 16-bit, watchdog, 16-bit Waveform generator	4 Serial, Smart Card DTC,,90 GPIO	13	8-channel 10-bit, 2-channel 8-bit DAC	-40 to 85	HSS	\$12.77
384-kbyte, 512-kbyte, 1024-kbyte Flash, 40-kbyte, 56-kbyte RAM	4		120 TQFP	Eight 8-bit, Twelve 16-bit, watchdog, 16-bit Waveform Generator	6 Serial, IrDA,Smart Card,2 I2C, DTC,84 GPIO	13	12-channel 10-bit, 2-channel 8-bit DAC	-20 to 75	CRC, HSS, USB, 4-ch EXDMAC	\$10.48
384-kbyte, 512-kbyte, 1024-kbyte Flash, 40-kbyte, 56-kbyte RAM	4		176 LFBGA 144 LQFP	Eight 8-bit, Twelve 16-bit, watchdog, 32-bit Waveform Generator	6 Serial, IrDA,Smart Card,2 I2C, DTC,101 GPIO	13	12-channel 10-bit, 2-channel 8-bit DAC	-20 to 75	UBC, USB, 24-bit Subclock Timer (TM32K), Boundary Scan, 4-ch EXDMAC	\$11.08
512-kbyte Flash, 31-kbyte RAM	4		100 QFP, 100 LQFP, 144 LQFP	Eleven 16-bit, watchdog	5 Serial,5 I2C,CAN, 124 GPIO	8	34-channel 10-bit,2-channel 8-bit DAC	-20 to 85	Two ADC circuits, X-Y converter, 3-phase PWM, CRC, DMAC II, DRAMC, 5-ch IEBus, Intelligent IO (12-ch 16-bit IC; 28-ch 16-bit OC; HDLC)	\$26.06
ROMless, 320-kbyte,384-kbyte, 512-kbyte Flash, 10-kbyte and 24-kbyte RAM	4		100 QFP, 100 LQFP, 144 LQFP	Eleven 16-bit, watchdog	5 Serial,5 I2C,CAN, 124 GPIO	8	34-channel 10-bit,2-channel 8-bit DAC	-20 to 85	X-Y converter, 3-phase PWM, CRC, DMAC II, 5-ch IEBus, Intelligent IO (8-ch 16-bit IC; 8-ch 16-bit OC; HDLC)	\$16.88

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Renesas Technology www.renesas.com	M32C8A	M16C	32	24/16	16	3 to 5.5		Four modes	16x16 multiply		
Renesas Technology www.renesas.com	M32C87	M16C	32	24/16	16	3 to 5.5		Four modes	16x16 multiply		
Renesas Technology www.renesas.com	R32C/111 R32C/100 Series	M16C	50	32/64	32	3.0 to 5.5	32 mA	Three modes; 5.0 uA	32x32+64	Single-precision	64-byte instruction buffer
Renesas Technology www.renesas.com	R32C/116 R32C/100 Series	M16C	50	32/64	32	3.0 to 5.5	32 mA	Three modes; 5.0 uA	32x32+64	Single-precision	64-byte instruction buffer
Renesas Technology www.renesas.com	R32C/117 R32C/100 Series	M16C	50	32/64	32	3.0 to 5.5	32 mA	Three modes; 5.0 uA	32x32+64	Single-precision	64-byte instruction buffer
Renesas Technology www.renesas.com	R32C/118 R32C/100 Series	M16C	50	32/64	32	3.0 to 5.5	32 mA	Three modes; 5.0 uA	32x32+64	Single-precision	64-byte instruction buffer
Renesas Technology www.renesas.com	SH-2 Series SH7147	SuperH	80	32/32	16	4.5 to 5.5		Five modes	32x32+64		
Renesas Technology www.renesas.com	SH-2 Series SH7047F	SuperH	50	32/32	16	4.5 to 5.5	220 mA	Four modes	32x32+64		
Renesas Technology www.renesas.com	SH-2 Series SH7083F	SuperH	80	32/32	16	3.0 to 3.6/ 4.5 to 5.5		Four modes	32x32+64		
Renesas Technology www.renesas.com	SH-2 Series SH7084F	SuperH	80	32/32	16	3.0 to 3.6/ 4.5 to 5.5		Four modes	32x32+64		
Renesas Technology www.renesas.com	SH-2 Series SH7085F	SuperH	80	32/32	16	3.0 to 3.6/ 4.5 to 5.5		Four modes	32x32+64		
Renesas Technology www.renesas.com	SH-2 Series SH7086F	SuperH	80	32/32	16	3.0 to 3.6/ 4.5 to 5.5		Four modes	32x32+64		
Renesas Technology www.renesas.com	SH-2 Series SH7124F	SuperH	50	32/32	16	4.0 to 5.5		Four modes	32x32+64		
Renesas Technology www.renesas.com	SH-2 Series SH7125F	SuperH	50	32/32	16	4.5 to 5.5		Four modes	32x32+64		
Renesas Technology www.renesas.com	SH-2 Series SH7144F	SuperH	50	32/32	16	3 to 3.6	160 mA	Three modes	32x32+64		

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
ROMless, 12-kbyte RAM	4		100 LQFP	Eleven 16-bit, watchdog	5 Serial, 5 I2C, 46 GPIO	11	10-channel 10-bit, 2-channel 8-bit DAC	-20 to 85	X-Y converter, 3-phase PWM, Cold/Warm Start-Up Detect, CRC, DMAC II, 5-ch IEBus	\$5.00
384-kbyte, 512-kbyte, 768-kbyte, 1024-kbyte Flash, 24-kbyte, 34-kbyte, 48-kbyte RAM	4		100 QFP, 100LQFP, 144 LQFP	Eleven 16-bit, watchdog	7 Serial, IrDA, 5 I2C, 2 CAN, 124 GPIO	11	34-channel 10-bit, 2-channel 8-bit DAC	-20 to 85	X-Y converter, 3-phase PWM, CRC, DMAC II, 5-ch IEBus, Intelligent IO (8-ch 16-bit IC; 16-ch 16-bit OC; HDLC)	\$16.79
256- to 512-kbyte Flash, 31- to 63-kbyte RAM, 8-kbyte data Flash	four-channel DMAC, single-channel DMA-II		64, 100 LQFP	Eleven 16-bit, watchdog, 24-channel IC/OC	I ² C, IEBus, SPI, Nine (a)synchronous, up to 86 GPIO	11 external	26-channel 10-bit; 2-channel 8-bit DAC	-40 to +85	External Bus Expansion, three-phase motor controller, clock stop detect, power-on reset, low voltage detect, CRC block, X-Y converter	\$5.00 to \$5.80
384-kbyte to 1-Megabyte Flash, 40- to 63-kbyte RAM, 8-kbyte data Flash	four-channel DMAC, single-channel DMA-II		100, 144 LQFP	Eleven 16-bit, watchdog, 24-channel IC/OC	Multi-master I ² C, IEBus, SPI, Nine (a)synchronous, up to 122 GPIO	11, 14 external	26- to 34-channel 10-bit; 2-channel 8-bit DAC	-40 to +85	External Bus Expansion, three-phase motor controller, clock stop detect, power-on reset, low voltage detect, CRC block, X-Y converter	\$5.40 to \$7.40
384-kbyte to 1-Megabyte Flash, 40- to 63-kbyte RAM, 8-kbyte data Flash	four-channel DMAC, single-channel DMA-II		100, 144 LQFP	Eleven 16-bit, watchdog, 24-channel IC/OC	Multi-master I ² C, IEBus, SPI, Nine (a)synchronous, up to 122 GPIO	11, 14 external	26- to 34-channel 10-bit; 2-channel 8-bit DAC	-40 to +85	External Bus Expansion, three-phase motor controller, clock stop detect, power-on reset, low voltage detect, 1-channel CAN, CRC block, X-Y converter	\$8.25 to \$11.10
384-kbyte to 1-Megabyte Flash, 40- to 63-kbyte RAM, 8-kbyte data Flash	four-channel DMAC, single-channel DMA-II		100, 144 LQFP	Eleven 16-bit, watchdog, 24-channel IC/OC	Multi-master I ² C, IEBus, SPI, Nine (a)synchronous, up to 122 GPIO	11, 14 external	26- to 34-channel 10-bit; 2-channel 8-bit DAC	-40 to +85	External Bus Expansion, three-phase motor controller, clock stop detect, power-on reset, low voltage detect, 2-channel CAN, CRC block, X-Y converter	\$9.00 to \$11.50
256-kbyte, 512-kbyte Flash, 16-kbyte RAM			100 LQFP	Ten 16-bit, watchdog	3 Serial, SSU, CAN, DTC, 73 GPIO	5	16-channel 12-bit ADC	-40 to 85	Two ADC circuits, 5-ch 16-bit MTU2, 3-ch 16-bit MTU2S, Port Output Enable, 2-ch CMT, UBC, AUD	
256-kbyte Flash, 12-kbyte RAM	SRAM, ROM		100 QFP	7 16-bit timers, 6-phase Motor Management, watchdog, Up to 12 PWM	3 (a)synchronous, CAN, 53 I/O, 16 Input only	8 external	2 eight-channel, 10-bit	-40 to +85	Data-transfer controller, on-chip debug	\$13.35
512-kbyte Flash, 32-kbyte RAM	4-channel DMAC, SRAM, ROM, SDRAM		100 TQFP	11 16-bit, watchdog, Up to 12 PWM	4 (a)synchronous, SPI-compatible, 65 I/O, 8 Input only	9 external	2 eight-channel, 10-bit	-40 to +85	Data-transfer controller, on-chip debug	\$13.99
512-kbyte Flash, 32-kbyte RAM	4-channel DMAC, SRAM, ROM, SDRAM		112 LQFP	11 16-bit, watchdog, Up to 12 PWM	4 (a)synchronous, SPI-compatible, I ² C, 76 I/O, 8 Input only	9 external	2 eight-channel, 10-bit	-40 to +85	Data-transfer controller, on-chip debug	\$14.35
512-kbyte Flash, 32-kbyte RAM	4-channel DMAC, SRAM, ROM, SDRAM		144 LQFP	11 16-bit, watchdog, Up to 12 PWM	4 (a)synchronous, SPI-compatible, I ² C, 100 I/O, 8 input only	9 external	2 eight-channel, 10-bit	-40 to +85	Data-transfer controller, on-chip debug	\$14.55
512-kbyte Flash, 32-kbyte RAM	4-channel DMAC, SRAM, ROM, SDRAM		176 LQFP	11 16-bit, watchdog, Up to 12 PWM	4 (a)synchronous, SPI-compatible, I ² C, 118 I/O, 16 input only	9 external	3 16-channel, 10-bit	-40 to +85	Data-transfer controller, on-chip debug	\$15.48
32, 64, 128-kbyte Flash, 8-kbyte RAM			48 LQFP, 52 VQFN	8 16-bit, watchdog, Up to 12 PWM	3 (a)synchronous, 23 I/O, 8 Input only	4 external	8-channel, 10-bit	-40 to +85	On-chip debug	\$5.10
64, 128-kbyte Flash, 8-kbyte RAM			64 QFP, 64 LQFP, 64 VQFN	8 16-bit, watchdog, Up to 12 PWM	3 (a)synchronous, 37 I/O, 8 Input only	5 external	8-channel, 10-bit	-40 to +85	On-chip debug	\$7.75
256-kbyte Flash, 8-kbyte RAM	4-channel DMAC, SRAM, ROM		112 QFP	7 16-bit, watchdog, Up to 12 PWM	4 (a)synchronous, I ² C, 74 I/O, 8 Input only	9 external	8-channel, 10-bit	-40 to +85	Data-transfer controller, on-chip debug	\$11.90

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Renesas Technology www.renesas.com	SH-2 Series SH7145F	SuperH	50	32/32	16	3 to 3.6	160 mA	Three modes	32x32+64		
Renesas Technology www.renesas.com	SH-2 Series SH7146F	SuperH	80	32/32	16	4.0 to 5.5		Four modes	32x32+64		
Renesas Technology www.renesas.com	SH-2 Series SH7149F	SuperH	80	32/32	16	3.0 to 3.6/ 4.5 to 5.5		Four modes	32x32+64		
Renesas Technology www.renesas.com	SH-2 Series SH7149F	SuperH	80	32/32	16	4.0 to 5.5		Four modes	32x32+64		
Renesas Technology www.renesas.com	SH-2 Series SH7136	SuperH	80	32/32	16	3.0 to 3.6/ 4.5 to 5.5		Four modes	32x32+64		
Renesas Technology www.renesas.com	SH-2 Series SH7137	SuperH	80	32/32	16	3.0 to 3.6/ 4.5 to 5.5		Four modes	32x32+64		
Renesas Technology www.renesas.com	SH-2A Series SH7211F	SuperH	160	32/32	16, 32	1.5/3.3		Three modes	32x32+64		
Renesas Technology www.renesas.com	SH-2A Series SH7211F	SuperH	160	32/32	16, 32	1.5/3.3		Three modes	32x32+64		
Renesas Technology www.renesas.com	SH-2A Series SH7243	SuperH	100	32/32	16	3.0 to 5.5		Three modes	32x32+64		
Renesas Technology www.renesas.com	SH-2A Series SH7285	SuperH	100	32/32	16	3.0 to 3.6/ 4.5 to 5.5		Three modes	32x32+64		
Renesas Technology www.renesas.com	SH-2A Series SH7286	SuperH	100	32/32	16	3.0 to 3.6/ 4.5 to 5.5		Three modes	32x32+64		
Renesas Technology www.renesas.com	SH2A-FPU Series SH7263	SuperH	200	32/32	16, 32	1.2/3.3		Four modes	32x32+64	Single- and double-precision	8-kbyte instruction/ 8K byte operand
Renesas Technology www.renesas.com	SH2A-FPU Series SH7203	SuperH	200	32/32	16, 32	1.2/3.3		Four modes	32x32+64	Single- and double-precision	8-kbyte instruction/data
Renesas Technology www.renesas.com	SH2A-FPU Series SH7670	SuperH	200	32/32	16, 32	1.2/3.3		Four modes	32x32+64	Single- and double-precision	8-kbyte instruction/data
Renesas Technology www.renesas.com	SH2A-FPU Series SH7262	SuperH	144	32/32	16, 32	1.1/3.3		Four modes	32x32+64	Single- and double-precision	8-kbyte instruction/ 8K byte operand

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
256-kbyte Flash, 8-kbyte RAM	4-channel DMAC, SRAM, ROM		144 LQFP	7 16-bit, watchdog, Up to 12 PWM	4 (a)synchronous, I ² C, 98 I/O, 8 Input only	9 external	8-channel, 10-bit	-40 to +85	Data-transfer controller, on-chip debug	\$12.26
256-kbyte Flash, 8-kbyte RAM	SRAM, ROM		80 LQFP	11 16-bit, watchdog, Up to 12 PWM	3 (a)synchronous, 45 I/O, 12 Input only	9 external	3 12-channel, 10-bit	-40 to +85	Data-transfer controller, on-chip debug	\$10.45
256-kbyte Flash, 8-kbyte RAM	SRAM		100 LQFP	11 16-bit, watchdog	Three (a)synchronous	9 external	Triple 12-channel, 10-bit	-40 to +85	Data-transfer controller, on-chip debug	\$8.09
256-kbyte Flash, 8-kbyte RAM	SRAM, ROM		100 LQFP, 100 QFP	11 16-bit, watchdog, Up to 12 PWM	3 (a)synchronous, 63 I/O, 12 Input only	9 external	3 12-channel, 10-bit	-40 to +85	Data-transfer controller, on-chip debug	\$10.24
256-kbyte Flash, 16-kbyte RAM	SRAM, ROM		80 LQFP	11 16-bit, watchdog, Up to 12 PWM	3 (a)synchronous, 3 SPI, I ² C, CAN, 44 I/O, 12 Inputs only	5 external	2 6-channel with 3 S/H each, 12-bit	-40 to +85	On-chip debug	\$12.45
256-kbyte Flash, 16-kbyte RAM	SRAM, ROM		100 LQFP	11 16-bit, watchdog, Up to 12 PWM	3 (a)synchronous, 3 SPI, I ² C, CAN, 57 I/O, 16 Inputs only	5 external	2 8-channel with 3 S/H each, 12-bit	-40 to +85	On-chip debug	\$11.90
512-kbyte Flash, 32-kbyte RAM	SRAM, ROM, SDRAM, eight-channel DMAC		144 LQFP	8 16-bit, watchdog	I ² C, four (a)synchronous	9 external	Eight-channel 12-bit; two-channel, 8-bit DAC	-20 to +85	On-chip debug	\$17.00
512-kbyte Flash, 32-kbyte RAM	8-channel DMAC, SRAM, ROM, SDRAM		144 LQFP	11 16-bit, watchdog, Up to 12 PWM	4 (a)synchronous, I ² C, 75 I/O	9 external	8-channel 12-bit; 2-channel, 8-bit DAC	-20 to +85	On-chip debug	\$17.69
128/256-kbyte Flash, 8/12-kbyte RAM	8-channel DMAC, SRAM, ROM, SDRAM		100 LQFP	11 16-bit, watchdog, Up to 12 PWM	4 (a)synchronous, SPI, I ² C, USB FS Device, 63 I/O, 8 Inputs only	9 external	8-channel with 3 S/H, 12-bit	-40 to +85	On-chip debug	\$12.20
512/768-kbyte Flash, 24/32-kbyte RAM	8-channel DMAC, SRAM, ROM, SDRAM		114 LQFP	11 16-bit, watchdog, Up to 12 PWM	4 (a)synchronous, 2 SPI, I ² C, USB FS Device, 92 I/O, 12 Inputs only	9 external	8-channel with 3 S/H, 12-bit	-40 to +85	On-chip debug	\$17.15
512/768/1024-kbyte Flash, 24/32-kbyte RAM	8-channel DMAC, SRAM, ROM, SDRAM		176 LQFP	11 16-bit, watchdog, Up to 12 PWM	4 USART, 2 SPI, 1 I ² C, CAN, USB FS Device, 101 I/O, 12 Inputs only	9 external	12-channel with 3 S/H, 12-bit, 2 8-bit DACs	-40 to +85	On-chip debug	\$18.45
32-kbyte RAM	SRAM, ROM, SDRAM, eight-channel DMAC		240 QFP	Multifunction, compare match, RTC, 7 16-bit, watchdog	Four I ² C, six (a)synchronous	17 external	Eight-channel 10-bit; two-channel, 8-bit DAC	-40 to +85	High Speed USB Host, High Speed USB function, SDHC, LCDC, 2-ch CAN, on-chip debug, sample rate converter, CDROM DEC, IE Bus	\$12.35
32-kbyte RAM	SRAM, ROM, SDRAM, eight-channel DMAC		240 QFP	Multifunction, compare match, RTC, 7 16-bit, watchdog	Four I ² C, six (a)synchronous	17 external	Eight-channel 10-bit; two-channel, 8-bit DAC	-40 to +85	High Speed USB Host, High Speed USB function, LCDC, 2-ch CAN, on-chip debug, IE Bus	\$12.35
32-kbyte RAM	SRAM, ROM, SDRAM, eight-channel DMAC		240 QFP	7 16-bit, watchdog	Four I ² C, six (a)synchronous	17 external	Eight-channel 10-bit; two-channel, 8-bit DAC	-40 to +85	USB Host High Speed, USB Function High Speed, Ethernet 10/100, SD, 2-ch sound	\$10.00
1-Mbyte VRAM, 64-kbyte RAM	SRAM, ROM, SDRAM, eight-channel DMAC		176 QFP	Multifunction, compare match, RTC, 7 16-bit, watchdog	Three I ² C, Five (a)synchronous,	17 external	Eight-channel 10-bit; two-channel, 8-bit DAC	-40 to +85	Video/LCDC, , USB host high speed, USB function high speed, SDHC SPI BOOT NOR Flash, bootable NAND, 2-ch CAN, on-chip debug, sample rate converter, CDROM DEC, IE Bus, Serial Sound, SPDIF	\$11.50

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Renesas Technology www.renesas.com	SH2A-FPU Series SH7264	SuperH	144	32/32	16, 32	1.1/3.3		Four modes	32x32+64	Single- and double-precision	8-kbyte instruction/8K byte operand
Renesas Technology www.renesas.com	SH-4A Series SH7763	SuperH	266	32/32	16, 32	1.2/3.3		Three modes	32x32+64	Single- and double-precision	32-kbyte instruction/data, four-way set associative
Renesas Technology www.renesas.com	SH-4A Series SH7780	SuperH	400	32/32	16, 32	1.25/3.3	1.5W	Four modes	32x32+64	Single- and double-precision	32-kbyte instruction/data, four-way set associative
Renesas Technology www.renesas.com	SH-4A Series SH7781	SuperH	400	32/32	16, 32	1.25/3.3		Four modes	32x32+64	Single- and double-precision	32-kbyte instruction/data, four-way set associative
Renesas Technology www.renesas.com	SH-4A Series SH7785	SuperH	600	32/32	16, 32	1.1/3.3		Two modes	32x32+64	Single- and double-precision	32-kbyte instruction/data, four-way set associative
Renesas Technology www.renesas.com	SH4A-FPU Series SH7723	SuperH	400	32/32	128	1.2/3.3	300 mA	Five modes	16x16		32/32-kbyte instruction/operand 256-kbyte mixed instruction/data
Renesas Technology www.renesas.com	SH4-DSP Series SH7722	SuperH	333	32/32	128	1.2/3.3	300 mA	Five modes	16x16		32-kbyte instruction/data
Renesas Technology www.renesas.com	SH-Tiny Series SH7125	SuperH	50	32/32	16	4.5 to 5.5		Four modes	32x32+64		
Samsung Electronics- www.samsungsemi.com	S3C2410	ARM920T	200, 266	27/32	16, 32	1.8/3.3	225 mW (1.8V)	Sleep, idle			16-kbyte instruction/data
Samsung Electronics- www.samsungsemi.com	S3C2412	ARM926EJ-S	200, 266	27/32	16, 32	1.2/(1.8/2.5/3.3)		Normal, idle, stop, power-off	DSP instructions		8-kbyte instruction/data
Samsung Electronics- www.samsungsemi.com	S3C2413	ARM926EJ-S	266	27/32	16, 32	1.2/(1.8/2.5/3.3)		Normal, idle, stop, power-off	DSP instructions		8-kbyte instruction/data
Samsung Electronics- www.samsungsemi.com	S3C2440	ARM920T	300, 400, 533	27/32	16, 32	1.2/1.3/3.3 (1.8/2.5/3.3 memory)		Sleep, idle			16-kbyte instruction/data

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
1-Mbyte VRAM, 64 kbyte RAM	SRAM, ROM, SDRAM, eight-channel DMAC		208 QFP	Multifunction, compare match, RTC, 7 16-bit, watchdog	Three I ² C, six (a)synchronous	17 external	Eight-channel 10-bit; two-channel, 8-bit DAC	-40 to +85	Video/LCDC, , USB host high speed, USB function high speed, SDHC SPI BOOT NOR Flash, bootable NAND, 2-ch CAN, on-chip debug, sample rate converter, CDROM DEC, IE Bus, Serial Sound, SPDIF	\$12.00
16-kbyte RAM	DDR-SDRAM, SRAM, ROM, 6-channel DMAC	Yes	449 BP	10 32-bit, 1 16-bit, real-time	I ² C, Five serial, PCI	33 external	Eight-channel, 10 bit; two-channel, 8-bit DAC	-20 to +75	Dual Gbit Ethernet MAC, LCDC, USB host & function, audio interface, On-chip debug	\$20.80
48-kbyte RAM	DDR-SDRAM, SRAM, ROM, 12-channel DMAC	Yes	449 BP	10 32-bit, real-time	Five serial, PCI	60, 11 external		-40 to +85	On-chip debug	\$30.00
16-kbyte RAM	DDR-SDRAM, SRAM, ROM, 12-channel DMAC	Yes	449 BP	10 32-bit, real-time	Five serial, PCI	60, 11 external		-40 to +85	IPSec, On-chip debug	\$35.00
152-kbyte RAM	DDR2-SDRAM, SRAM, ROM, 12-channel DMAC	Yes	436 BP	Six 32-bit	Six serial, PCI	9 external		-40 to +85	Display unit, On-chip debug	\$38.00
16kbyte RAM	DDR1-SDRAM, SRAM, ROM, 12-channel DMAC	Yes	449 BP	6 32-bit, 16bit pulse unit, 32-bit compare match, 3-channel 32-bit PWM	Serial, 2-ch serial FIFO, 3 ch serial comm, SIM, IRDA, I ² C, USB Host function	9 external		- 20 to +70	Camera video process, video procesing H.264/MPEG4, LCD, 2D graphics engine, NAND, JPEG, SD, transport stream, USB 2.0 host and function High speed, ATAPI, Key-scan, onchip debug	\$20.80
128kbyte RAM	SDRAM	Yes	449 BP	3-channel 32-bit PWM	Serial, 2-ch serial FIFO, 3 ch serial comm, SIM, IRDA, I ² C, USB Host function	9 external		- 20 to +70	Camera video process, video processing, LCD, 2D graphics engine, NAND, JPEG, SD, transport stream, USB host and function High speed, Key-scan, onchip debug	\$17.70
32-kbyte, 64-kbyte, 128-kbyte Flash, 8-kbyte RAM			48 LQFP, 64 LQFP, 64 QFP, 52 VQFN, 64 VQF	Eight 16-bit, watchdog	3 Serial, 45 GPIO	5	8-channel 10-bit	-40 to 85	Two ADC circuits, 6-ch 16 bit MTU2, Port Output Enable, 2-ch CMT, UBC, 15 mA IO	\$7.86
4-kbyte SRAM, NAND booting	4-channel DMC, Flash, SRAM, ROM, SDRAM	Yes	272 FBGA	Four 16-bit	Three UART, two SPI, I ² S, I ² C, two USB host/device	24 external	Eight-channel, 10 bit touchscreen	0 to +70 -40 to +85	STN/TFT LCDC, SD/MMC, SMC	
4-kbyte SRAM, NAND booting	4-channel DMC, Flash, SRAM, ROM, SDRAM	Yes	272 FBGA	Four 16-bit	Three UART, two SPI, I ² S, I ² C, two USB host/device	24 external	Eight-channel, 10 bit touchscreen	0 to +70 -40 to +85	STN/TFT LCDC, SD/MMC, SMC	
4-kbyte SRAM, NAND booting	4-channel DMC, Flash, SRAM, ROM, DDR/SDR	Yes	289 FBGA	Four 16-bit	Three UART, two SPI, I ² S, I ² C, two USB host/device	24 external	Eight-channel, 10 bit touchscreen	0 to +70 -40 to +85	STN/TFT LCDC, 2MP CAMERA, SD/MMC, CF/ATA Interface	
4-kbyte SRAM, NAND booting	4-channel DMC, Flash, SRAM, ROM, SDRAM	Yes	289 FBGA	Four 16-bit	Three UART, two SPI, I ² S, I ² C, AC97, two USB host/device, CF/ATA Interface	24 external	Eight-channel, 10 bit touchscreen	0 to +70 -40 to +85	STN/TFT LCDC, 4MP CAMERA, SD/MMC	

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Samsung Electronics- www.samsungsemi.com	S3C2443	ARM920T	400, 533	26/32	16, 32	1.2/(1.8/2.5/3.3)		Normal, idle, stop, power-off			16-kbyte instruction/data
Samsung Electronics- www.samsungsemi.com	S3C6400	ARM1176JZF	400,533	27(16)/32	16, 32	1.2/(1.8/2.5/3.3)		Normal, idle, stop, deep stop,power-off	SIMD DSP instructions	VFP	16-kbyte instruction/data
STMicroelectronics www.st.com	STM32 ARM Cortex-M3 Flash Microcontrollers	Cortex-M3 Thumb-2	36, 72		16, 32	2 to 3.6	27 mA (72 MHz)	Stop <20uA Standby 2uA	Single cycle multiply and hardware division		
STMicroelectronics www.st.com	STR910FA ARM Flash Microcontrollers	ARM966E-S ARM/Thumb	96	EMI 24-bit Address (3 CS), 16 or 8 bit data	16, 32	2.7 to 3.3 or 3.0 to 3.6 1.8 (+/-10% I/O ring)	1.7 mA/MHz	Sleep: 50 uA, RTC 0.3 uA	Dedicated DSP instructions including single cycle Multiply-Accumulate		
Stretch www.stretchinc.com	S5530	SCP	250, 300	24/8 or 24/16 or Multiplexed 24/32	16, 24	1.5	2 to 4W		Customizable Execution Unit, any bit width	Yes	32-kbyte instruction/data
Stretch www.stretchinc.com	S5610	SCP	250, 300	24/8 or 24/16 or Multiplexed 24/32	16, 24	1.5	2 to 4W		Customizable Execution Unit, any bit width	Yes	32-kbyte instruction/data
Stretch www.stretchinc.com	S5620	SCP	250, 300	24/8 or 24/16 or Multiplexed 24/32	16, 24	1.5	2 to 4W		Customizable Execution Unit, any bit width	Yes	32-kbyte instruction/data
Stretch www.stretchinc.com	S6100	SCP	300, 345	32	16, 24, 64	1.2, 1.0	2W		Customizable Execution Unit, any bit width	Yes	40-kbyte instruction/data
Stretch www.stretchinc.com	S6105	SCP	300, 345	32	16, 24, 64	1.2, 1.0	2W		Customizable Execution Unit, any bit width	Yes	40-kbyte instruction/data
Tensilica www.tensilica.com	330HiFi	Xtensa	540 (65nm GP worst case)	64	16, 24, 64	Process-dependent	0.104mW/MHz (area); 0.167mW/MHz (speed) 65nm GP	Powerdown	Dual 16x16 MAC, zero-overhead looping, clamps, max/min value, normalize and sign extend		4/8-kbyte instruction/data, two-way set associative, programmable write-through or write-back
Tensilica www.tensilica.com	388VDO	Xtensa	300 (90nm GT worst case)	Two 32-bit	16,24,64,128	Process-dependent	47mW (200MHz) Typical H.264 SDTV decode (90nm GT)	Powerdown	Core 0: 3-issue 32-bit FLIX; general multipliers. Core 1: 8 16x16 multipliers plus custom multiplier for CABAC		
Tensilica www.tensilica.com	545CK DSP	Xtensa	520 (65nm GP worst case)	128	16, 24, 64	Process-dependent	0.08mW/MHz (area); 0.14mW/MHz (speed) 65nm GP	Powerdown	3-issue VLIW DSP with 8-way SIMD 16x16 multiplier unit. DSP instruction extensions		

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
4-kbyte SRAM, NAND booting	6-channel DMC, Flash, SRAM, ROM, DDR/SDR	Yes	400 FBGA	Four 16-bit	Four UART, two SPI(High speed SPI), I ² S, I ² C, AC97, two USB host/device, CF/ATA Interface	24 external	Eight-channel, 10 bit touchscreen	0 to +70 -40 to +85	STN/TFT LCDC, 8MP CAMERA, SD/MMC, HSMMC(SDHC)	
4-kbyte SRAM, 16-kbyte instruction/data TCM, NAND booting	32-channel DMC, Flash, SRAM, ROM, DDR/SDR	Yes	424 FBGA	Five 32-bit	Four UART, two SPI(High speed SPI), I ² S, I ² C, AC97, PCM, USB OTG/host, Modem Interface, CF/ATA Interface	127 external	Eight-channel, 10 bit touchscreen	0 to +70 -40 to +85	TFT LCDC, Video Codec(D1 30fps), JPEG, TV Encoder, 2D Graphic, 16MP CAMERA, Three HSMMC(SDHC)	
32-, 64-, 128-, 256-, 384-, 512-kbyte Flash, 6 - 64 kbyte SRAM	12-channel DMA		36QFN, 48 LQFP, 64 LQFP, 100 LQFP/BGA, 144 LQFP/BGA	Four 16 bit, two 16-bit PWM and dead-time generation, two watchdog, 15 uA realtime, 24-bit down counter, two 16-bit DAC	3 SPI, 2 I ² C, 5 USART(IrDa/ISO7816), I ² S, SDIO, USB, CAN, up to 112 GPIO 5V Tolerant	60, 16 priority levels	Three 21-channel 12-bit (1 uS) ; 2-channel 12-bit DAC	-40 to 105	Serial Wire Debug (SWD) and JTAG, 3-ph induction motor control, Internal 8MHz RC and 32kHz RC, Flexible static memory controller (supports NOR, NAND, Compact Flash, SRAM, PSRAM and LCD Parallel interface)	From \$1.80
256- or 512-kbyte Main Flash + 32-kbyte second Flash, 64- or 96-kbyte SRAM	8-channel DMA, dedicated DMA for Ethernet MAC		80/128 LQFP, 144 LFBGA	Seven 16-bit, watchdog, 1uA realtime	Ethernet, USB, CAN, 3 UART, 2 I ² C, 2xSPI, up to 80 GPIO 5V tolerant	32, 32 priority levels	8-channel, 10-bit (0.7 uS)	-40 to +85	JTAG port, Embedded Trace Module (ETM), 3-ph induction motor control block, true 1uA RTC	From \$4.77
256-kbyte SRAM, 32-kbyte dual-port RAM	64-bit DDR400	Yes	672 FCBGA	Two 32-bit, 32-bit watchdog	Four 10/100/1000 Ethernet/FIFO, PCI or PCI-X, two UART, SPI, TWI, eight GPIO	8 GPIO		0 to +100	Instruction Set Extension Fabric	\$70
256-kbyte SRAM, 32-kbyte dual-port RAM	64-bit DDR400 with ECC	Yes	1053 FCBGA	Two 32-bit, 32-bit watchdog	SysAD Bus I/F; Four 10/100/1000 Ethernet/FIFO, PCI or PCI-X, SPI, two TDM, two UART, TWI, eight GPIO	8 GPIO		0 to +100	Instruction Set Extension Fabric	\$100
256-kbyte SRAM, 32-kbyte dual-port RAM	64-bit DDR400 with ECC	Yes	1053 FCBGA	Two 32-bit, 32-bit watchdog	60x Bus I/F; Four 10/100/1000 Ethernet/FIFO, PCI or PCI-X, SPI, two TDM, two UART, TWI, eight GPIO	8 GPIO		0 to +100	Instruction Set Extension Fabric	\$100
80-kbyte Dual Port RAM plus 64-kbyte in programmable fabric	Four DMA, 16 or 32 bit DDR2 667		622HSBGA		PCIe, 10/100/1000 Ethernet, two I ² S, SPI, eGIB, TWI, 24 GPIO, two UARTs, four 10-bit data ports, four 32 bit AIM	8 GPIO		-40 to +125, 0 to 100	Instruction Set Extension Fabric, programmable accelerator	From \$44
80-kbyte Dual Port RAM plus 64-kbyte in programmable fabric	Four DMA, 16 or 32 bit DDR2 667		622HSBGA		10/100/1000 Ethernet, two I ² S, SPI, eGIB, TWI, 24 GPIO, two UARTs, four 10-bit data ports, four 32 bit AIM	8 GPIO		-40 to +125, 0 to 100	Instruction Set Extension Fabric, programmable accelerator	From \$33
Memory protection unit, single-cycle instruction and/or data SRAM up to 128-kbyte each			IP core	Three 32-bit		15		(Core)		License
Total local instruction 64-kbyte; data 72-kbyte			IP core	Three 32-bit		0		(Core)		License
128-kbyte Instruction RAM, Dual Data RAMs (128-kbyte each)			IP core	Three 32-bit		15		(Core)	Hardware Acceleration for Digital Video Codec operation	License

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Tensilica www.tensilica.com	Diamond 106Micro	Xtensa	610 (65nm GP worst case)	32	16, 24	Process-dependent	0.029mW/MHz (area); 0.044mW/MHz (speed) 65nm GP	Powerdown			
Tensilica www.tensilica.com	Diamond 108Mini	Xtensa	615 (65nm GP worst case)	32	16, 24	Process-dependent	0.041mW/MHz (area); 0.065mW/MHz (speed) 65nm GP	Powerdown			
Tensilica www.tensilica.com	Diamond 212GP	Xtensa	600 (65nm GP worst case)	32	16, 24	Process-dependent	0.062mW/MHz (area); 0.103mW/MHz (speed) 65nm GP	Powerdown	Single-cycle 16x16 MAC, zero-overhead looping, clamps, max/min value, normalize and sign extend		8-kbyte instruction/data, two-way set associative, programmable write-through or write-back
Tensilica www.tensilica.com	Diamond 232L	Xtensa	520 (65nm GP worst case)	32	16, 24	Process-dependent	0.062mW/MHz (area); 0.103mW/MHz (speed) 65nm GP	Powerdown	Single-cycle 16x16 MAC, zero-overhead looping, clamps, max/min value, normalize and sign extend		16-kbyte instruction/data, four-way set associative, programmable write-through or write-back
Tensilica www.tensilica.com	Diamond 570T	Xtensa	560 (65nm GP worst case)	64	16, 24, 64	Process-dependent	0.08mW/MHz (area); 0.14mW/MHz (speed) 65nm GP	Powerdown	Single-cycle 16x16 MAC, zero-overhead looping, clamps, max/min value, normalize and sign extend		16-kbyte instruction/data, two-way set associative, programmable write-through or write-back
Tensilica www.tensilica.com	Xtensa 7	Xtensa	680 (65nm GP typical)	32/32, 64, 128	16, 24 modeless mix	Process-dependent	38 uW/MHz (65nm GP) speed-optimized, minimum configuration	Powerdown	Five 16x16, 32x32 Vectra DSP co-processor options, user instructions, 16x16 MAC, 16x16 and 32x32 multiply, Optional SIMD DualMAC	Optional, IEEE-754 compatible	Configurable 0- to 32-kbyte instruction/data, four-way set associative
Tensilica www.tensilica.com	Xtensa LX2	Xtensa	680 (65nm GP typical)	32/32, 64, 128	16, 24 modeless mix	Process-dependent	38 uW/MHz (65nm GP) speed-optimized, minimum configuration	Powerdown	Five 16x16, 32x32 Vectra DSP co-processor options, user instructions, 16x16 MAC, 16x16 and 32x32 multiply, 32-bit SIMD and HiFi Audio Engine	Optional, IEEE-754 compatible	Configurable 0- to 32-kbyte instruction/data, four-way set associative
Texas Instruments www.ti.com/c2000	Piccolo TMS320F2802/F2803x	TMS320C28x	40 to 60	16/ 32	16, 32	1.9/3.3	<300 mW	Four modes, each peripheral independently	32x32; dual 16x16		
Texas Instruments www.ti.com/c2000	TMS320F280x	TMS320C28x	60 to 100	19/16	16, 32	1.8/3.3	425 mW	Four modes, each peripheral independently	32x32; dual 16x16		
Texas Instruments www.ti.com/c2000	TMS320F281x	TMS320C28x	150	19/16	16, 32	1.9/3.3	625 mW	Four modes, each peripheral independently	32x32; dual 16x16		
Texas Instruments www.ti.com/c2000	TMS320F2823x	TMS320C28x	100 to 150	16/32	16, 32	1.9/3.3	580 mW	Four modes, each peripheral independently	32x32; dual 16x16		
Texas Instruments www.ti.com/c2000	TMS320F2833x	TMS320C28x	100 to 150	16/32	16, 32	1.9/3.3	580 mW	Four modes, each peripheral independently	32x32; dual 16x16	Yes	

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
Cacheless with memory protection unit; single-cycle instruction and dual data SRAM interfaces			IP core	Three 32-bit		15		(Core)		
Cacheless with memory protection unit; single-cycle instruction and dual data SRAM interfaces			IP core	Three 32-bit		15		(Core)		\$75,000 license
Memory protection unit, single-cycle instruction and/or data SRAM up to 128-kbyte each			IP core	Three 32-bit		15		(Core)		License
		Yes	IP core	Three 32-bit		15		(Core)		License
Memory protection unit, single-cycle instruction and/or data SRAM up to 128-kbyte each			IP core	Three 32-bit		15		(Core)		License
Configurable: instruction/data, up to 256-kbyte RAM and ROM, XLMI interface to memories or tightly coupled hardware		Optional and configurable	IP core	Up to three 32-bit		Up to 32		(Core)	Automated processor-generation system creates new processor and tool suite in one hour	License
Configurable: instruction/data, up to 256-kbyte RAM and ROM, XLMI interface to memories or tightly coupled hardware		Optional and configurable	IP core	Up to three 32-bit		Up to 32		(Core)	Automated processor-generation system creates new processor and tool suite in one hour. Optional ECC/parity on Local memories	License
32- to 168-kbyte Flash, 12- to 20-kbyte RAM			38 TSSOP, 48 LQFP, 64 TQFP, 80 LQFP	16 and 32-bit, 16-bit PWM	SCI, 2 SPI, CAN, I ² C, LIN, 44 GPIO	All peripherals and I/O	12-bit, 7-16 channel	-40 to +85 -40 to +125	Single 3.3V supply, on F2803x: Control Law Accelerator, CAN, LIN AECQ100	sub to \$2.00 to \$7.95
12- to 36-kbyte RAM, 32- to 256-kbyte Flash			100 LQFP/100 BGA	16 and 32-bit, 16-bit PWM	4 SPI, 2 SCI, 2 CAN, I ² C, 35 GPIO	96	12-bit, 16-channel	-40 to +85, -40 to +125	0.18-micron, five-layer aluminum Hi-Res PWM technology provides 16 bits of accuracy in a 100 KHz control loop and 12 bits at 1MHz	\$3.45 to \$13.80 (100)
36- to 40-kbyte RAM, 128- to 256-kbyte Flash			128/176 LQFP, 179 BGA	16 and 32-bit, 16-bit PWM	SPI, 2 SCI, CAN, McBSP, 56 GPIO	96	12-bit, 16-channel	-40 to +85, -40 to +125	0.18-micron, five-layer aluminum Hi-Res PWM technology provides 16 bits of accuracy in a 100 KHz control loop and 12 bits at 1MHz	\$9.70 to \$16.70 (100)
52- to 68-kbyte RAM, 128- to 512-kbyte Flash	DMA		176 LQFP, 179 BGA	16 and 32-bit, 16-bit PWM	3 SCI, SPI, 2 CAN, 2 McBSP, I ² C, 88 GPIO	96	12-bit, 16-channel	-40 to +85, -40 to +125	Hi-Res PWM technology provides 16 bits of accuracy in a 100 KHz control loop and 12 bits at 1MHz	\$14.10 to \$20.30 (100)
52- to 68-kbyte RAM, 128- to 512-kbyte Flash	DMA		176 LQFP, 179 BGA	16 and 32-bit, 16-bit PWM	3 SCI, SPI, 2 CAN, 2 McBSP, I ² C, 88 GPIO	96	12-bit, 16-channel	-40 to +85, -40 to +125	Hi-Res PWM technology provides 16 bits of accuracy in a 100 KHz control loop and 12 bits at 1MHz	\$15.30 to \$21.22 (100)

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Texas Instruments www.ti.com/c2000	TMS320R28xx	TMS320C28x	150	19/16	16, 32	1.9/3.3	525 mW	153 uW, four modes, each peripheral independently	32x32; dual 16x16		
Texas Instruments www.ti.com/tms470	TMS470 R1Axxx	TMS470	Up to 48	32	16, 32	1.8 to 2	70 mA	Standby: 2mA Halt: 1 mA	8x32		
Texas Instruments www.ti.com/tms470	TMS470 R1Bxxx	TMS470	Up to 60	32	16, 32	1.8 to 2	125 mA	Standby:4mA Halt 2 mA	8x32		
Texas Instruments www.ti.com/tms470	TMS470M Automotive	ARM v7M	48 to 80	32/32	16, 32	1.5/3.3	350 mW	Two modes	32 hardware multiplier, 32 hardware divider		
Texas Instruments www.ti.com/tms470	TMS470PLF2x Automotive Cluster	ARM v4T	48	32/32	16, 32	1.8/5	650 mW	Four modes	32 hardware multiplier		
Texas Instruments www.ti.com/tms470	TMS470PLF4/6x Automotive	ARM v4T	48 to 72	32/32	16, 32	1.8/3.3 or 1.5/3.3	250 mW	Two modes	32 hardware multiplier		
Texas Instruments www.ti.com/tms470	TMS470R1X Automotive	ARM v4T	24 to 72	32/32	16, 32	1.8/3.3	300 mW	Two modes	32 hardware multiplier		
Texas Instruments www.ti.com/tms470	TMS570 Automotive	ARM v7R	80 to 160	32/64	16, 32	1.5/3.3	550 mW	Two modes	32 hardware multiplier, 32 hardware divider, DSP/SIMD extensions	Planned	Planned
Toshiba America Electronic Components www.toshiba.com/taec	900/H1	TLCS	20, 80	24/32	8, 16, 32	3.0 to 3.6, 4.5 to 5.5	37 mA/45 mA (20/80MHz)	Idle2: 26 mA, idle1: 2.7 mA, stop: 0.4 uA	One-clock cycle MAC: 32x32+64bit		
Toshiba America Electronic Components www.toshiba.com/taec	TMPA910	ARM926EJ-S	200	7 layer bus system	32	0.1 to 1.5, 1.8 to 3.6, 3.0 to 3.6	800 mW	Halt, Sleep, PCM, PLL-Off			16-kbyte instruction/data
Toshiba America Electronic Components www.toshiba.com/taec	TMPR 3927CF	MIPS32	133	20 to 28/16 to 32	32	2.5/3.3	1W	Halt, doze, reduce frequency	One-cycle 32x32+64 MAC		
Transmeta Corporation www.transmeta.com	Efficeon TM88X0	x86	Up to 1700	32	32		Application-dependent	Auto-halt, quick start, deep sleep, DSX	Yes	Yes	128/64-kbyte instruction/data, L2: 1-Mbyte
Ubicom www.ubicom.com	IP3023	Ubicom	250	Software I/O (Serial/Parallel I/O)	32	1.2/2.5 to 3.3, 5 tolerant	575 mW	Runtime clock control, separate control of I/O and core PLLs	One-cycle 16x16+48-bit MAC		None, single-cycle memory on-chip
Ubicom www.ubicom.com	IP5100 StreamEngine 5000	Ubicom	275	Hardware and Software I/O (Serial/Parallel I/O)	32	1.2/2.5 to 3.3, 5 tolerant	1500 mW	Runtime clock control, separate control of I/O and core PLLs	One-cycle 16x16+48-bit MAC, Enhanced new instruction set		16/8-kbyte instruction/data, support for external DDR and flash memory

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
40-kbyte RAM			128 LQFP, 179 BGA, 176 LQFP	16-bit/PWM	SPI, 2 SCI, CAN, McBSP, 56 GPIO	96	12-bit, 16-channel	-40 to +85, -40 to +125	0.18-micron, five-layer aluminum	\$9.15 to \$10.65 (1000)
8- to 32-kbyte SRAM, 64- to 288-kbyte Flash	Some		80 LQFP, 100 LQFP, 144 LQFP	12 to 16 HET channel	2 SPI, 2 SCI, 1 to 2 CAN, 40 to 94 GPIO	All peripherals and I/O	8- to 16-channel 10-bit	-40 to 105	analog watchdog timer	\$4.95 to \$8.95
32- to 64-kbyte RAM, 384- to 1024 kbyte Flash	DMA		144 LQFP	12 to 32 HET channel	2 to 5 SPI, 2 to 3 SCI, 1 to 2 CAN, 87 to 93 GPIO	All peripherals and I/O	12- to 16-channel 10-bit	-40 to 105	analog watchdog timer	\$9.95 to \$14.95
196- to 640-kbyte Flash, 12- to 64-kbyte RAM		MPU	80 - 144 LQFP	Up to 24 x-bit/ Up to 24 x-bit PWM	Up to 3 SPI, 2 LIN/SCI, 2 CAN, 40-84 GPIO	8 external, 64 internal	10-bit, 16-channel	-40 to +85, -40 to +105, -40 to +125	Optional program and instrumentation trace, main memory ECC, peripheral parity	\$4.40 to \$6.75
256- to 1024-kbyte Flash, up to 64-kbyte RAM	DMA	MPU	144 TQFP	Up to 24 x-bit/ Up to 24 x-bit PWM	1 SPI, 1 MibSPI, 1 LIN/SCI, 2 CAN, 40-84 GPIO	48	10-bit, 16-channel	-40 to +105,	Control for 6 Stepper Motors	\$5.00 to \$8.00
256- to 1024-kbyte Flash, up to 64-kbyte RAM	DMA	MPU	144 TQFP	Up to 24 x-bit/ Up to 24 x-bit PWM	1 SPI, 1 MibSPI, 1 LIN/SCI, 2 CAN, 40-84 GPIO	48	10-bit, 16-channel	-40 to +105,	Optional program and data trace; optional safety lock step dual core, main memory parity/ECC, peripheral parity	\$5.00 to \$8.00
128kB-1024kB Flash 48kB RAM	DMA	MPU	80 - 144 LQFP 176-324 PBGA	Up to 32 x-bit/ Up to 32 x-bit PWM	Up to 5 SPI, 2 SCI, 3 CAN, 5 I2C, C2SI, 40-187 GPIO	8 external, 64 internal	10-bit, up to 32-channel	-40 to +85, -40 to +105, -40 to +125		\$4.25 to \$17.00
704-kbyte to 2.0-Mbyte Flash 56- to 160-kbyte RAM	DMA	MPU	100-176 LQFP 208-256 PBGA	Up to 32 x-bit/ Up to 32 x-bit PWM	Up to 3 SPI, 2 LIN/SCI, 3 CAN, FlexRay, 40-105 GPIO	8 external, 64 internal	10-bit, up to 32-channel 12-bit, up to 24-channel	-40 to +85, -40 to +105, -40 to +125	Optional program and data trace; optional calibration interface; safety lock step dual core or M3 I/O processor, main memory parity/ECC, peripheral parity	\$7.90 to \$19.10
Up to 512-kbyte Flash/ROM, 288-kbyte SRAM	Eight -channel micro DMA, NAND Flash, DRAM	Yes	100/144/160/176/228/ QFP/LQFP/FBGA	Up to eight 8-bit, up to six 16-bit, watchdog, real-time clock	Up to three UART, synchronous SIO, HS SIO, SEI, CAN, SPI, IrDA, I ² C, up to 136 PIO	56, nine CPU, nine external, 38 internal, seven levels	Up to 12-channel, 10-bit: two channel 8-bit DAC	-40 to +85	Four 32-bit register banks, LCD controller, USB Host & Device,	\$3 to \$10
ROMLESS, 56-kbyte SRAM	8-channel chip-select one channel for DRAM	Yes	361 BGA	16-bit timer: 6 channels, 2 channels with PWM functions	I2C-2 channels, UART-2 channels, I2S-2 channels	External: 28 Internal: 21	10-bit ADC 6 Channels	0 to +70	Touch screen controller, LCD accelerator, NAND Flash controller, SD, USB,	\$7 to \$10
	SDRAM, SGRAM, DIMH Flash, SRAM, SMROM, ROM, DMA	64-entry, 4-kbyte to 4-Mbyte pages	240 PQFP	Three 32-bit, watchdog	Two UART, 16 PIO	6 external		0 to +70	Debug support unit	\$15
	64-bit DDR	Yes	592/783 BGA					0 to +100 (junction)	MMX, SSE, SSE2, SSE3, Enhanced LongRun Power Management, ECC Memory Support	\$75 to \$150
256-kbyte SRAM (instruction/data), 64-kbyte data SRAM	Flash, SDRAM		228 uBGA	Two 32-bit, 32-bit watchdog, can add timers	Four MII, two SerDes (10bT MAC/PHY, USB host/device, GPSI, SPI, UART). Soft I/O capable (PCMCIA, CF, IDE, MPEG-TS, PCI for 802.11a/g, UART, SPI, I ² C, I ² S, AC97)	Up to 64	Analog squelch for 10Base-T Ethernet PHY	0 to +70	Eight-way hardware multithreading, zero-cycle context switching, 32-bit random-number generator, software I/O supports interfaces via GPIO	\$12
192-kbyte of SRAM (instruction/data) plus 24-kbyte cache memory	Serial Flash/DDR1/2 (8-bit-wide)		256 BGA	One real-time 32-bit, one 32-bit watchdog, and 10 multi function	MIIX 2, RMII x 2, USB 2.0 (FS/HS), USB 2.0 (FS), UART (SerDes HW or SW), SPI (SerDes HW or SW), GPSI, PCI. Soft I/O capable (Utopia, ISA/PCMCIA/CF, IDE, I ² C, I ² S, AC97)	Up to 64		0 to +70	Ten-way hardware multithreading, zero-cycle context switching, 32-bit random-number generator, software I/O supports interfaces via GPIO, deterministic processing, dedicated security engine, and native audio processing.	

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Ubitom www.ubicom.com	IP5160 StreamEngine 5000	Ubitom	270	Hardware and Software I/O (Serial/Parallel I/O)	32	1.2/2.5 to 3.3, 5 tolerant	1500 mW	Runtime clock control, separate control of I/O and core PLLs	One-cycle 16x16+48-bit MAC, Enhanced new instruction set		16/8-kbyte instruction/data, support for external DDR and flash memory
Ubitom www.ubicom.com	IP5170 StreamEngine 5000	Ubitom	350	Hardware and Software I/O (Serial/Parallel I/O)	32	1.2/2.5 to 3.3, 5 tolerant	2200 mW	Runtime clock control, separate control of I/O and core PLLs	One-cycle 16x16+48-bit MAC, Enhanced new instruction set		16/8-kbyte instruction/data, support for external DDR and flash memory
Ubitom www.ubicom.com	IP7100 StreamEngine 7000	Ubitom	270	Hardware and Software I/O (Serial/Parallel I/O)	32	1.0/2.5 to 3.3, 5 tolerant	1000 mW	Runtime clock control, separate control of I/O and core PLLs	One-cycle 16x16+48-bit, 32x32 MAC, Enhanced new instruction set including byte instructions		16/16-kbyte instruction/data, support for external DDR and flash memory
Ubitom www.ubicom.com	IP7160 StreamEngine 7000	Ubitom	350, 400	Hardware and Software I/O (Serial/Parallel I/O)	32	1.0/2.5 to 3.3, 5 tolerant	1200 mW	Runtime clock control, separate control of I/O and core PLLs	One-cycle 16x16+48-bit, 32x32 MAC, Enhanced new instruction set including byte instructions		16/16-kbyte instruction/data, support for external DDR and flash memory
Ubitom www.ubicom.com	IP7170 StreamEngine 7000	Ubitom	500	Hardware and Software I/O (Serial/Parallel I/O)	32	1.2/2.5 to 3.3, 5 tolerant	1700 mW	Runtime clock control, separate control of I/O and core PLLs	One-cycle 16x16+48-bit, 32x32 MAC, Enhanced new instruction set including byte instructions		16/16-kbyte instruction/data, support for external DDR and flash memory
VIA Technologies www.viatech.com	C3	x86	1000 to 1400	32/64	32	1.4	17.1W TDP	Autohalt, stopgrant		Yes	64-kbyte instruction/data, L2: 64-kbyte
VIA Technologies www.viatech.com	C7	x86	1000 to 2000	32/64	32	1.004 to 1.196	20W TDP	Autohalt, stopgrant, sleep, deepsleep, deeper sleep		Yes	128-kbyte instruction/data, L2: 128-kbyte
VIA Technologies www.viatech.com	C7-D	x86	1500 to 2000	32/64	32	1.084 to 1.196	20W TDP	Autohalt, stopgrant, sleep, deepsleep		Yes	128-kbyte instruction/data, L2: 128-kbyte
VIA Technologies www.viatech.com	C7-M	x86	1500 to 2000	32/64	32	1.004 to 1.196	20W TDP	Autohalt, stopgrant, sleep, deepsleep, deeper sleep		Yes	128-kbyte instruction/data, L2: 128-kbyte
VIA Technologies www.viatech.com	C7-M ULV	x86	1000 to 1500	32/64	32	0.796 to 0.956	7.5W TDP	Autohalt, stopgrant, sleep, deepsleep, deeper sleep		Yes	128-kbyte instruction/data, L2: 128-kbyte

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
192-kbyte of SRAM (instruction/data) plus 24-kbyte cache memory	Serial Flash/DDR1/2 (16-bit wide)		256 BGA	One real-time 32-bit, one 32-bit watchdog, and 10 multi function	MII x 2, RMII x 2, RGMII, USB 2.0 (FS/HS), USB 2.0 (FS), UART (SerDes HW or SW), SPI (SerDes HW or SW), GPSI, PCI. Soft I/O capable (Utopia, ISA/PCMCIA/CF, IDE, I ² C, I ² S, AC97)	Up to 64		0 to +70	Ten-way hardware multithreading, zero-cycle context switching, 32-bit random-number generator, software I/O supports interfaces via GPIO, deterministic processing, dedicated security engine, and native audio processing.	\$12
192-kbyte of SRAM (instruction/data) plus 24-kbyte cache memory	Serial Flash/DDR1/2 (16-bit wide)		256 BGA	One real-time 32-bit, one 32-bit watchdog, and 10 multi function	MII x 2, RMII x 2, RGMII, USB 2.0 (FS/HS), USB 2.0 (FS), UART (SerDes HW or SW), SPI (SerDes HW or SW), GPSI, PCI. Soft I/O capable (Utopia, ISA/PCMCIA/CF, IDE, I ² C, I ² S, AC97)	Up to 64		0 to +70	Ten-way hardware multithreading, zero-cycle context switching, 32-bit random-number generator, software I/O supports interfaces via GPIO, deterministic processing, dedicated security engine, and native audio processing.	\$14
240-kbyte of SRAM (instruction/data) plus 32-kbyte cache memory	Serial Flash/DDR1/2 (16-bit wide)		256 BGA	One real-time 32-bit, one 32-bit watchdog, and 10 multi function, 3PWMs	MII x 2, RMII x 2, USB 2.0 (FS/HS), UART (SerDes HW or SW), GPSI, PCI, SD/SDIO. Soft I/O capable (Utopia, ISA/PCMCIA/CF, IDE, I ² C, I ² S, AC97)	Up to 64		0 to +70	Twelve-way hardware multithreading, zero-cycle context switching, 32-bit random-number generator, software I/O supports interfaces via GPIO, deterministic processing, dedicated security engine, and native audio processing.	\$10
240-kbyte of SRAM (instruction/data) plus 32-kbyte cache memory	Serial Flash/DDR1/2 (16-bit wide)		256 BGA	One real-time 32-bit, one 32-bit watchdog, and 10 multi function, 3PWMs	MII x 2, RMII x 2, RGMII x 2, USB 2.0 (FS/HS), UART (SerDes HW or SW), SPI (SerDes HW or SW), GPSI, PCI, SD/SDIO. Soft I/O capable (Utopia, ISA/PCMCIA/CF, IDE, I ² C, I ² S, AC97)	Up to 64		0 to +70	Twelve-way hardware multithreading, zero-cycle context switching, 32-bit random-number generator, software I/O supports interfaces via GPIO, deterministic processing, dedicated security engine, and native audio processing.	\$12
240-kbyte of SRAM (instruction/data) plus 32-kbyte cache memory	Serial Flash/DDR1/2 (16-bit wide)		256 BGA	One real-time 32-bit, one 32-bit watchdog, and 10 multi function, 3PWMs	MII x 2, RMII x 2, RGMII x 2, USB 2.0 (FS/HS), UART (SerDes HW or SW), SPI (SerDes HW or SW), GPSI, PCI, SD/SDIO. Soft I/O capable (Utopia, ISA/PCMCIA/CF, IDE, I ² C, I ² S, AC97)	Up to 64		0 to +70	Twelve-way hardware multithreading, zero-cycle context switching, 32-bit random-number generator, software I/O supports interfaces via GPIO, deterministic processing, dedicated security engine, and native audio processing.	\$14
			EBGA					0 to +85 (case)	Streaming SIMD extensions	
			NanoBGA2 400L					0 to +100 (junction)	MMX, SSE, SSE2, SSE3, PadLock	\$50 to \$100
			NanoBGA2					0 to +100 (case)	MMX, SSE, SSE2, SSE3, PadLock	\$45 to \$75
			478 μFC-PGA, 479 μFC-BGA					0 to +100 (junction)	MMX, SSE, SSE2, SSE3, PadLock	\$50 to \$85
			NanoBGA2 400L					0 to +100 (junction)	MMX, SSE, SSE2, SSE3, PadLock	\$70 to \$120

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32-bit microprocessors sorted by company

Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
VIA Technologies www.viatech.com	Eden	x86	400 to 1500	32/64	32	0.796 to 0.956	7.5W TDP	Autohalt, stopgrant, sleep, deepsleep, deeper sleep		Yes	128-kbyte instruction/data, L2: 128-kbyte
VIA Technologies www.viatech.com	Eden ESP	x86	400 to 1000	32/64	32	15, 1.15	7W TDP	Autohalt, stopgrant		Yes	64-kbyte instruction/data, L2: 64-kbyte
VIA Technologies www.viatech.com	Eden-N	x86	533, 800, 1000	32/64	32	0.9, 0.95, 1	7W TDP	Autohalt, stopgrant, sleep, deepsleep		Yes	64-kbyte instruction/data, L2: 64-kbyte
Xilinx www.xilinx.com	PowerPC 405 embedded in Virtex-II Pro and Virtex-4 FX FPGAs	PowerPC	Up to 450	32/64	32	1.5 (Virtex-II Pro) or 1.2 (Virtex-4 FX)	0.45 mW/MHz Virtex-4 FX	Yes	Access to embedded multipliers and XtremeDSP slices in FPGA via dedicated auxiliary processor unit (APU) controller. User defined DSP Coprocessors.	Optional soft FPU in FPGA Fabric	16-kbyte instruction/data, two-way set-associative
Xilinx www.xilinx.com	MicroBlaze (soft configurable core) for Virtex and Spartan FPGAs	MicroBlaze	Up to 200	32/32 Harvard Architecture	32	1.2 to 3.3 (FPGA usage)			Configurable option via Fast Simplex Link (FSL). User defined DSP coprocessors	Tightly integrated FPU option in MicroBlaze v4.00	Configurable 0- to 64-kbyte instruction/data, direct mapped, write-through
XMOS www.xmos.com	XS1-G1	XS1-G	400	32	32	1	100mW		32x32-64 MAC		
XMOS www.xmos.com	XS1-G2	XS1-G	400	32	32	1	200mW		32x32-64 MAC		
XMOS www.xmos.com	XS1-G4	XS1-G	400	32	32	1	400mW		32x32-64 MAC		
ZiLOG www.zilog.com	ZATARA ZA9L00XXNW1LS G	32-Bit ARM 9	180	Dual		1.8 / 3.0 to 3.6					
ZiLOG www.zilog.com	ZATARA ZA9L00XXNW1LX G	32-Bit ARM 9	180	Dual		1.8 / 3.0 to 3.6					
ZiLOG www.zilog.com	ZATARA ZA9L01XXNW1LS G	32-Bit ARM 9	180	Dual		1.8 / 3.0 to 3.6					
ZiLOG www.zilog.com	ZATARA ZA9L01XXNW1LX G	32-Bit ARM 9	180	Dual		1.8 / 3.0 to 3.6					

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Memory	DMA / memory controller	MMU	Package selection	Timers / PWM	Serial, Parallel I/O	Interrupts	ADC; DAC	Temperature ranges (degrees Celsius)	Additional features	Price (\$/10,000)
			NanoBGA2 400L					0 to +100 (junction)	MMX, SSE, SSE2, SSE3, PadLock	\$35 to \$150
			EBGA					0 to +85 (case)	3DNow!	
			nanoBGA					0 to +85 (case)	3DNow!	
Up to 9936-kbyte Local BRAM, up to 4-Gbyte external	SDRAM, DDR, DDR2, SRAM, Flash, ZBT, SDRAM, Multi-channel DMA (soft IP)	Integrated MMU in PowerPC	Virtex-II Pro, Virtex-4 FX	PIT, FIT, watchdog, PWM	User definable - CoreConnect-enabled I ² C, GPIO, SPI, PCI, 16450/550 UART, UART lite, Dual "hard" 10/100/1000 EMACs (Virtex-4 FX), PCI	User definable - Core-Connect enabled controller, PowerPC capability		0 to +85 -40 to +100	Virtex-4 FX contains: Dual PowerPC 405 cores with Auxiliary Processor Unit (APU) controllers for custom instructions and accelerators, dual "hard" Tri-mode 10/100/1000 Ethernet, debug support, catalog of IP available.	Virtex to 4 FX devices start at \$29.99 and offer the hard PowerPC block
Up to 6048-kbyte Local BRAM, up to 4-Gbyte external	SDRAM, DDR, DDR2, SRAM, Flash, ZBT, SDRAM, Multi-channel DMA (soft IP)		IP Core	PIT, FIT, watchdog, PWM	User definable - CoreConnect-enabled I ² C, GPIO, SPI, PCI, 16450/550 UART, 10/100 EMAC, UART lite, CAN, MOST, Flexray	0 to 32 configurable with programmable level or edge sensitivity		NA - IP Core (For FPGA, 0 to +85 -40 to +100)	User-configurable CPU, dedicated interface Fast Simplex Link (FSL) for hardware acceleration, optional debug features for HW/SW debugging, catalog of IP available	Included in the Xilinx Embedded Development Kit at zero cost with royalty free license
64-kbyte SRAM, 8-kbyte PROM	built-in	built-n	44QFP, 80QFP, 100BGA	10	64				XLink interconnect	
128-kbyte SRAM 16-kbyte PROM	built-in	built-n	44QFP, 80QFP, 100BGA, 144 BGA	20	128				XLink interconnect	
256-kbyte SRAM 32-kbyte PROM	built-in	built-n	100BGA, 144BGA, 336 BGA, 512 BGA	40	256				XLink interconnect	\$15
64-kbyte SRAM			256 BGA	(9) 16-bit	Up to 76 GPIO		6 channel 10-bit	0 to +70	Security subsystem, smart card reader, magnetic stripe reader	
65-kbyte SRAM			256 BGA	(9) 16-bit	Up to 76 GPIO		6 channel 10-bit	-40 to +85	Security subsystem, smart card reader, magnetic stripe reader	
66-kbyte SRAM			256 BGA	(9) 16-bit	Up to 76 GPIO		6 channel 10-bit	0 to +70	Security subsystem	
67-kbyte SRAM			256 BGA	(9) 16-bit	Up to 76 GPIO		6 channel 10-bit	-40 to +85	Security subsystem	