

2002 DSP directory



Image by Mike O'Leary

**MARKET ANALYSIS
FORECASTS DSP SALES
TO TURN UPWARD IN
2002, WITH ISUPPLI
PREDICTING A 4%
RISE AND FORWARD
CONCEPTS EXPECTING
A 32% GAIN.**

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LAST YEAR WAS A HARSH ONE for processor-device sales. According to market analysis from iSuppli (www.isuppli.com) and Forward Concepts (www.forwardconcepts.com), DSP sales were down 30 to 45%, respectively, for 2001, a marginally worse drop than microcontroller sales suffered. The same market analysis forecasts DSP sales to turn upward in 2002, with iSuppli predicting a 4% rise and Forward Concepts expecting a 32% gain. A DSP-inventory glut for the cell-phone market at the beginning of

the year was a significant factor in the downturn in sales.

Signal processing is finding its way into many applications, including traditionally control-oriented ones, which are benefiting from access to DSP operations that speed math-oriented processing and allow more precise and sensorless control designs. The lines distinguishing DSPs and microcontrollers are blurring, as both types of devices are incorporating aspects of the other. In fact, several unified, or hybrid, microsignal-processor architectures now blend DSP and control processing into a single instruction thread, offering new options for applications that include both control- and signal-processing requirements (**Reference 1**).

In an attempt to maintain a clear distinction between DSP and controller devices, the directory survey requested devices, cores, or extensions that not only can process signals, but also find their primary application in signal processing. The DSP had to be a software-programmable device, core, or extension that includes an assembler or a compiler in the tool set. This requirement eliminated those products that, although they may include a programmable DSP core, restrict users to only selecting and setting operating parameters. Last, listed devices or IP must be currently or soon available. These criteria eliminate potential products from inclusion, but the directory still contains more entries than ever before.

In addition to being more restrictive, this year's directory is structured differently from those of previous years. The directory lists entries alphabetically by vendor and consolidates the support section that each entry normally includes in the last entry of the vendor's section. This structure reduces the amount of duplicate information, but, more important, it emphasizes that tool sets are usually common across a vendor's product lines. Almost without exception, integrated tool sets are a strategic element of any DSP offering and play a large role in design wins (**Reference 2**). The directory index groups entries by processor size rather than location in the directory to support comparison of similar-sized processors.



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ADELANTE TECHNOLOGIES' SATURN

Adelante's Saturn is an extensible, low-power, small-area, "open" RTL DSP core and subsystem targeting wireless-baseband handsets and digital-control applications. It employs a dual Harvard architecture with two 16-bit multipliers, four 16-bit ALUs that can combine into two 40-bit ALUs (32-bit with 8-bit overflow), a shift and saturation unit, a bit-manipulation unit, a barrel shifter, a hardware-loop-control unit, a program-control unit, and two data memories configurable to 64k words and expandable to 1M word with paging. The designer extends the core via custom application-specific instructions, execution units, and coprocessors to accelerate repetitive tasks.

The Saturn core integrates into Adelante's Lunar DSP subsystem, which includes program and data memory, DMA, interfaces to external processors, peripherals, and I/O (including an AMBA bus for ARM and MIPS processors), BIST, and JTAG hardware-debugging capability. Special constructs in the three-stage pipeline enable single-cycle overhead short branching and zero-overhead long branching. One nonmaskable interrupt and 16 maskable interrupts with single-cycle interrupt switching with simultaneous shadow X/Y-address-pointer switching support immediate execution of service routines.

▶ The core measures 0.5 mm² and consumes 0.25 mW/MHz in a standard 0.18-micron CMOS process.

▶ The Saturn can perform 420 million MACs/sec at 210 MHz.

Addressing modes: The Saturn supports single- and dual-data-memory-operand addressing for 32-bit operands, with direct data and absolute addressing.

Offset, indirect, absolute, immediate, modulo, and bit-reversed addressing support bit/nibble/byte access to memory. Two of the three X/Y-address pointers are context-sensitive.

Special instructions or integral-peripheral functions: Designers can extend the Saturn's 16-bit instruction set with 256 application-specific 96-bit VLIW (very-long-instruction-word) instructions that can fully exploit all core resources in parallel to accelerate repetitive DSP functions (for example, two-cycle execution of a 12-operation Viterbi butterfly). Designers can also integrate application-specific execution units and coprocessors into the DSP subsystem to accelerate computationally intensive functions, such as

turbo coding or multichannel ADPCM (adaptive differential pulse-code modulation).

Support: The Atmosphere Development Environment supports code-development debugging for application-specific instructions and execution units. The code-development tools include a compiler, a linker, a debugger, an instruction-set simulator, and a profiler. The debugger supports use with a JTAG hardware debugger and the runtime debug block for in-circuit runtime emulation. Adelante offers design services for the development, integration, and verification of application-specific execution units and application-specific coprocessors.

AGERE SYSTEMS' DSP16000

Agere's DSP16210 and DSP16410 devices use the DSP16000 core and target digital-communications applications that benefit from large, on-chip RAM with downloadable system support. The DSP16210 includes 60k words of dual-port RAM and can address as many as 192k words of external storage in both its code/coefficient-memory address space and data-memory address space. An internal boot ROM includes system-boot code and hardware-development-system code. This device also contains a bit-manipulation unit; a two-input, 40-bit ALU with add/compare/select for enhanced signal-coding efficiency and Viterbi acceleration; and a three-input adder for single-cycle accumulation of the results of both

▶ The DSP16410 can perform 800 MACs/sec at 200 MHz.

multipliers. To optimize I/O throughput and reduce the I/O service-routine burden on the DSP core, two modular I/O units manage the simple serial-I/O port and the 16-bit parallel host-interface peripherals. They also provide transparent DMA transfers between the peripherals and on-chip, dual-port RAM.

The DSP16410 targets communications-infrastructure applications and features twin DSP16000 dual-MAC DSP cores and enhanced DMA capabilities. Each DSP core has access to a 192-kbyte block of memory (384 kbytes total) and share a 4-kbyte block of memory for interprocessor communications. Its large on-chip memory supports fixed-point signal-processing functions, including equalization, channel coding, compression, and speech



coding. A centralized DMA unit supports transparent peripheral-to-memory and memory-to-memory transfers. The DSP16410 includes a 16-bit parallel port with DMA support that can provide host access to all DSP memory. The two serial-I/O units also include DMA support, are compatible with TDM highways, and include hardware support for u-law and A-law companding.

Addressing modes: The DSP16000 core architecture supports immediate, register-direct, address-register-indirect, and program-counter-relative modes, as well as register-plus-displacement addressing, and circular-buffer addressing.

Special instructions or integral-peripheral functions: The special instructions are arithmetic, logical, and shift operations, and bit-manipulation instructions to implement nonlinear algorithms, such as signum, A-law and u-law conversions, half-wave and full-wave rectification, and rounding. The bit-manipulation instructions include barrel shifting, normalization and exponent computation, and bit-field insertion or extraction.

AGERE SYSTEMS' STARPRO2000

The StarPro2000 targets high-performance communications-infrastructure applications, such as wireless base stations, voice-over-IP gateways, remote-access servers, and radio-network controllers. The StarPro2000 integrates three StarCore SC140 quad MAC DSP cores, 768 kbytes of shared memory, three serial-I/O units, one parallel-interface unit, and two external memory-interface units. Agere enhanced each SC140 DSP core with instruction and data caches,

▶ The StarPro2000 can perform 3000 million MACs/sec at 250 MHz.

local data memory, an interrupt controller, and bus-interface logic. The combination forms a SuperCore macrocell that is the basic building block for the StarPro family. The cores and peripherals connect via a high-speed, split-transaction-architecture, 128-bit-wide local interconnect bus that

can perform 128-bit transactions every clock cycle to minimize bottlenecks for internal and external transactions. The DSP core's instruction set, large set of general-purpose registers, and short instruction pipeline make it a viable target for coding algorithms in C.

Addressing modes: The SC140 architecture supports absolute, absolute-long, absolute-jump, reverse-carry, modulo, multiple-wrap-around-modulo, register-direct, address-register-indirect, and program-counter-relative addressing modes. Dual 64-bit data fetch, stores, or both can simultaneously address parallel instructions as byte, word, long, as well as dual-word, quad-word, and dual-long.

Special instructions or integral-peripheral functions: The multipliers support mixed signed and unsigned operands in both fractional and integer formats. The SC140 architecture supports bit-mask-test/set/clear operations for both data registers and memory, and an SIMD (single-instruction-multiple-data) version of maximum and minimum additions and subtractions. The SC140 can perform eight 16-bit additions or maximum and minimum operations per cycle and includes the MAX2VIT, which works with Viterbi Shift Left to accelerate Viterbi decoding algorithms.

The StarPro2000 includes six 32-bit, general-purpose timers that can interrupt any DSP core; a 32-bit, parallel-interface port with 31-bit address space and 32-bit data bus; and two 8-bit, general-purpose bit-I/O units. The two external-memory interfaces have a 28-bit address space and a 32-bit data bus. Eight memory-to-memory DMA channels allow block-memory moves anywhere in the memory space. Two DMA channels support each of the three serial-interface ports.

Support: Agere's LuXWorks supports development for DSP16000 and StarPro2000 devices. The integrated system-level development

tools includes a C compiler, an assembler, a linker, and a simulator. Hardware-development platforms and in-circuit-emulation capabilities are available through Agere's TargetView JTAG communication system featuring Agere's DART for real-time data collection. Agere also provides optimized libraries for voice transcoding and echo cancellation for wired networks and 2G, 2.5G, and 3G wireless standards. Additional third-party tools are available in cooperation with the StarCore Joint Development Center.

ANALOG DEVICES' ADSP-21XX

All ADSP-21xx processors are source-code-compatible and feature a high-level algebraic programming syntax. All instructions execute in a single clock cycle, including multifunction instructions. ADSP-21xx processors use separate program and data buses operating on 24-bit instructions and 16-bit data. The wider instruction word allows the device to use a more complex and robust instruction set than a 16-bit operation code, and the 16-bit data word provides lower power consumption for the needed dynamic range.

Processors are available with as much as

▶ All ADSP-21xx processors are source-code-compatible.

▶ Products cost less than \$4 in high volume.

2.4 Mbits of on-chip SRAM around the DSP core. All ADSP-21xx processors integrate a programmable DMA controller to maximize I/O throughput. The ADSP-218x supports as much as 4 Mbytes of external memory, and the ADSP-219x architecture supports 16M words of external memory.

All processors support a variety of serial-communications interfaces to ADC/DACs and other processors.

Addressing modes: ADSP-21xx processors support immediate, register-direct, memory-direct, and register-indirect addressing modes. The ADSP-219x adds register, indirect-post-modify, immediate-modify, and direct- and indirect-offset addressing modes. Each address generator supports as many as four circular buffers, each with three registers. The ADSP-219x supports as many as 16 circular buffers using a data-address-generator shadow-register set and a set of base registers for additional circular-buffering flexibility.

Special instructions or integral-peripheral functions: The ADSP-21xx contains dedicated loop hardware and a "do-until" loop instruction that supports loops ranging from 0 to 16,000 iterations, or loops, with infinite iterations. The ADSP-218x supports four-deep nesting via its loop hardware, and the ADSP-219x supports as many as eight loops. In addition to the standard arithmetic and logic instructions, the ALU supports division primitives. The ADSP-219x program sequencer features a six-deep pipeline and supports delayed branching. The ADSP-219x buses and instruction cache provide the data flow to maintain a continuous execution rate.

ANALOG DEVICES' ADSP-21000 SHARC FAMILY

The ADSP-21161N is the latest member of the SHARC family of general-purpose programmable DSPs. It is based on a Super Harvard ARCHitecture and has both SIMD (single-instruction-multiple-data) and SISD (single-instruction-single-data) functions. The SHARC SIMD core contains two computational blocks that each include a multiplier, an ALU, a data-register file, and a barrel shifter that can process in parallel in SIMD mode. The core contains dual data-address generators, independent data- and address-memory buses, a program sequencer with zero-overhead looping, an instruction cache, and a timer. While the core operates at full speed, the I/O processor moves data on and off chip. SHARC DSPs integrate 1 to 4 Mbits of on-chip SRAM; as many as four serial ports, six link ports, and 14 zero-overhead DMA channels; an SPI-



compatible port; a synchronous-DRAM controller; a parallel host interface; cluster-multiprocessing support; and an IEEE JTAG standard 1149.1 test-access port with on-chip emulation. The two-

▶ SHARC natively supports 32-bit fixed, 32-bit IEEE floating, and extended 40-bit floating-point data types.

▶ Multiprocessing configurations require no glue hardware.

independent, on-chip dual-ported SRAM blocks are selectable between program and data memory. The independent synchronous serial ports operate in TDM multichannel mode and, on the ADSP-21065L and ADSP-21161, offer I²S mode, which is useful for audio applications.

Addressing modes: ADSP-21000 SHARC DSPs support absolute and relative-direct addressing, premodify and postmodify registering, immediate-value-indirect addressing, and

modulo and bit-reverse addressing. The dual-ported memory allows independent data transfers from the core and the I/O. Three on-chip buses allow two data transfers from the core and one from I/O in one cycle.

Special instructions or integral-peripheral functions: The ADSP-21000 SHARC family features distributed on-chip bus arbitration. Devices allow you to connect as many as six processors (two for the ADSP-21065L) in parallel, plus a host. All SHARC instructions execute in one cycle. Special instructions include bit manipulation, division iteration, reciprocal of square-root seed, conditional subroutine call, single and block repeat with zero-overhead looping, average-of-two numbers, bit packing and unpacking fixed- to and from floating-point conversion, and conditional execution of most instructions. SHARC supports IEEE-754 single-precision floating-point, 32-bit fixed-point, and a 40-bit extended IEEE format for additional accuracy.

ANALOG DEVICES' ADSP-215XX BLACKFIN

Built from the Micro Signal Architecture core jointly developed by Analog Devices and Intel, Blackfin DSPs feature dual-MACs, high clock rates, and dynamic power management for balancing system performance and power consumption. The modified Harvard architecture core combines signal- and control-processing features into a single instruction-set architecture that benefits programming in high-level languages, such as C/C++. DSP-core functional blocks and capabilities include two 16-bit MACs, two 40-bit ALUs, four 8-bit video ALUs, and a barrel shifter, plus eight 32-bit math registers with support for 8/16/32-bit integer and 16/32-bit fractional data types. The four 8-bit video ALUs address multimedia algorithms, including MPEG-2, MPEG-4, and JPEG, allowing a single device to concurrently process audio, video, imaging, and data information. The ADSP-21535 targets next-generation digital-communication systems and Internet appliances, and the ADSP-21532 targets consumer-multimedia systems.

▶ System architecture supports an integrated DSP and RISC microcontroller-unit instruction set.

▶ Dynamic power management minimizes power consumption for power-constrained applications.

Blackfin DSPs include support for user and supervisor modes, byte addressing, memory protection, and an orthogonal

RISC instruction set. All Blackfin DSPs support a hierarchical and configurable memory model. L1 memory is physically closest to the core for highest system performance and is configurable as either SRAM or cache. L2 memory provides a larger memory space suitable for bulk storage of instructions or data. Additionally, dynamic power management permits context-sensitive control over power consumption by enabling designers to dynamically vary

both the operating frequency and the voltage of the DSP core for optimizing power-consumption profiles.

Addressing modes: All Blackfin DSPs support DSP and general-purpose addressing modes, including indirect, indexed, auto-increment or -decrement, postincrement, and bit-reversed. Four sets of index, base, length, and modify registers enable circular (modulo) buffering of as many as four buffers per data-address generator. In addition, eight 32-bit registers are available for general-purpose addressing of 8-, 16-, and 32-bit data.

Special instructions or integral-peripheral functions: The Blackfin DSP instruction set includes special instructions for video and next-generation communications algorithms. Videopixel-manipulation instructions include quad-byte operations for sum-absolute difference, average, and pack/unpack. Communications algorithms use dual-MAC instructions with rounding and saturate options in addition to add/compare/select or vector operators.

ANALOG DEVICES' ADSP-2199X

The ADSP-2199x family includes high-performance, mixed-signal DSPs that maintain full code compatibility with the ADSP-219x products. These devices integrate mixed-signal components, such as high-resolution ADCs, with a variety of peripheral components to form single-chip devices targeting embedded-signal-processing and -control applications, such as industrial measurement and control, high-end servo-motor drives, uninterruptible power supplies, high-end switched-mode power supplies, optical-networking control, and intelligent-sensor interfaces.

▶ Processors target mixed-signal, embedded-control, and signal-processing applications.

▶ Devices integrate a 150-MIPS DSP with a 14-bit, 18M-sample/sec ADC.

The ADSP-21990 and ADSP-21991 integrate a 150-MIPS, 16-bit ADSP-219x core with a 4k-word program memory, a 4k-word data memory, and an eight-channel, 14-bit, 18M-sample/sec ADC core, with dual S/H amplifiers for simultaneous sampling. An external memory interface enables direct access to as much as 1M word of external memory for program-memory expansion, data-memory

expansion, or both. The ADSP-21990 is available in industrial-temperature ranges and packaged in both BGA and QFP versions. The ADSP-21991 supports increased on-chip memory to 32k-word program memory and 8k-word data memory in pin-for-pin-compatible packages.

Addressing modes: Identical to the ADSP-219x products, the ADSP-2199x products support immediate, register-direct, memory-direct, register-indirect, indirect-postmodify, immediate-modify, and direct- and indirect-offset addressing modes. The ADSP-2199x supports as many as 16 circular buffers using a data-address-generator shadow register and a set of base registers for additional circular-buffering flexibility.

Special instructions or integral-peripheral functions: The ADSP-21990 and ADSP-21991 products share all of the architectural features and special instructions of the ADSP-219x core. The key integrated peripheral of these products is the high-performance, 14-bit ADC. The embedded-control peripherals include a three-phase PWM generation unit; a 32-bit incremental-encoder interface; dual auxiliary PWM outputs; a watchdog timer; and general-purpose peripherals, such as timers, digital-I/O lines, and serial-communications and programmable-interrupt controllers. Additionally, these devices include an on-chip precision-voltage reference and an integrated power-on-reset circuit.



ANALOG DEVICES' ADSP-TS101S TIGERSHARC FAMILY

The ADSP-TS101S TigerSHARC floating-point DSP targets multiprocessing and 3G wireless-infrastructure applications. This static superscalar architecture blends the best features of DSP, RISC, and VLIW (very-long-instruction word) for a high-performance DSP architecture. These features include a load/store architecture, branch prediction, large interlocked register file, fast mathematical computations, bit reversing,

▷ TigerSHARC can perform 1500 MFLOPS or 2000 16-bit million MACs/sec at 250 MHz.

▷ Targets wireless-infrastructure and multiprocessing applications.

zero-overhead looping, background data movement with DMA, and an instruction width that varies from one to four words. Two computational blocks in TigerSHARC support 1-, 8-, 16-, and 32-bit operations. Each computational block contains a 32-entry register file, an ALU, a multiplier, and a shifter. It can execute two 32-bit floating-point MACs, eight 16-bit MACs with 40-bit accumulation, or two 16-bit complex MACs in a single cycle. The device can perform as many as 32 mathematical

operations per cycle with 8-bit data types. Three 128-bit buses support TigerSHARC's three on-chip memory banks, which total 6 Mbits. In a given cycle, the device can fetch four 32-bit instruction words and load 256 bits of data into the register file or store it in memory.

Addressing modes: TigerSHARC has two integer ALUs in addition to the two computational blocks. It uses the ALUs primarily for data-address generation, and each unit contains a 32-bit ALU and a fully orthogonal, 32-word register file. These units can generate an address per cycle, which allows the device to send two 128-bit words to each computational unit. These units also support preaddress and postaddress modification, circular buffering, and bit reversing without an extra-cycle penalty.

Special instructions or integral-peripheral functions: Special instructions to accelerate both symbol- and chip-rate processing for 3G baseband-signal processing, include a complex MAC operation for chip-rate processing and add/compare/select operation for channel-decoding algorithms. Peripherals include four bidirectional link ports, a 14-channel DMA controller, and a 64-bit-wide external port that includes an SDRAM controller, a host interface, and support for glueless multiprocessing of as many as eight TigerSHARCs. The four link ports are byte wide interfaces that transmit data on both the rising and the falling clock edge and offer a second method for multiprocessing with ring and 2-D mesh multiprocessing configurations.

ANALOG DEVICES' SOFTFONE

The SoftFone, also known as the AD20msp430, integrates an ADSP-218x core and ARM controller to perform voice-coding and channel-equalizer functions for GSM cell phones and GPRS (general-packet-radio-service) mobile terminals. The RAM-based chip eliminates ROM turns, and you can implement it into different GSM/GPRS devices by changing the software.

Addressing modes: You can augment the 16 Mbits of directly addressed, on-chip flash memory with external flash and RAM.

▷ SoftFone is a RAM-based design requiring no ROM turns.

▷ Complete reference design is available.

Special instructions or integral-peripheral functions: The instruction set is the basic ADSP-218x instruction set. On-chip peripherals on all devices include a microstate machine to control events with less-than-1-bit-period resolution; bus-arbitration logic to allow direct access to and from memory and

all internal buses and registers; and programmable serial ports for connection to the voiceband/baseband codecs. Some devices include USB and other standard interfaces for smart-phone and wireless-PDA devices. Complementary chips for voiceband/baseband codes, quad-band RFIC, and power management/battery charging are available.

Support: The CrossCore development components include the VisualDSP++ software-development environment, EZ-Kit Lite evaluation systems, emulators, and DSP/math libraries. VisualDSP++ is an integrated software-development environment that includes an assembler, a C/C++ compiler, a linker, a debugger, an archiver, a loader utility for creating bootable images, VDK (VisualDSP++ kernel), advanced plotting tools, and statistical profiling. The EZ-Kit Lite evaluation system supports extension by the addition of JTAG in-circuit emulation. Emulators are available for serial-port, PCI, and USB host platforms. The VisualFone is the development system for SoftFone-based products. A complete GSM/GPRS protocol stack for SoftFone is available from TTPCom.

ARC'S ARCTANGENT

The ARCTangent-A4 and ARCTangent-A5 cores are synthesizable, user-customizable, 32-bit RISC processors with optional DSP extensions. Developers add the DSP extensions with the ARChitect configuration tool, a graphical-design tool that generates RTL files and synthesis scripts. The ARCTangent-A4 has a 32-bit instruction set, and the ARCTangent-A5 has the ARCompact 16/32-bit instruction set, which allows free mixing of 16- and 32-bit instructions for greater code density without mode-switching penalties. Both cores are synthesizable with industry-standard tools and are portable to almost any foundry or process.

▷ Cores support a user-customizable instruction set, registers, buses, interrupts, caches, and memories.

▷ Single tool chain supports RISC/DSP and multiprocessor software development.

The integrated RISC/DSP cores allow programmers to use a single tool chain for RISC and DSP software development.

Addressing modes: The ARCTangent supports as many as four banks of XY memories from 512 bytes to 16 kbytes and has a user-extendable register file. The address-generation units for the XY memories support modulo and bit-reverse addressing with variable-offset preincrement and postincrement modes.

Special instructions or integral-peripheral functions: DSP features include 16×16, 24×24-, and dual 16×16-bit MACs with 8 guard bits for the accumulator, saturating add and subtract instructions, fractional arithmetic, normalize (find first bit), swap, minimum/maximum, 32×32-bit barrel shifter, 32×32-bit multiplier, and zero-overhead loops. The instruction set is conditional, with as many as 16 user-defined condition codes. Developers can also configure and extend the instruction set to optimize performance for specific applications.

Support: The ARCTangent RISC/DSP comes with RTL source code, extensive documentation, the ARChitect processor-configuration tool, MetaWare High C/C++ software-development tools, an assembly-language DSP-function library that is callable from C/C++ programs, customer training, and technical support. The single tool chain supports both RISC and DSP-software development. ARC also provides peripheral-IP cores, including USB, Ethernet, and Bluetooth controllers; the Precise/MQX RTOS system software; network-protocol stacks; and software for vertical-market consumer and communication applications.



BOPS' MANARRAY

The ManArray architecture is a fully scalable, configurable, synthesizable DSP architecture that is programmable and reusable in an array of implementations for communications, mobile-multipedia, and wireless applications. Each application-specific family balances the trade-offs in cost, power, and performance for targeted applications. The MoCARay configuration targets GPRS/EDGE (general-packet-radio-service/enhanced-data-rate-for-GSM-evolution) baseband layer 1 processing at less than 20 mW and turbo-codec processing at less than 50 mW, for software-defined, trimode 2G/2.5G/3G handsets. The MICoRay configuration targets full-duplex MPEG4 CIF codec processing at less than 100 mW for high-quality videoconferencing on Smartphones and PDAs. The WirelessRay configuration targets physical-layer processing for 802.11b, 802.11g, and 802.11a at less than 70 mW for wireless-LAN devices.

▶ The ManArray DSP core can achieve 100 MIPS/mW.

▶ The core has power consumption of 11 to 36 mW for as many as 4000 MIPS.

Addressing modes: The BOPS architecture supports SIMD (single-instruction-multiple data), MIMD (multiple-instruction-multiple-data), and SMIMD (synchronous-multiple-instruction-multiple-data) operation. A fully programmable, patternable, scalable DMA engine supports the addressing modes and data-flow management necessary to meet the computational requirements of the high-performance, scalable DSP cores.

Special instructions or integral-peripheral functions: Each family has an enhanced instruction set targeting mobile-wireless, mobile-video, or high-performance streaming media. You can easily integrate all functions—from a RISC coprocessor to a simple PCI interface—into BOPS SOCs (systems on chip).

Support: The BOPS software-development kit integrates tools for application-software programmers, SOC designers, firmware designers, and system architects into one development environment. The Jordan and Travis evaluation boards enable BOPS customers to evaluate the ManArray architecture and develop SOCs that use the BOPS' ManArray-based family of programmable DSP cores. BOPS Halo Parallelizing C compiler enables programmers accelerate their software-development schedule by automatically exploiting the three levels of parallelism in the ManArray architecture, including packed data, processor arrays, and indirect VLIW (very-long-instruction-word) instructions.

CIRRUS LOGIC'S CS49400

Cirrus Logic's CS49400 DSP integrates a 32-bit audio processor; a dedicated multistandard decoder; key peripherals; and X, Y, and program memories in a single chip targeting digital-entertainment applications. The device can support multichannel DTS 96/24, Dolby Digital, AAC, and THX Ultra2 Cinema without additional logic or memory, and it supports customer software-security keys.

CIRRUS LOGIC'S CS49400

Support for AAC, DTS-ES 96/24, and THX Cinema requires no additional external logic or memory.

▶ Support for AAC, DTS-ES 96/24, and THX Cinema requires no additional external logic or memory.

Special instructions or integral-peripheral functions: Along with dual S/PDIF (Sony/Philips digital-interface) transmitters and serial and parallel host interfaces, the CS49400 includes 12 audio-input and 16 PCM-output channels.

Support: The CS49400 features an audio framework, including customizable programming, certified audio decoders, and sound-enhancement programs for DTS 96/24, Dolby Digital, AAC, and THX. The CrystalWare Software Library provides legacy audio-decoder support.

DSP ARCHITECTURES' DSP24 FAMILY

The high-performance DSP24 array-processor core, optimized for signal and image processing in the frequency domain, targets applications that perform operations on large arrays of data. It is a pass-based processor, with each function valid for one complete pass. Each operation code defines a basic flow for the desired operation that repeats for multiple pairs of data to complete one pass. For typical array-processing applications, such as FFTs, the device sets up a function code (for example, BFLY32). Radix32 butterfly then clocks the whole data array into the DSP24 and applies the function to the whole array. There is a latency when implementing the DSP24 functions, that the MMU24 automatically compensates for when you use it in a system. The pipelined systolic structure allows you to cascade multiple DSP24s for increased performance and higher radices. This structure permits 80/100-MHz operation on an unlimited array size with support for enhanced read-only FFT, double-length FFT, dual FFT, and stacked FFT to reduce latency.

▶ The device targets low-power, software-minimized, frequency-domain signal-processing applications.

▶ Radiation-hardened versions are available.

Addressing modes: The DSP24 addressing includes digit reversing, read-only-FFT addressing, fast sine/cosine, decimation, interpolation, modulo increment/decrement, array padding, zero filling, radix2 through radix1024 patterns, and parameterized user sequences.

Special instructions or integral-peripheral functions: The DSP24 includes radix2 through radix1024 instructions. It can perform no-overhead window functions and filter/image multiplies and uses five bidirectional data ports for any-port-to-any-port data routing.

Support: The DSP24 and optional MMU24 software-development kit come with C models and optional VHDL models. Valley Technologies (www.valleytech.com) offers board and module products, including the VectorWare language.

DSP GROUP'S OAKDSPCORE

The 16-bit, fixed-point, single-MAC, licensable OakDSPCore architecture includes and microcontroller instructions for higher code density. The OakDSPCore has two data buses and one program bus, configurable ROM/RAM size, a data-address-arithmetic unit, a multiplier, a 36-bit ALU, two sets of two 36-bit accumulators, and support for a C compiler. It also includes a bit-manipulation unit with a 36-bit barrel shifter, an exponent-evaluation unit that supports fast normalization, and a bit-field-operation unit. The zero-overhead-loop mechanisms include an interruptible single-word instruction loop and four-level nesting of block repeats. User-definable registers speed hardware acceleration and provide coprocessor support. It has four pipeline stages, single-cycle interrupt latency, and automatic context switching. Power management includes active-, slow-, and idle-operation modes. OakDSPCore is compatible with the PineDSPCore.

▶ The OakDSPCore handles bit-manipulation, control, and DSP instructions.

▶ Power management includes three modes.

Addressing modes: The OakDSPCore supports register, single- and double-indirect, short- and long-immediate, short- and long-index, and stack-pointer addressing modes. It supports circular (modulo) buffering for all its pointers and direct addressing for the entire 64k-word data space. It also has a program-memory-indirect addressing mode.

Special instructions: Instructions for the OakDSPCore include



single-cycle minimum/maximum calculation with pointer latching, double-precision calculations, normalization, exponent, conditional accumulator modifications, division step, read-modify (add/subtract/OR/AND/XOR)-write, test 16-bit mask bits and test bit, delayed return, interruptible single-word repeat loop and block repeat, 36-bit shift left or right in a single cycle, and a bank exchange of alternative registers.

DSP GROUP'S PALMDSPCORE

PalmDSPCore is a family of three licensable, dual-MAC, soft DSP cores—of 16, 20, and 24 bits each—that have an instruction-level-parallelism architecture, MIMD (multiple-instruction-multiple-data) and SIMD (single-instruction-multiple-data) instructions, seven computation units working in parallel, and symmetrical cross-coupled MAC paths. PalmDSPCore has two multipliers; a three-input ALU; a three-input split adder-subtractor unit; four orthogonal, 40-bit accumulators; and a bit-manipulation unit, including insert-extract operations. The data-address-arithmetic unit contains two additional adder-subtractor-units. It has integrated accelerators for FFT and Viterbi-decoding, RTOS, and bit-exact standards. It has zero-overhead-loop mechanisms with infinite levels of repeat and block repeat and six pipeline stages. It also has coprocessor support and 16 user-defined registers for hardware acceleration. PalmDSPCore has high code density through variable instruction width (16 or 32 bits). Maximum PalmDSPCore program-memory space is 16M words. PalmDSPCore is a process- and library-independent, fully synthesizable soft core and is compatible with previous SmartCores generations, including Teak, Teak-Lite, and OakDSPCore.

▶ Seven arithmetic units support SIMD and MIMD operations.

▶ Devices feature high code density with 16- and 32-bit instruction widths.

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Addressing modes: PalmDSPCore supports circular (modulo) buffering, register, short- and long-direct, short- and long-immediate, relative, bit-reversal, double-word, parallel, index-based, and stack-pointer addressing. It also supports a maximum quadruple-indirect addressing mode (for example, to simultaneously feed four inputs of the two multipliers or four inputs of the split ALU).

Special instructions: The device supports single, parallel, and multiparallel instruction sets. It also supports dual-MAC, complex FFT butterfly in two cycles, Viterbi decoding in two cycles, microcontroller instructions, delayed branches and return, normalization, exponent, conditional instructions (parallel moves, logic, arithmetic, and accumulator), and infinite levels of repeat and block repeat.

DSP GROUP'S PINEDSPCORE

PineDSPCore, the first generation of the SmartCores family, is a 16-bit, fixed-point, single-MAC, licensable DSP core. It has a compact DSP-and-control instruction set for high code density. PineDSPCore has two data buses and one program bus, a configurable ROM/RAM size, and a data-arithmetic-addressing unit. The computation unit includes a multiplier, a 32-bit product register, a 36-bit ALU, two 36-bit accumulators with 4 guard bits, and a normalization mechanism. The ALU performs arithmetic and logic operations on the data operands and functions, such as step division and rounding. PineDSPCore also includes

▶ The DSP-and-control instruction set is compact.

▶ PineDSPCore is a licensable DSP core.

two zero-overhead loop mechanisms: a single-word instruction loop and a block repeat. It has user-definable registers for hardware acceleration, coprocessor support, or both. It has three pipeline

stages and single-cycle interrupt latency. Power management includes active-, slow-, and idle-operation modes.

Addressing modes: PineDSPCore supports register, single- and double-indirect, and short- and long-immediate addressing modes. It supports circular (modulo) buffering for all its pointers and direct addressing for the entire 64k-word data space. In addition, it has a program-memory indirect addressing mode.

Special instructions: Instructions include conditional accumulator modifications, conditional and unconditional call and branch, arithmetic and logical operations, round, rotate, shift, compare, division step, MAC, square, single-word repeat loop, and block repeat.

DSP GROUP'S TEAK

The low-power, 16-bit, fixed-point, dual-MAC, licensable Teak DSP soft core has an instruction-level-parallelism architecture. The process- and library-independent, fully synthesizable soft core supports the ASIC design environment. Teak has configurable memory size; a data-address-arithmetic unit; two multipliers; a 40-bit, three-input split ALU; four 40-bit accumulators; an exponent unit; and a bit-manipulation unit. It has integrated accelerators for complex FFT; Viterbi-decoder; wide-automatic-context-switching; RTOS; and bit-exact standards, such as GSM communications. It has zero-overhead-loop mechanisms with infinite levels of repeat and block repeat. Teak has compact code with a 16-bit instruction width, including parallel instructions. You can extend Teak's program memory to 4M words. With user-definable registers for hardware acceleration, coprocessor support, or both and mechanisms for power-consumption reduction, Teak is code-compatible with the OakDSPCore and Teak-Lite instruction sets of SmartCores.

▶ The compact code has a 16-bit instruction width.

▶ FFT butterfly completes in five cycles, and Viterbi decoder completes in three cycles.

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Addressing modes: Teak supports circular (modulo) buffering, register, short- and long-direct, short- and long-immediate, relative, bit-reversal, and short- and long-index-based addressing modes. It can also perform quadruple-indirect addressing (for example, to simultaneously feed four inputs of the two multipliers or four inputs of the split ALU).

Special instructions: Instructions include dual-MAC performance, read/write double words to and from memory, and single-cycle minimum/maximum search with pointer latching. The device handles complex FFT butterfly in five cycles and Viterbi decoding in three cycles. Devices also perform bit-manipulation and microcontroller instructions, double-precision multiplication, normalization, exponent, conditional instructions, division step, and infinite levels of repeat and block repeat.

DSP GROUP'S TEAKLITE

The 16-bit, fixed-point, single-MAC, licensable Teaklite soft DSP core that is code-compatible with the OakDSPCore instruction set.

▶ Devices feature high code density.

▶ Power-management modes support lower power devices.

It enhances the OakDSPCore in several areas, mainly portability. It is a process- and library-independent soft core; it increases operating speed by 30% in the same process technology and reduces power consumption by architecture and power-reduction mechanisms. Its design methodology better meets ASIC-design-environment requirements by employing a single-edge design (still with four pipeline stages) and full or partial testability and by using standard memories. TeakLite



has a configurable memory size, a data-address-arithmetic unit, a multiplier, an ALU, four 36-bit accumulators, a bit-manipulation unit, and zero-overhead loop mechanisms for repeat and block repeat. Its instruction set includes microcontroller instructions enabling high code density. It has user-definable registers for hardware acceleration, coprocessor support, or both; cycle-stealing DMA support, burst-mode DMA support, or both; and power-management operation modes.

Addressing modes: TeakLite supports register, single- and double-indirect, short- and long-immediate, short- and long-index, and stack-pointer addressing modes. It supports circular (modulo) buffering for all its pointers and direct addressing for the entire 64k-word data space. In addition, it has a program-memory-indirect addressing mode.

Special instructions or integral-peripheral functions: Instructions include single-cycle minimum/maximum calculation with pointer latching, double-precision calculations, normalization, exponent, conditional accumulator modifications, division step, read-modify (add/subtract/OR/AND/XOR)-write, test 16-bit mask bits and test bit, delayed return, interruptible single-word repeat loop and block repeat, 36-bit shift left or right in a single cycle, and a bank exchange of alternative registers.

Support: DSP Group provides a full set of advanced GUI-based development tools, including an optimizing C/C++ compiler, an assembler, a linker, common-object-file-format converters, a debugger with an emulation interface and the Assyst extendable simulator for system-on-chip simulation, a profiler, and the Evaluation Development Platform. DSP Group has a large infrastructure of third-party vendors offering software, tools, and design services.

EQUATOR TECHNOLOGIES' MAP-BSP FAMILY

Equator's MAP-BSP family of VLIW/SIMD (very-long-instruction-word/single-instruction-multiple-data), merged-video DSPs

▶ The MAP-BSP-15-400 can perform 40 GOPS at 400 MHz.

▶ MAP-BSP devices are entirely program-mable in C.

and microprocessor devices target videocentric applications. All of the MAP-BSP devices are pin-compatible and can operate on 8-, 16-, 32-, 64-, and 128-bit-wide data. MAP-BSP devices integrate the processor with SDRAM and PCI interfaces and a flexible multimedia-I/O system that supports a single external bank of DRAM. Advanced features include compiler-managed register sets, task-optimized functional units,

throughput-optimized data cache, and support for digital RGB.

Addressing modes: MAP-BSP devices support direct, indirect, and virtual addressing modes.

Special instructions or integral-peripheral functions: The MAP-BSP instruction set includes operations geared toward FIR and FFT functions. Interface support includes two ITU-656 video-in ports, two TCI-In transport-stream-in ports, a TU-656 video-out port, and in/out general-purpose data ports. The hardware includes a variable-length encoder/decoder, used in MPEG-1, -2, and -4 encoding/decoding, and polyphase filtering for video scaling.

Support: Equator's iMMediaTools suite supports development for all of the MAP-BSP devices and includes a parallelizing C compiler, a linker, a source-level debugger, simulators, and standard libraries.

HITACHI SEMICONDUCTOR'S SH-DSP AND SH3-DSP

Processors in the SH-DSP series (SH7615, SH7616, SH7622, and SH7065) combine a 32-bit RISC CPU and a 16-bit integer DSP unit into a single core. The DSP unit can execute single-cycle 16×16-

integer multiplies and can multitask its operations. Hitachi's SH7616 is a CMOS single-chip microcontroller that integrates a 10/100-Mbps Ethernet controller supported by two 2-kbyte FIFOs and a multichannel DMA controller targeting Ethernet applications, such as network video/printers, network terminals, and management processors. The SH7065 integrates 256 kbytes of on-chip flash.

▶ The SH7622 can perform 87 MIPS at 60 MHz.

▶ The SH7727 can perform 208 MIPS at 160 MHz.

Processors in the SH3-DSP series (SH7727, SH7729) combine a 32-bit RISC CPU and 16-bit integer DSP unit into a multitasking core with a four-bus structure targeting Web/Smart-phone, handheld PCs, Internet terminal/IP fax, digital still cameras, and security-terminal applications.

SH3-DSP devices include 16 kbytes of X/Y RAM, 16 kbytes of cache (Ways 2 and 3 lockable), a bus-state controller for glueless connection to SDRAM, and on-chip JTAG and real-time-instruction trace-debugging modules. The SH7729R includes data protection and virtual memory.

Addressing modes: Devices support direct- and indirect-register, predecrement or postincrement indirect-register, indirect-register-with-displacement, indirect-indexed-register, indirect-global-base-register-with-displacement, indirect-indexed-global-base-register, indirect-program-counter-with-displacement, and program-counter-relative immediate addressing.

Special instructions or integral-peripheral functions: The SH-DSP and SH3-DSP use a 16- and 32-bit instruction set that supports one-cycle multiplication/addition, operand-unrelated parallel moves, conditional execution for DSP datapath instructions, multiprecision arithmetic in microcontroller instructions, and single-cycle exponent detection (DSP operations are all 32-bit instructions.). The SH7622 SH-DSP core device includes high-speed on-chip USB.

SH3-DSP devices include a memory-management unit, a timer, a real-time clock, an interrupt controller, and a serial-communication interface. The SH7727 includes USB host and LCD controllers that support bus-master functions. The SH7729R includes an infrared communication, ADC, DAC, and power management.

Support: Hitachi and third parties offer evaluation kits, emulators, companion chips, reference-design platforms, software board support, RTOSs, middleware, and application packages. Hitachi offers middleware for the SH-DSP and SH3-DSP covering telephony applications, including G.729, G.725 and G.723.

IMPROV SYSTEMS' JAZZ

The Jazz DSP, a configurable VLIW (very-long-instruction-word) processor architecture, incorporates features such as overlaid data-

▶ Processor-to-processor data communication uses direct on-chip data memories.

▶ All processors attach to a single Q-bus that enables queuing of tasks.

paths, a distributed-register system, code compression, and power management. The Jazz PSA (programmable system architecture) is customizable to provide accelerated execution of key application algorithms. The flexible DSP-core architecture facilitates design modifications without compromising the verification integrity and processor tool chain.

It can scale from a single uniquely configured Jazz DSP processor core to a system-level platform implementation that consists of many processors in an interconnected structure.

Addressing modes: Supported addressing includes direct, indirect, indexed, immediate, displacement, bit reverse, bit-reverse index,



vector index, and post-increment. A wrap mode provides support for circular buffers.

Special instructions or integral-peripheral functions: Special instructions support single-cycle built-in library functions for common signal-processing data transforms. This platform architecture supports the implementation of multiple processors, nonvolatile instruction memory, configurable I/O interfaces, and hardware support for u-tasking. Special task-control instructions provide support for the unique u-task scheduling in the Jazz PSA.

Support: The Jazz Tool Suite uses a graphical design environment to support unique Jazz DSP processor-configuration development and includes an integrated development environment, a compiler, an assembler, an instruction-set simulator, a profiler, a debugger, and FPGA-emulation support. Improv's Rehearsal boards provide a near-real-time system for designers to run configurations of the Jazz PSA core to verify designer-defined DSPs and to run with other elements of the overall system. Improv's application-oriented platform-solution kits contain a collection of hardware and software components, such as custom Jazz DSPs, application software, and reference designs. Acappella is a family of application-optimized hardware/software for the voice-over-packet market.

INFINEON TECHNOLOGIES' CARMEL DSP 10XX AND 20XX CORE

The 10xx 16-bit, fixed-point Carmel DSP core combines a predefined instruction set and CLIW (configurable-long-instruction-word) technology. The 10xx core targets wireless, wired, and consumer applications. User-defined CLIW instructions execute in one clock cycle without wait states or setup overhead, just like any predefined instruction, allowing software code to switch between execution units on a clock-by-clock basis. This ability is particularly useful for reducing the cycle count of inner loops, increasing the overall application code performance by a factor of two or more over software implementations that use only the predefined instruction set.

The second-generation, reconfigurable, 16-bit, fixed-point Carmel DSP 20xx core uses CLIW technology and adds PowerPlug technology to design optimized execution units for specific algorithms. The 20xx core targets wireless, broadband, multimedia, and consumer-electronics applications. The core includes six standard arithmetic units and accommodates as many as four additional PowerPlug modules to accelerate computationally intensive functions, such as MAC, Viterbi, image, and video. The combined effect is an increase in flexibility and higher efficiency than using predefined, general-purpose instruction sets.

Addressing modes: The Carmel DSP 10xx and 20xx cores support immediate address in the instruction, direct reference to operand registers, and indirect reference to an operand data memory. Addresses may be 16 or 32 bits, with linear, bit-reverse, and modulo (aligned and nonaligned) address modification, each with increment, decrement, and offset modifications.

Special instructions or integral-peripheral functions: CLIW technology allows user definition of 96-bit instructions, composed of as many as six individual parallel subinstructions, to increase the efficiency of the core in tight DSP loops. The 20xx core can also include as many as four PowerPlug modules, which are user-defined execution units targeting specific applications that seamlessly integrate into the regular tool chain. The core includes built-in support for Viterbi decoding as well as for minimum/maximum

searches. The Carmel DSP is inherently modular, with extensive libraries of synthesizable system peripherals and memories, as well as software functions. You can integrate peripheral functions into the core via the Infineon Flexible Peripheral Interconnect bus.

Support: Third-party partners provide hardware- and software-development tools to aid in system-design and application-software development. Infineon also provides development-chip implementations of the core with large on-chip memory and multiple I/O options, as well as evaluation boards and hardware/software cosimulation models.

LSI LOGIC'S LSI402ZX AND LSI403LP

The high-performance, 16-bit, fixed-point LSI402ZX DSP is based on the LSI Logic ZSP400 DSP core targeting voice-over-networks CPE/IADs (customer premise equipment/integrated-access devices), infrastructure, wireless-infrastructure, and audio applica-

▶ The LSI402ZX can perform 800 MIPS at 200 MHz.

▶ The LSI403LP can perform 600 MIPS at 150 MHz.

tions. The low-power, 16-bit, fixed-point LSI403LP DSP is based on the LSI Logic ZSP400 DSP core targeting voice-over-networks CPE/IAD devices and audio applications. The ZSP400 architecture applies aspects of microprocessor design to the LSI402ZX and LSI403LP implementations. Both devices are software-compatible with all ZSP devices and implement a five-stage,

four-way superscalar pipeline to process as many as 20 instructions at a time. The processor's execution unit contains two MACs and two ALUs. The LSI402ZX includes 62k words of instruction RAM and 62k words of data RAM. The LSI403LP provides 16k words of instruction RAM, 16k words of data RAM, and 16k words of instruction- or data-configurable memory. An eight-channel DMA controller, which transfers instructions or data to and from memory, supports both devices.

Addressing modes: The LSI402ZX provides two independently enabled circular buffers and supports reverse-carry addressing. Reverse-carry addressing is an alternative mode of indexing the base-address registers that speeds FFTs and similar operations that require you to modify the next load or next store address in a reverse-carry fashion.

Special instructions or integral-peripheral functions: Both devices can perform a single-cycle add-compare-select for Viterbi decoding. They also support bit manipulation, 32-bit arithmetic, logic operations, and two-cycle complex-multiply instructions. Both devices include two high-speed TDM serial ports, a single 16-bit host-interface port, an external memory-interface unit, a four-pin (LSI403LP) or eight-pin (LSI402ZX) programmable I/O port, and an IEEE 1149.1 JTAG port for program downloading and debugging.

Support: LSI Logic and third-party tools support both devices. LSI provides a Gnu-based compiler, a linker, and an assembler, available for Windows and Solaris platforms. Green Hills Software offers a commercial tool chain, and Corelis offers JTAG debugging tools. Complementing the ZSP Solution Partners Program, ZOpen, LSI Logic's open-architecture-software framework, provides integration guidelines with supporting utilities, compliant third-party algorithms, and a methodology that standardizes application development. ZSP software-application partners provide ZOpen-compliant algorithms that you can integrate into your system designs.

MOTOROLA'S 56800 AND 56800E

Motorola's DSP56800 family integrates the performance and instruction set of a DSP with the control functions of an embedded

▶ The 10xx core can achieve 2800 MOPS with a single-cycle instruction rate at 200 MHz.

▶ The 20xx enables user-defined execution units for highest efficiency.



microcontroller into a single core. These devices target applications that traditionally use 16-bit microcontrollers but also require DSP functions, such as point of sale, voice recognition, digital telephone-answering devices, and a variety of low-power applications. Motorola's 56800E family is an enhancement to Motorola's 56800 DSP architecture for applications that require more memory and greater performance. The 56800E core offers five times the performance (to 200 MIPS) at one-third the power consumption of the original core and double the microcontroller-code density. It offers expanded memory addressing to 4 Mbytes of program memory and 32 Mbytes of data

▶ The devices use a unified microcontroller/DSP architecture.

▶ The 56800E is an enhanced-core extension of the 56800.

memory. It includes 8-, 16-, and 32-bit data types; supports fast interrupts; and supports real-time debugging.

Addressing modes: The addressing modes cover register-direct, address-register-indirect, immediate, and absolute categories. Devices in the 56800E family support 19 total addressing modes across these categories.

Special instructions or integral-peripheral functions: The 56800 uses a bus structure that allows data to keep pace with the DSP while maintaining the peripheral set of a microcontroller. The 56800 peripherals include an interrupt controller, an external memory interface, general-purpose I/O, a scalable controller-area network, an ADC, a quadrature decoder, a PWM, serial interfaces, a quad timer module, JTAG support, and on-chip emulation.

Support: The Metrowerks CodeWarrior IDE tool set, as well as target development boards from Motorola for software development and companion daughtercards developed for market-specific applications, support the 56800 and 56800E. Other third-party tool developers and consultants support both device families.

OAK TECHNOLOGY'S PM-44IX

Oak Technology's iDSP family targets image-processing applications, such as imaging-enabled printers and multifunction peripherals. The iDSP provides designers with all the flexibility of a software-based image-processing option at the price and performance of fixed-function silicon. The PM-44ix contains four symmetric parallel-pipelined processors and employs the SIMD (single-instruction-multiple-data) parallel-processing architecture to take advantage of the parallelism inherent in image data.

▶ The four parallel-pipelined processors can perform 3700 MIPS/930 MMACs (million MACs) at 253 MHz.

▶ The PM-44ix supports as many as 16 color-ink-jet and 30 monochrome-laser copies per minute.

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Addressing modes: To maximize memory bandwidth, all memory accesses in the iDSP measure 32 bits. Specialized extraction and

insertion units allow you to manipulate bit fields of any size within 32-bit registers.

Special instructions or integral-peripheral functions: The iDSP instruction set contains specialized instructions for manipulating image data and coordinating parallel processing.

Support: The iDSP programming environment includes an IDE, an image-processing library, and an evaluation board. Oak Technology's worldwide direct-sales and support organization supports the iDSP.

QUICKLOGIC'S QUICKDSP

QuickLogic's QuickDSP family combines a DSP with the flexibility of programmable logic targeting voice-over-IP and imaging ap-

plications. This dedicated hardware option can achieve a fourfold improvement over traditional programmable logic for a range of

▶ QuickDSP is an integrated DSP and programmable-logic device.

▶ You can use the Quick DSP as a coprocessor or a preprocessor to other DSPs.

functions, including floating-point arithmetic, FIR, IIR, adaptive filtering, FFTs, forward-error correction, and high-level data-link control. QuickLogic embeds a reprogrammable computational unit and RAM blocks into silicon to allow DSP-design engineers to implement complex algorithms and multiple-sample processing across single or

multiple datapaths. Because the logic usage is efficient even for complex designs, design engineers can use smaller, less expensive devices with lower power consumption.

Addressing modes: You can configure the ECUs (embedded computational units) for eight arithmetic functions via a dynamically reprogrammable instruction-set sequencer. This flexibility lets designers reconfigure the ECU for algorithm-intensive applications, such as adaptive filtering.

Special instructions or integral-peripheral functions: The QuickDSP comes with 18 ECUs on the largest part (QL7180), an instruction-set sequencer, and multiple dual-port 2304-bit RAM modules. These RAM modules vary from 12 to 36 blocks for a total of 82.9 kbits of RAM. The QuickDSP comes with four PLLs that create a master clock from a lower input-frequency clock. One of the four PLLs is multiplexed with the dedicated clock, and the remaining three connect to global clocks.

Support: The QuickDSP RDK (reference-design kit) combines the QuickDSP device with a hardware- and software-development platform, allowing users to implement and debug their DSP and programmable-logic designs. The QuickDSP RDK is capable of in-system operation, in which you can attach the main RDK assembly to a third-party programmable DSP-evaluation module or DSP starter kit via two interface connectors. In this implementation, the QuickDSP device directly connects to the bus of the third-party host-programmable DSP processor, and the DSP program or any associated debugging environment can control it. Design support from the Corporate Applications Group at QuickLogic is available to customers.

RC MODULE'S NEUROMATRIX NM640X

RC Module's NeuroMatrix NM6403 is a dual-core application-specific DSP processor based on the NeuroMatrix architecture targeting video-image processing and neural-network applications.

It provides scalable performance, a programmable operand width of 1 to 64 bits, and operation as fast as 50 MHz. This flexibility allows designers to trade precision for performance to suit their applications. The NM6403 processor includes a 32/64-bit RISC processor and a 1- to 64-bit vector coprocessor that supports vector operations with elements of

▶ The vector coprocessor can handle variable-length, 1- to 64-bit data.

▶ Variable-length data enables speed and precision trade-offs.

variable bit lengths (patent pending). Two identical programmable interfaces work with external memory, and two communication ports are hardware-compatible with TI's TMS320C4x, allowing you to build multiprocessor systems.

The vector coprocessor, which has an SIMD (single-instruction-multiple-data) architecture, works on packed integer data comprising 64-bit blocks in the form of variable 1- to 64-bit words. The device supports vector-matrix or matrix-matrix multiplication.



The Vector coprocessor's core looks like an array multiplier comprising cells that include a 1-bit memory (flip-flop) surrounded by several logical elements. You can combine the cells into several macrocells with two 64-bit programmable registers. These registers define the borders between rows and columns with macrocells. Each macrocell performs the multiplication on variable-input words using preloaded coefficients and accumulates the result from the macrocells in the column above it. The columns simultaneously calculate the results in one processor cycle. For 8-bit data and coefficients, the vector coprocessor performs 24 MAC operations with 21-bit results in one 20-nsec processor cycle. The number of MAC operations depends on the length and number of words packaged into a 64-bit block. The engine's configuration can change dynamically during calculations. An application can start with maximum precision and minimum performance and dynamically increase performance by reducing the data-word lengths. To avoid arithmetic overflow, the NM6403 uses two types of saturation functions with user-programmable saturation boundaries.

The RISC core (VLIW) has a five-stage pipeline that operates with 32- and 64-bit-wide instructions. Each instruction usually executes two operations. Two 64-bit interfaces support SRAM, DRAM, and EDO DRAM and comprise two separate address-generation units that can address as much as 16 Gbytes. Each interface supports two memory banks and can support a "shared-memory" mode. Two DMA coprocessors transfer data between high-speed I/O communication ports and external memory.

Addressing modes: The NM6403 supports 32-bit immediate, base, indexed, and relative addressing.

Special instructions or integral-peripheral functions: The NM6403 processor uses vector instructions to handle packets of as many as 32 64-bit data words. These instructions may define operations such as matrix-matrix, matrix-vector, or vector-vector multiplication, vector-vector addition/subtraction with saturation of results, block moving, and bit manipulation. The NM6403 has conditional branch, call, and return instructions.

Support: The NeuroMatrix Software Development Kit for PCs includes an ANSI X3J16/95-0029 preliminary-standard compatible C++ compiler, an assembler, an instruction-level simulator, a cycle-accurate simulator, a linker, a source-level debugger, a load/exchange library, and a set of application-specific vector-matrix libraries. RC Module offers PCI and CompactPCI evaluation/development boards. The vector-matrix library simplifies C-language programming for FFT, DCT, Sobel, and Hadamard Transform. RC Module also provides a NM6403 Verilog behavioral model for Sun host platforms for system-level simulation and a synthesizable core targeting Samsung and Fujitsu semiconductor technologies.

SENSORY'S RSC FAMILY

The RSC-3x and RSC-4x speech processors combine a microcontroller with advanced-speech-processing technology targeting high-quality speech recognition, speech and music synthesis, speaker verification, and record and playback.

▷ RSC processors are specialized for speech recognition and synthesis.

▷ High-quality speech output is possible to as little as 5 kbps.

These devices feature a high-performance microcontroller with on-chip memories and a 24×24 hardware multiplier. The RSC-4x family also features a vector processor. Each device uses a neural network to perform speaker-independent speech recognition and achieve high-quality speech syn-

thesis using both time- and frequency-domain-compression techniques, enabling them to provide high-quality speech output to as little as 5 kbps. In addition to providing the necessary horsepower to perform speech recognition and speech synthesis, the processors have sufficient cycles available for general-purpose product control for as many as 24 I/O lines.

Addressing modes: RSC devices support sequential addressing modes.

Special instructions or integral-peripheral functions: The RSC-3x and RSC-4x processors include an on-chip ADC, a DAC, and digital filters. The RSC-4x family also features twin DMA units, comparator blocks, a watchdog timer, and other product-control features.

SENSORY'S SC-6X FAMILY

The SC-6x DSP family targets speech-synthesis applications. The Sensory speech algorithms support long-duration speech, compressed speech using 1-kbps MX, higher

▷ The SC-6x supports low-data-rate speech synthesis.

▷ Five bit rates for CX and MX support a range of speech-quality and memory requirements.

economy compression using 3-kbps CX. Five other fixed bit rates of CX and a variable range of MX bit rates are available to mix and match your quality and memory requirements. These DSPs support three low-power modes, two timer interrupts, one DAC interrupt, and five general-purpose interrupts to increase battery life and response speed to button and keyboard

presses. The SC-6x devices have sufficient horsepower to support interactive interfaces and 14-channel polyphonic music while speaking.

Addressing modes: The addressing modes are immediate, direct, indirect-with-postmodification, and three relative modes. The program-counter unit provides addressing for program memory (on-board ROM). It includes a 16-bit arithmetic block for incrementing and loading addresses. It also consists of the program counter, the data pointer, a buffer register, a code-protection write-only register, and a hardware-loop counter (for strings and repeated-instruction loops). The program-counter unit generates a ROM address as output.

Special instructions or integral-peripheral functions: The SC-6x processors offer instructions to facilitate filtering algorithms, such as FIR, FIRK, COR, and CORK. FIR is useful for adaptive filtering or applications in which coefficients come from an external source. COR instructions perform 16×16-bit multiplies and 48-bit accumulation in three clock cycles. Instructions are also available to perform 16×16-bit multiplies and 32-bit accumulation in two clock cycles.

Support: Sensory's tools include a development environment with a C compiler, demonstration units, and evaluation and prototyping tools, such as the Voice Extreme Toolkit. Each tool set includes required hardware and software, complete documentation, and numerous samples. Turnkey product-development and linguistics services are available directly through Sensory or through its worldwide network of third-party development houses. For generic DSPs and processors, Sensory offers text-to-speech software and the small-footprint Voice Activation and Fluent Speech voice-recognition engines.

SIROYAN'S ONEDSP ARCHITECTURE AND SRXXX FAMILY

Siroyan's OneDSP architecture uses VLIW (very-long-instruction-word)-clustering techniques to provide scalable, high-performance



DSP power allowing as many as 32 execution-unit clusters in a single core. Prevalidated configuration options include setting the number of clusters and endianess, as well as the cache-memory size and configuration.

▶ The VLIW DSP architecture can scale as many as 32 dual-issue clusters.

▶ OneDSP can perform as many as 25.6 billion MACs at 200 MHz.

Each cluster consists of general-purpose registers, accumulators, a number of execution units, cache memory, local memory, and an on-chip bus interface. The master cluster executes either scalar RISC instructions from its instruction cache or VLIW instructions from its V-cache. In multicluster designs, VLIW instructions are issued in parallel from the V-cache in each of the slave execution-unit clusters. You can configure the SRA328 core with as many as eight execution-unit clusters with 32-bit datapaths. It targets communication and consumer applications.

Addressing modes: In addition to normal RISC addressing modes, OneDSP supports autoincrement, autodecrement, circular-buffer-addressing, and bit-reversed-addressing modes.

Special instructions or integral-peripheral functions: OneDSP supports Galois-field arithmetic for Reed-Solomon-coding applications and encryption algorithms. Siroyan will provide other application-specific instructions. The SRXXX cores have an integrated DMA engine capable of basic scatter/gather functions and bit-reversed addressing and ships with an example system that includes an AMBA AHB and APB bus system, an external memory interface, and an area of on-chip SRAM.

Support: Siroyan's OneDSP development environment runs on Unix, Linux, or Windows OSs. A debug adapter is also available for connecting the debug board on the target development board to the host computer via Ethernet, allowing programmers to share target boards. Siroyan supplies a tool chain for application-software development, including a Gnu C compiler for scalar code, an optimizing C compiler for both scalar and VLIW code, an assembler, a debugger, and an OS kernel. Siroyan also works with third-party developers to deliver software and tools.

STARCORE TECHNOLOGY CENTER'S STARCORE SC100

StarCore's SC100 16-bit, fixed-point architecture has an extensible 16-bit instruction word that includes the SC140 DSP core. The scalable SC100 architecture targets communications applications. Low power dissipation per function helps extend battery life and meet power-per-channel budgets. Compact code density requires less memory, thereby reducing system cost. Customers can use a single DSP architecture and reuse key kernels and code for entry-level as well as advanced applications.

▶ The SC100 architecture features compact code density.

helps extend battery life and meet power-per-channel budgets. Compact code density requires less memory, thereby reducing system cost. Customers can use a single DSP architecture and reuse key kernels and code for entry-level as well as advanced applications.

Addressing modes: The SC100 architecture supports register-direct mode, address-register-indirect mode, program-counter-relative modes, and special-address modes.

Special instruction or integral-peripheral functions: The SC100 multipliers support all combinations of signed and unsigned operands and both fractional and integer formats. The SC100 architecture supports an SIMD (single-instruction-multiple-data) version of maximum and minimum additions and subtractions (MAX2, ADD2, SUB2). It can perform eight 16-bit additions or maximum and minimum operations per cycle and includes MAX2VIT, which works with Viterbi shift left to accelerate Viterbi decoding algorithms. A user-defined instruction-set-accelerator module enhances the SC100 basic instruction set.

Support: StarCore creates low-level, baseline development tools, including a C compiler, an assembler; a linker; an instruction-set sim-

ulator; and optimized, hand-coded C-callable DSP-core libraries to assist programmers in application development. StarCore has also partnered with third-party developers, such as Metrowerks, Wind River, Green Hills, Tasking, Lineo, Ose Systems, Trinity Convergence, Signals and Software, and Numerix to provide a choice of tools, OSs, and applications software.

STMICROELECTRONICS ST100 FAMILY

▶ The ST122 can perform 1200 million MACs/sec at 600 MHz.

▶ Interfaces support customizable coprocessors.

The general-purpose, 16-bit, fixed-point ST100 family architecture targets wired- and wireless-communications, automotive, and multimedia applications. The instruction set features DSP and 16- and 32-bit microcontroller instructions. The DSP architecture supports a 4-Gbyte memory space, 40-bit registers and accumulators,

four idle modes for power-consumption reduction, and three zero-overhead nestable loops. It is scalable for high-performance and low power.

Addressing modes: The family supports 13 addressing modes, including circular, which is well-suited for FIR filtering, and bit reverse for FFT. Data-memory accesses handle bytes, half-words (16 bits), and words (32 bits).

Special instructions or integral-peripheral functions: The instruction set supports predication for most of its instructions, packed arithmetic, and a special instruction for Viterbi. The ST122 core supports 16×32-bit MAC operations for audio applications and multimedia-specific instructions. It can interface with as many as four tightly coupled coprocessors to improve system performance.

Support: STMicroelectronics and third-party partners, such as Green Hills and OSE Systems, provide a suite of evaluation boards and tools for hardware and software development.

TENSILICA'S VECTRA DSP ENGINE

The Vectra DSP engine, a fixed-point coprocessor for the Xtensa, 32-bit RISC synthesizable processor architecture, targets high-volume embedded-processor and DSP applications. Designers use the Xtensa Processor Generator to configure and extend a family of core processors with custom functions while doing software development and testing. The DSP configurations and options available range from simple 16-bit MAC operations to five variants of Xtensa's Vectra DSP engine that include an SIMD (single-instruction-multiple-data) architecture; a vector register file for holding data; coefficient, and intermediate results; and support for single- and double-width operand sizes for greater computational accuracy. The optional DSP functional blocks are tightly coupled into the core pipeline.

▶ The Xtensa TIE (Tensilica Instruction Extension) compiler supports creation of new designer-defined instructions.

▶ The software-development tools are automatically re-created with each new processor configuration.

Designers use the Xtensa Processor Generator to configure and extend a family of core processors with custom functions while doing software development and testing. The DSP configurations and options available range from simple 16-bit MAC operations to five variants of Xtensa's Vectra DSP engine that include an SIMD (single-instruction-multiple-data) architecture; a vector register file for holding data; coefficient, and intermediate results; and support for single- and double-width operand sizes for greater computational accuracy. The optional DSP functional blocks are tightly coupled into the core pipeline.

Addressing modes: The Vectra DSP engine's four addressing modes include immediate and indexed with or without updates to the base register.

Special instructions or integral-peripheral functions: Instruction encoding of 16 and 24 bits reduces data moves, making better use of register files and its allocations. Compound instructions include special shifts, compare/branch, and zero-overhead loop instructions.

Support: The Gnu-based GCC or Xtensa XCC software tool suites automatically tailor themselves to support access to the resources in each new processor configuration. The development environment includes an instruction-set simulator, a bus-functional model, an RTOS OS kit, DSP libraries for the five Vectra configurations, EDA tool scripts, and the Xtensa multiprocessor-system-modeling API. Designers can use the Tensilica instruction-extension-language compiler to create algorithm-specific DSP functions.

TEXAS INSTRUMENTS' TMS320C2000

The TMS320C2000 family of 19 code-compatible DSP controllers offer a combination of on-chip peripherals, such as flash memory, fast ADCs, and CAN modules targeting embedded-control applications, such as optical-networking, tunable-laser, automotive, power-supply, and motor-control applications. The TMS320F2810 and TMS320F2812 DSPs are 32-bit control DSPs with onboard flash memory and performance to 150 MIPS. The C28x core offers 300 MIPS of computational bandwidth with a signal-processing core optimized for control. It is fully code compatible with current devices in the C2000 family.

▷ Devices combine performance and peripheral integration for the embedded-control industry.

▷ These code-compatible DSPs target embedded-control applications.

Addressing modes: The C2000 DSP platform supports indirect and direct addressing.

Special instructions or integral-peripheral functions: The C2000 DSP platform integrates flash memory, an ADC, an event

manager optimized for pulse-width-modulation generation, CAN modules, and serial interfaces.

TEXAS INSTRUMENTS' TMS320C5000

The TMS320C5000 DSP platform uses a modified Harvard architecture and includes the TMS320C54x and TMS320C55x DSP generations. The C55x DSPs are source-code-compatible with the C54x DSPs. The C54x focuses on low power consumption, but the C55x takes power efficiency to a new level: A 300-MHz C55x delivers a maximum fivefold improvement in performance over a

▷ The C55x is one of the industry's most power-efficient programmable DSPs.

▷ Devices consume as little as 0.9V and 0.05 mW/MIPS with a maximum performance of 800 MIPS.

120-MHz C54x and dissipates as little as one-sixth its core power. The C55x has 12 independent buses, and the C54x has eight. Both architectures include one program bus and an associated program-address bus. The C55x bus is 32 bits wide, and the C54x bus is 16 bits wide. The C55x has three data-read buses and two data-write buses; the C54x has two data-read buses and one data-write bus. Each data bus also

has its own address bus. The corresponding address buses are 24 bits wide on the C55x and 16 bits wide on the C54x. The C5000 DSP platform has 17 code-compatible DSPs sampling or shipping in high volume.

Addressing modes: The C54x supports single-data-memory-operand addressing that also supports 32-bit operands. It also supports dual-data-memory-operand addressing that parallel instructions use. It provides immediate, memory-mapped, circular, and bit-reversed addressing. In addition to the C54x modes, the C55x supports absolute addressing, register-indirect-addressing, direct-addressing, and displacement mode. The C55x includes dedicated registers to support circular addressing for instructions that use indirect addressing. Programs can simultaneously use as many as five independent circular-buffer locations with as many as three

independent buffer lengths. These circular buffers have no address-alignment constraints. The C54x supports two circular buffers of arbitrary lengths and locations.

Special instructions or integral-peripheral functions: The C54x performs dedicated-function instructions, such as FIR filters, single and block repeat, eight parallel instructions, multiply, accumulate, and subtract (10 multiply instructions), and eight dual-operand memory moves. The C55x also has special instructions that take advantage of the additional functional units and increase parallelism capabilities. User-defined parallelism allows you to combine instructions to perform two operations. You can also combine a built-in parallel instruction with a user-defined parallel instruction.

TEXAS INSTRUMENTS' TMS320C6000

Texas Instruments' TMS320C6000 DSP platform, a general-purpose, VLIW (very-long-instruction-word) DSP architecture, targets advanced imaging, third-generation wireless and broadband communications-infrastructure applications. This architecture includes the floating-point TMS320C67x DSP generation and the fixed-point TMS320C62x and TMS320C64x DSP generations. The C62x DSP has eight independent, multipurpose functional units and can perform two 16×16-bit MAC operations per cycle. The C67x DSP is a superset of the C62x DSP instruction set that adds floating-point capabilities to six of the C62x DSP's eight functional units. The C64x DSP is object-code-compatible with the C62x DSPs but has significant architectural enhancements, such as four 16×16-bit MAC operations per cycle and operating frequencies of 400, 500, and 600 MHz. The C6000 DSP platform performs MAC operations by using separate multiply and add instructions. Thirteen code-compatible C6000 DSP products are available for sampling or are shipping in volume.

Addressing modes: The C6000 DSP platform performs linear and circular addressing. However, unlike most other DSPs, which have dedicated address-generation units, C6000 DSPs calculate addresses using one or more of its functional units.

Special instructions or integral-peripheral functions: All C6000 DSP processors can conditionally execute all instructions, a method of reducing branching and thereby optimizing performance. On the C64x DSP, the MPYU4 instruction performs four 8×8-bit unsigned multiplies. The ADD4 instruction performs four 8-bit additions. Six of the C64x functional units can perform dual 16-bit addition/subtraction. Two of the functional units perform dual 16-bit compare, shift, minimum/maximum, and absolute-value operations. The M units also support dual 16-bit and quad 8-bit averaging operations as well as bit-expansion and bit-interleaving and -deinterleaving operations. Four of the six remaining functional units support quad 8-bit addition/subtraction operations. Two functional units support quad 8-bit compare and minimum/maximum instructions. Some instructions operate directly on packed 8- and 16-bit data.

TEXAS INSTRUMENTS' TMS320DA250

TMS320DA250, a member of Texas Instruments' C55x generation of fixed-point DSPs, targets portable Internet-audio players, car stereos, home-audio jukeboxes, and other audio applications. The DA250 supports many digital-audio formats and digital-rights-management technologies. The general-purpose-I/O functions provide sufficient pins for status, interrupts, bit I/O for LCDs, key-



boards, and media interfaces for a “microless” design. The parallel interface operates either as a slave to a microcontroller or as a media interface. The media interface includes an ATA flash card or a memory buffer for spinning media.

▶ This device includes built-in secure-digital memory-stick and multi-digital-rights-management support.

▶ Software-development support includes third-party algorithms and compressed-audio algorithms.

Addressing modes: Addressing modes include synchronous SRAM interfaces, SDRAM interfaces, or both, with general-purpose-I/O capabilities or enhanced 16-bit EHPI16 with general-purpose-I/O capabilities. The device also includes an enhanced 16-bit host-port interface (EHPI16) mixed with address bus.

Special instructions or integral-peripheral functions: Integrated peripherals include a real-time clock; a low- and full-speed USB 2.0 interface; memory-stick and MMC/SD

(multimedia-card/secure-digital) interfaces; an I²C multimaster and slave interface; two 16-bit timers and one watchdog timer; and a 10-bit ADC for battery monitoring, buttons, and control signals.

TEXAS INSTRUMENTS' TMS320DRE200

The ETSI 300 401-compliant DRE200 baseband performs channel and source decoding on one chip. The digital baseband can decode all Eureka modes and perform user-interface functions. The DRE200 baseband is compatible with standard audio-DAC interfaces and can interface to an external microcontroller, DRAM, and SRAM. Devices achieve disturbance-free operation during multiplex subchannel reconfiguration or ensemble switching, and they can feed data to external TPEG (Transport Protocol Expert Group)

▶ The DRE200 is a turnkey reference design with comprehensive support.

▶ You can update and upgrade products via software.

or MOT (multimedia-object-transfer) decoders and external memory.

Addressing modes: The DRE200 supports immediate, absolute, accumulator, indirect, direct, stack, and memory-mapped-register addressing modes.

Special instructions or integral-peripheral functions: None.

TEXAS INSTRUMENTS' TMS320DSCX FAMILY

The TMS320DSC21, TMS320DSC24, and TMS320DSC25 DSPs digital-imaging systems on a single chip combine a TMS320C5000 DSP and an ARM7TDMI RISC processor targeting media-processing and system-control functions. The chips integrate a video encoder with an on-screen display, an SDRAM controller with a

▶ The cores are configurable per system requirements.

▶ The development environment supports system emulation before silicon tape-out.

bandwidth-transfer rate of 320 Mbytes/sec, and a preview engine that performs 30-frame/sec NTSC and PAL previewing (DSC21/DSC25). The DSCx family of products can achieve real-time processing of a full-resolution 2 million-pixel image with a 1-sec shot-to-shot delay. DSCx DSPs can support the capture of high-resolution still photos, and it can record video clips with audio and music from the Internet. These

systems support digital-audio and -video formats, including real-time MPEG-1, MPEG-4, JPEG, M-JPEG, H.263 and MP3, as well as data-communication standards, such as IrDA (DSC21), USB, and RS-232.

Addressing modes: Addressing modes include SDRAM, SRAM, flash-media, and removable-media interfaces. The SDRAM transfer rate is 80 Mbytes/sec, with both 332 (DSC21/24/25) and 316 (DSC24) interface capabilities. The DSC24 enables 2-D-to-2-D data transfer from SDRAM to an on-chip image buffer, as well as direct SDRAM access via an SDRAM controller. The ARM can access the DSP via the host-port interface, and its bus controller has on- or off-chip access to general-purpose I/O, flash, Compact flash, and Smart Media applications.

Special instructions or integral-peripheral functions: In addition to the TMS320C54x DSP-generation instruction set, the DSCx DSP subsystem incorporates imaging enhancements to provide fast-block-based processing for imaging or video-encoding and -decoding functions.

Support: The eXpressDSP Real-Time Software Technology encompasses development for all of these devices and includes the Code Composer Studio integrated development environment; DSP/BIOS, a scalable real-time kernel; the TMS320 DSP Algorithm

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Standard, a standard set of coding conventions and application-programming interfaces; and a third-party network. Also available are evaluation modules, technical training classes, and customer-application support.

3DSP'S SP-3, SP-5, AND SP-20/UNIPHY

The soft-IP-core, fixed-point DSP family, bus controller, peripherals, and microprocessor interfaces from 3DSP use a scalable SuperSIMD (single-instruction-multiple-data) architecture. The core supports multiprocessor systems, program cache or direct-mapped program memory, 32 prioritized interrupts, 32 general-purpose I/O pins, and a JTAG-only debugging interface. The SP3 is a programmable, five-stage pipelined DSP that targets MP3-player, home-audio (AAC, AC3), wireless-GSM-phone, GPS, and CPE (customer-premise-equipment) voice-over-packet processing applications. The SP-5 is a programmable, superscalar, dual-issue, five-stage, pipelined DSP that targets 3G wireless, voice-over-packet gateway, xDSL, MPEG4, and wireless-LAN applications. SP-5flex is a fully synthesizable and configurable DSP core, based on the SP-5 architecture, that supports balancing power, cost, and performance. It targets voice-over-packet, digital-wireless, audio, video, imaging, and broadband-modem applications. The SP-5V is a programmable, superscalar, dual-issue, five-stage, pipelined DSP that targets voice-over-packet applications. Development support includes a voice-over-packet software suite, application demo, and reference design.

▷ Devices enable multifunction digital-imaging devices on one chip.

▷ Code compatibility enables single platform, multiple-product strategy.

player, home-audio (AAC, AC3), wireless-GSM-phone, GPS, and CPE (customer-premise-equipment) voice-over-packet processing applications. The SP-5 is a programmable, superscalar, dual-issue, five-stage, pipelined DSP that targets 3G wireless, voice-over-packet gateway, xDSL, MPEG4, and wireless-LAN applications. SP-5flex is a fully synthesizable and configurable DSP core, based on the SP-5 architecture, that supports balancing power, cost, and performance. It targets voice-over-packet, digital-wireless, audio, video, imaging, and broadband-modem applications.

The programmable, dual-mode, nine-stage, pipelined SP-20/UniPHY DSP IP core that includes custom instructions targeting physical-layer signal processing for 802.11a/b/g, HiLAN2, and xDSL. UniPHY combines accelerated versions of 3DSP's SuperSIMD architecture and SP-x instruction set with an expansion-instruction mode. UniPHY is capable of execution speeds of 400 MHz to 1 GHz because it supports a multiple-standard PHY implementation on the same processor. The "soft-datapath" technology and programmability enables a "softPHY" implementation that facilitates modification for changing physical-layer standards.

Addressing modes: The DSP cores provide circular-buffer, 2-D-matrix, bit-reverse, page, register-indirect, and stack-pointer addressing.

Special instructions or integral-peripheral functions: Each instruction can handle as many as 24 RISC-equivalent instructions. Each arithmetic instruction can process one 32-bit, one 24-bit, two 16-bit, or four 8-bit data. Push and pop instructions to allow efficient context switching. The SP-5V includes LMS24 and LMS16 instructions for echo-canceller algorithms.

Support: The software- and hardware-development environment includes complementary software and hardware IP and supports overall system emulation before to silicon tape-out.

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