



The Model 6802 6U VME board from Pentek offers 32 channels of 24-bit delta-sigma analog-to-digital conversion and a front-panel-data-port output interface for high-speed data transfers.

**IN A TIME WHEN NEW TECHNOLOGIES BECOME OBSOLETE IN MERE MONTHS, THE VMEBUS HAS SURVIVED FOR MORE THAN 20 YEARS, OFFERING TIMELY PERFORMANCE UPDATES AND PROTECTING CUSTOMER INVESTMENTS.**

# VMEbus: a study in *evolution* and SURVIVAL

**T**HE VMEBUS (VersaModule Eurocard bus), which debuted in October 1981, has outlived similar computer architectures and continues to thrive through well-timed modernization of the specification and a steadfast determination to maintain compatibility with legacy hardware. Although the hardware is expensive

and based on 20-year-old technology, VME has remained popular with many military, medical-, transportation-, and industrial-control-system developers because of its longevity, ruggedness, and open standards, and the large number of manufacturers offering off-the-shelf products.

Although the recent economic slowdown has had a negative effect on most other embedded-computer technologies, the VME market has managed to remain steady and even show growth in the military segment. Many VME manufacturers considered switching to the higher volume albeit lower priced CompactPCI hardware after observing the enormous growth and rosy projections for the telecommunications-system market before 2001. However, the communications slowdown and the military response to the attacks of September 11 convinced most manufacturers that VME will remain strong for the foreseeable future.

During the past eight years, VME has also been a major beneficiary of the military's COTS (commercial-off-the-shelf) initiative. In 1994, Secretary of Defense William Perry changed government procurement policies and mandated the use of commercial products and practices when possible instead of the traditional design-from-scratch approach. With the large number of boards and systems already in use, developers flocked to VME for new embedded designs.

Originally, manufacturers Motorola, Mostek, and Signetics created the VMEbus by combining the VersaBus electrical standard, which

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Motorola defined for its 68000 micro-processor, with the Eurocard mechanical form factor. Although the VersaBus has long since disappeared, VME took off because it was processor-independent, based on a reliable mechanical form factor, and released as a nonproprietary standard. Any vendor can manufacture VMEbus products and systems without paying royalties or license fees. The manufacturers selected the Eurocard format because it was popular in Europe, and the hardware was readily available. The Eurocard pin-and-socket connector scheme was also more resistant to mechanical wear and vibration than the common pc-board edge connectors.

The VMEbus specification has been available from several standards bodies during the past 20 years. A revised version of basic specifications is now called IEEE 1014; a later update is referred to as ANSI/VITA 1. Both the world-level IEC (International Electrotechnical Commission) and ISO (International Organization for Standardization) have accepted and published the specifications. You can order a copy of the VMEbus specifications (ISO/IEC15776, IEC-60821) on CD-ROM from the IEC at [www.iec.ch](http://www.iec.ch) for approximately \$150. For up-to-date information on VME and its extensions or to purchase a copy of the specification, go to the VITA (VMEbus International Trade Association) Web site ([www.vita.com](http://www.vita.com)).

### IN THE BEGINNING

The basic VMEbus specification, now known as IEEE-1014-1987, offers designers a nonmultiplexed bus with a 16- to 32-bit address range and an 8- to 32-bit data-

### AT A GLANCE

- ▶ Like all shared-bus computer systems, VME has struggled to keep bandwidth in step with constantly increasing data rates.
- ▶ VME remains strong by participating in long-life-cycle markets, retaining backward compatibility, and constantly refining the standard.
- ▶ New bridge chips and bus transceivers allow designers to reliably extend VME parallel data rates to 320 Mbytes/sec.
- ▶ Although it is a 20-year-old technology, VME will compete for future embedded designs with new serial-switched-fabric technology.

path width. Bus transfers are asynchronous, relying on a handshaking protocol instead of a system clock, and the data bandwidth is limited to 40 Mbytes/sec. VME is a master/slave architecture in which a single master processor gains control of the bus, transfers data to one or more slaves, and then relinquishes control of the bus. A VME backplane can contain as many as 21 card slots with multiple master computer boards. Boards are available in 3U (160×100-mm), 6U (160×233-mm), and 9U (367×400-mm) sizes; 6U is the most popular. To power individual boards, 5V and ±12V are available on the backplane. Although the VMEbus standard has progressed considerably since the original specification, these early boards are still compatible with the latest technology.



The VSO (VITA Standards Organization) in 1995 approved a revision to the VMEbus specification, VME64, to give designers a mechanical and electrical superset of the original standard. This revision expanded the data-width and addressing range to 64 bits for 6U boards and doubled the bandwidth to 80 Mbytes/sec. The revision also incorporated bus-protocol changes to enable cycle retry and add automatic plug-and-play features. The committee also approved a lower noise connector system, but guarantees, however, that boards that meet the original IEEE-1014-1987 specification will work without modification.

To relieve congestion on the bus and expand I/O pins, the VSO (VITA Standards Organization) in 1998 adopted another superset, the VME64 Extensions (VME64x). VME64x adds a new 160-pin connector family to replace the 96-pin backplane connectors. It also adds a 95-pin P0/J0 connector between the existing connectors and beefs up the backplane power with more 5V-dc supply pins and new 3.3V pins. The bus bandwidth also

increased again, with two edge bus cycles that increase data rates to as much as 160 Mbytes/sec. VME64x also added more user-defined I/O pins, rear transition modules, ejector handles, and preliminary hot-swap capability. The new backplane connector for VME64x is interesting because it is both backward- and forward-compatible. The new 160-pin connector has five rows of pins in the same physical space that the three-row VME64 connector occupies. Although 96-pin con-

## VME: THE NEXT GENERATION

Faced with the reality of bandwidth-starved applications, a group of manufacturers has proposed modifying the VMEbus standard to include provisions for switched-fabric architecture. The proposal, called VXS (VMEbus Switched Serial Standard), adds a switched serial interconnect to VME while retaining the parallel bus. To date, there is no dominant switched fabric, so VXS will

accommodate multiple serial technologies, although not simultaneously. The VITA (VMEbus International Trade Association) Web site, [www.vita.com](http://www.vita.com), currently lists more than 60 competing switched-fabric technologies, including InfiniBand, RapidIO, 10 Gigabit Ethernet, and 3GIO.

The VXS proposal adds a new P0 connector between the P1 and P2 connectors to route the

serial signals to a central fabric-switch card. VXS will require a new backplane with provisions for one or more switch cards to coordinate serial datapaths. Although backward compatibility is a desirable feature, VXS will not work with older boards that include a P0 connector. An interesting VXS option is to send both control and data signals over the serial fabric, thus eliminating the need for all P1 and

P2 VMEbus signals except power. Can we still call this configuration VME?

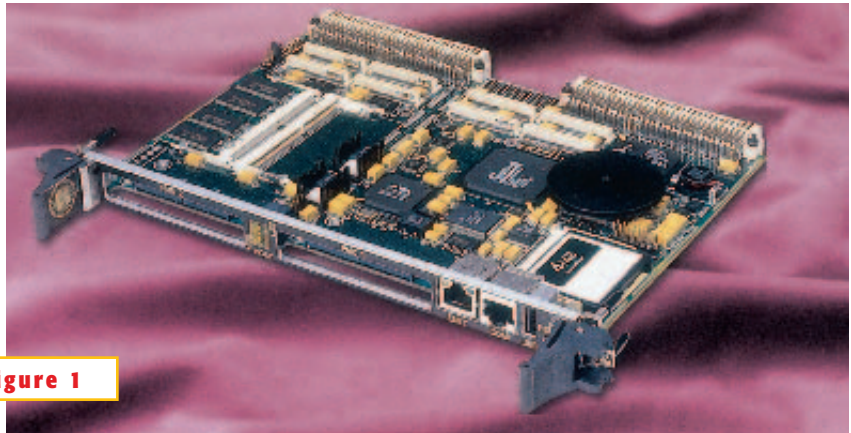
A VITA working group is also studying a new VME mechanical arrangement tailored to the next generation of high-speed, serial-based systems. This system will forgo legacy compatibility to optimize performance. Initial proposals are for 4U or 8U, fully enclosed modules spaced 1.2 in. apart on the backplane.

nectors will plug into a backplane using 160-pin connectors, boards with 96-pin connectors obviously cannot use the added features of the VME64x specification.

Several techniques have been proposed to extend the bus bandwidth to 320 Mbytes/sec and greater, but each has failed to gain popular support. For example, in 1999, Arizona Digital and General Micro Systems demonstrated a star-configuration backplane in which signals driven from Slot 1 transfer directly to Slot 11 and then radiate out to all other slots. To support this approach, VITA tentatively approved 2eSST, a source-synchronized transfer protocol that eliminates one of the remaining data-strobe edges and increases the theoretical data rate to 320 Mbytes/sec. The drawback of the Arizona Digital approach was that users had to replace existing backplane hardware. General Micro Systems has recently introduced the Atlantis V191 Mark II, a PowerPC single-board computer using the 2eSST transfer protocol (**Figure 1**).

**KICK IT UP A NOTCH**

Motorola leads the latest effort to increase bus bandwidth with a PCI-X-to-2eSST-VMEbus bridge chip code-named Tempe (**Figure 2**). In addition to the 320-Mbyte/sec 2eSST-protocol, the chip also supports most previous VMEbus protocols, enabling existing cards and new Tempe-enabled cards to work together in a system. Communications between legacy cards take place at VMEbus speeds, and



**Figure 1**

**General Micro Systems' V191 PowerPC CPU board incorporates 2eSST signaling and provides VMEbus data transfers as fast as 533 Mbytes/sec.**

Tempe-based cards transfer data at 2eSST rates. On the host side, the Tempe chip includes a 133-MHz PCI-X bus interface, providing maximum data-transfer rates of 1 Gbyte/sec, a twofold improvement over the standard 64-bit/66-MHz PCI interface. The PCI-X interface also provides block-data transfers, split transactions, and the elimination of wait states to further enhance host-side performance. A significant advantage of Motorola's 2eSST approach is that existing cards and backplanes require no modification or replacement. Motorola plans to make the Tempe chip available this year to any VME manufacturer.

Boards with the Tempe chip will require new transceivers to achieve the 2eSST data rates. In support, Texas Instruments has announced the SN74VMEH22501 universal bus transceiver to

provide incident wave switching at data-signaling rates of 40 Mbps, an eightfold improvement over the VME64 standard. Incident wave switching occurs when the bus voltage rises above the receiver's threshold, and the transmitter supplies the first signal step. There is no need to wait for signal reflections from the bus terminations. The new device is an 8-bit bus transceiver that operates from a 3.3V power source and interfaces with 5V devices. The SN74VMEH22501 will be available to support the Tempe chip deployment.

As many designers have found, there will always be applications in which maximum data rates exceed the limitations of a shared-bus system. For these high-speed applications, which include medical imaging and other signal-processing problems, designers have turned to aux-

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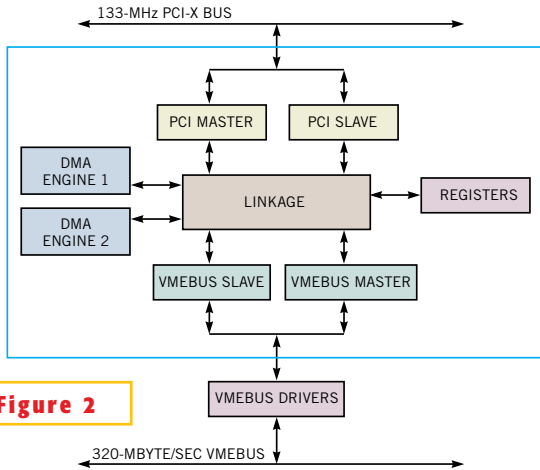
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**Figure 2**

**Tempe, a yet-to-be-released PCI-X-to-VMEbus bridge chip from Motorola, features the 320-Mbyte/sec 2eSST and supports legacy protocols.**

iliary communications techniques to bypass the shared bus and transfer data directly between subsystems. Third-party VME add-ons, such as SkyChannel from Sky Computers and Raceway from Mercury Computers use point-to-point connections and crossbar switches to send high-speed information around the VMEbus (Reference 1). SkyChannel and Raceway are both approved ANSI/VITA standards and multiply their basic bandwidth by allowing several transfers to simultaneously occur.

**TURN TO FABRIC**

SkyChannel and Raceway are precursors to the next generation of computer-system architecture, which promise to

eliminate many of the problems associated with a multidrop bus scheme (Reference 2, see sidebar “VME: the next generation”). With this switched-fabric architecture, data connections between computing subsystems may change dynamically to support multiple simultaneous transfers. Designers use the term “fabric” to represent this architecture, because the multiple datapaths resemble threads in a cloth. A major benefit of a switched fabric

is that each connection is a direct point-to-point datapath. This configuration yields better electrical characteristics, allowing higher frequencies and bandwidth than shared-bus architectures. Most of the switched-fabric specifications call for LVDS (low-voltage differential signaling) for maximum bandwidth between nodes. A typical switching fabric may use multiple stages of switches to route transactions between a source and a target. A sophisticated switched-fabric system can also increase system availability by routing around defective paths or nodes.

VMEbus users need not wait for a specification update to use switched-fabric interconnections for high-speed applications. Many VME computer boards



**Figure 3**

**The StarLink PMC from DY4 Systems gives VMEbus users a 400-Mbyte/sec switch-fabric data interconnect without modifying the backplane.**

already have PMC (PCI Mezzanine Card) slots for direct I/O expansion. Switch-fabric cards, such as the new StarLink PMC module from DY4 Systems, allow users to easily add datapaths with a sustained bandwidth of 400 Mbytes/sec (**Figure 3**). Each PMC incorporates a six-port fabric switch, eliminating the need for a separate external switching card. Prices for the StarLink PMC start at \$2000, and delivery time is 12 weeks.

Obstacles to continually increasing VME data rates, whether higher bus speeds or switched fabric, are the physical characteristics of the connectors on the card edge and the backplane. Connectors are also one of the most difficult hardware elements to change while ensuring compatibility with legacy equipment. At speeds greater than 1 GHz, connectors begin to behave like active components because of their inherent capacitance. Therefore, designers must consider transmission-line effects. Following the lead of Ethernet, backplanes are probably heading for signal frequencies as high as 10 GHz through a single copper pair. Many experts agree that 10 GHz is the upper limit for copper, after which you move to optical-transmission techniques.

VMEbus systems have survived for years in an environment in which you usually measure the lifespan of a new technology in months. VME has proved that it is flexible enough to satisfy a large segment of today's high-technology market for embedded systems, yet you can still plug in and communicate with an I/O board that was built in 1981. You can expect to see the VME standards continue to adapt to changing technology, and, with the newly proposed serial updates, it would not be surprising to see designers specifying VME systems in another 20 years. □



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#### REFERENCES

1. Webb, Warren, "High-speed datapaths bypass bus bottlenecks," *EDN*, March 26, 1998, pg 54.
2. Webb, Warren, "Switched fabric: a stitch in time," *EDN*, April 12, 2001, pg 69.