



Weigh in on your way

**"You ate too much!
Don't do it next time!
It will tell you in a
friendly way, 'Oh,
you're overweight!
What happened?'"**

**—Yefim G Kriger,
who recently won a patent
for a vehicle that can
regularly weigh drivers,
track pounds lost or gained,
and warn them when
they are overeating,
in *The New York Times*,
Dec 29, 2003**

Legacy backplanes get boost to 5 Gbps

By Nicholas Cravotta

NATIONAL SEMICONDUCTOR has further extended the life of legacy backplanes with the SCAN50C400, a quad SERDES (serializer/deserializer) transceiver. The four-channel transceiver

maintains signal integrity at 5 Gbps over FR-4 backplanes designed for 1.25 and 2.5 Gbps and enables the reuse of ASICs for an additional product generation. The CML (current-mode-logic) serial I/O runs at 1.25, 2.5, or 5 Gbps rates for backward compatibility with legacy line cards running at lower speeds.

Employing fixed and adaptive equalizers to improve recovered signal integrity, the transceiver achieves UI (unit-interval) transmitter jitter and 0.65-UI receiver-jitter tolerance; has a IEEE P802.3ae D4.0 standard-compliant

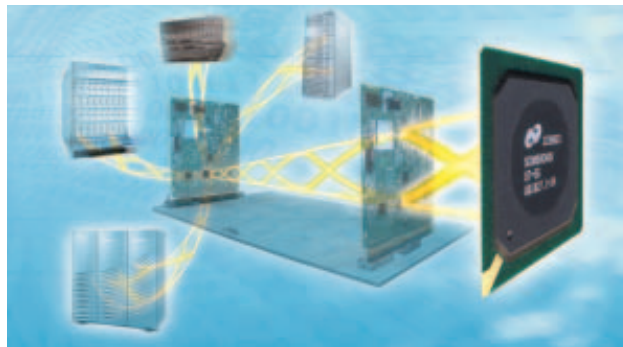
MDIO (management-data-input/output) bus to control programmable features, such as de-emphasis; and offers

built-in self test, loopback modes, and a JTAG port to support at-speed testing.

Samples and evaluation boards are available now. Volume production begins in the first quarter, and prices are less than \$100 (large volumes).

—by Nicholas Cravotta

► **National Semiconductor Corp.**, <http://lvds.national.com>.



The new SCAN50C400 extends legacy FR-4 backplanes to serial data rates of 4 Gbps.

Package extends the capabilities of development tools

IMPULSE ACCELERATED TECHNOLOGIES has released the CoDeveloper C-language-design tool for programmable platforms based on the Altera (www.altera.com) Nios and Xilinx (www.xilinx.com) MicroBlaze embedded processors. The product complements Altera's Quartus II and SOPC Builder products for the Nios processor and Xilinx Platform Studio tool for the MicroBlaze processor. The CoDeveloper hardware/software-design tool allows engineers to use C to develop applications for FPGA devices. CoDeveloper includes compiler tools that provide the necessary C-to-RTL compilation path, as well as automated generation of interfaces for the MicroBlaze or the Nios processors. The tool allows engineers to use Microsoft (www.microsoft.com) Visual Studio, Metrowerks (www.metrowerks.com) CodeWarrior, or other GCC (Gnu Compiler Collection)-based tools

when performing simulations and debugging.

In addition to generating hardware representations in the form of HDL files and of hardware/software interfaces, the CoDeveloper tool exports files, including platform-specific runtime libraries, HDL components, and Tcl scripts to either the Altera Quartus or the Xilinx Platform Studio environment.

CoDeveloper for Nios and CoDeveloper for MicroBlaze sell for \$4995 each for a permanent, single-user license. You can purchase a one-year term license for either product for \$1995. The universal version, which supports both Altera and Xilinx, is available for a one-time license fee of \$8995.—by Gabe Moretti

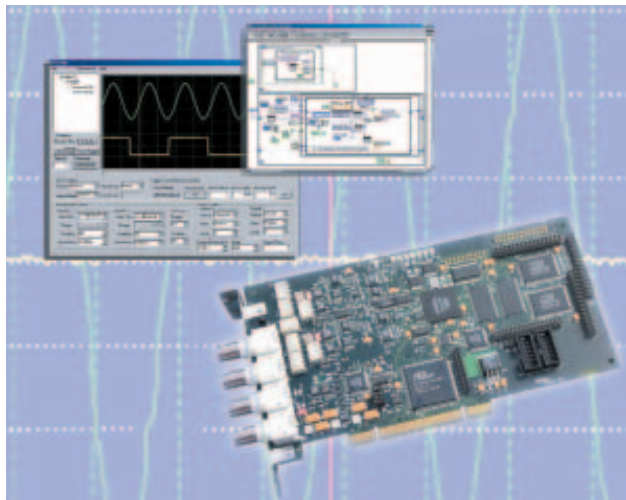
► **Impulse Accelerated Technologies**, 1-866-446-7857, www.impulsec.com.

50M-sample/sec, 8-bit, two-channel PCI ADC-board prices start at \$995

ALAZARTECH'S ATS850 PCI-BASED waveform digitizer provides 8-bit, 50M-sample/sec conversion simultaneously on two channels with flexible triggering and fully programmable front ends.

The company says that a programmable-chip-based design enables the lowest cost in the industry. Each channel provides independently programmable full-scale input ranges of ± 20 mV to ± 20 V, ac/dc coupling, and $50\Omega/1-$

M Ω input impedance. You can program the sampling rate from 10k to 50M samples/sec and capture signals from rapidly occurring triggers by using a multiple-record mode, which allows both pre- and post-triggering.



For less than \$1000, the ATS850 brings two-channel, 50M-sample/sec, 8-bit analog-to-digital conversion to a PCI bus near you.

A 40-bit time stamp records the occurrence of each trigger event relative to all other triggers in a session.

The standard \$995 model includes 256k points of acquisition memory per channel. A \$2995 deep-memory model that can capture 16M points per channel will be available in March. You can transfer acquired data to the host PC's memory using scatter-gather DMA (bus mastering), which provides transfer rates in excess of 40 Mbytes/sec—even with Windows. ATScope software, which allows you to set up the digitizer, acquire signals, and view and store them without drawing diagrams or writing program code, accompanies the unit. OEMs can integrate the board into their systems with the aid of the Windows XP/2000/98SE-compatible ATS-SDK software-development kit. This kit includes sample programs written in C/C++ and Visual Basic. LabView virtual-instrument software is also available.

—by Dan Strassberg

► **AlazarTech**, 1-514-633-0001, www.alazartech.com.

LAPTOP-SIZED EMULATOR VALIDATES IP

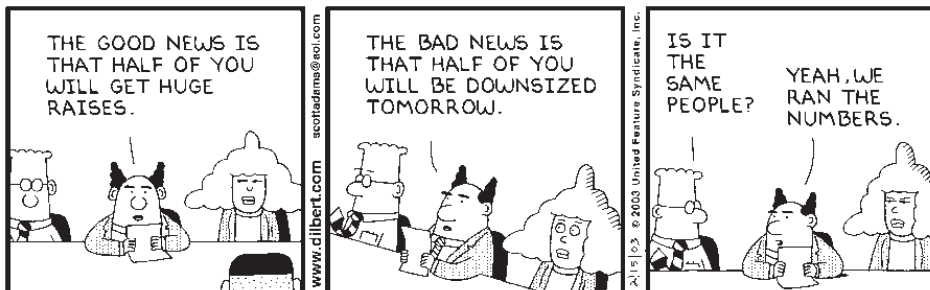
The Aptix Pathfinder IP (intellectual-property)-validation Station provides a prototyping platform for small, embedded designs or for embedded-IP blocks. The device measures 9.5×11.5×2.75 in. and incorporates an Altera (www.altera.com) Stratix EP1S30 or EP1S80 FPGA and provides a capacity of as many as 470,000 ASIC-equivalent logic gates and as many as 7.4 Mbits of embedded memory.

The tool comes with Aptix Expeditor Co-Emulation. This feature enables designers to use their simulation testbenches to provide stimulus and check responses for designs on the emulator. This ability saves development time and allows direct comparison between simulation and emulation results. The emulator includes debugging capabilities through the Expeditor interface. The Pathfinder IP Validation Station sells for \$30,000, including the Aptix Expeditor Co-Emulation interface.

—by Gabe Moretti

► **Aptix**, 1-408-541-4700, www.aptx.com.

DILBERT By Scott Adams



► Sales over the Web represented 4.5% of all retail sales in 2003, but Forrester Research Inc forecasts that they will continue to outpace overall sales and account for 10% of all sales by 2008.

Single-board computer multiplies VMEbus transfer rates

MOTOROLA COMPUTER GROUP has recently announced the MVME6100 single-board computer employing the 2eSST (two-edge source-synchronous-transfer) protocol for significantly faster

VMEbus data-transfer rates. Compared with VME64's typical 40-Mbyte/sec transfer rate, the MVME6100 moves data across the VMEbus at 320 Mbytes/sec. Using Tundra's latest VMEbus-to-PCI-X bridge in 2eSST mode, the MVME6100 also preserves compatibility with more than 20 years' worth of VMEbus legacy products.

Key features of the board include a 1.3-GHz MPC7457 PowerPC processor, a 128-bit AltiVec coprocessor for vector processing, as much as 2 Gbytes of DDR ECC memory, two 64-bit PCI-X-bus interfaces, and dual gigabit-Ethernet interfaces. Initially, VxWorks board-support package and a Linux support



A new single-board computer from Motorola Computer Group boosts data transfers across the VMEbus backplane to 320 Mbytes/sec.

package will support the MVME6100. The MVME6100 will be available in May 2004 at an estimated price of \$3995.—by Warren Webb

► **Motorola Computer Group**, www.motorola.com/computer.

Tool tackles complex FPGAs

DESIGNERS TODAY can consider FPGAs as viable alternatives to many ASICs when deciding how to implement products. Yet, they often have had to depend on tools that were more primitive than those available for ASIC design. At the beginning of the programmable-device industry, the devices were simple, and semiconductor companies usually provided most of the associated EDA tools free as inducements to customers to choose their devices. Today, FPGAs stand on their own merits, and designers choose a device for its physical and logical characteristics, not because it comes with associated inexpensive tools. In the last couple of years, obtaining timing closure for designs targeting the most sophisticated FPGAs has become as difficult as with ASIC devices.

To address this difficulty, Mentor Graphics has introduced Precision Physical Synthesis, which integrates RTL-to-gate synthesis with timing analysis. The tool enhances the traditional synthesis flow with placement modification, retiming, logic replication, and resynthesis. It avails itself of detailed knowledge concerning the FPGA vendor's design rules and uses the data to improve the quality of results. Such technology is the same as the method that ASIC-synthesis tools use. The product offers the PreciseView interactive environment, which complies with the vendor's rules to minimize interconnection delays. Designers can also use PreciseTime's incremental timing analysis to cross-probe between design views to identify bottlenecks and explore ways to overcome them.

The tool operates on Windows NT, 98, 2000, and XP, as well as the Solaris, Linux, and HP-UX platforms. Prices start at \$35,000, and upgrade options are available for users of Precision RTL.—by Gabe Moretti

► **Mentor Graphics**, 1-503-685-8000, www.mentor.com.

Single-chip add-drop multiplexer integrates cross-connect

PARAMA NETWORKS' ADM (add-drop multiplexer)-on-chip offers all the functions required to build applications such as SONET/SDH terminal equipment; metro digital-cross-connect systems; and transport and aggregation multiplexers, including cross-connect systems, line and tributary framers, and overhead-processing systems.

The PNI8040 has eight software-programmable OC-3 to OC-48 or STM-1 to STM-16-rate ports, two OC-192/STM-64 ports, and 40 Gbps of digital-cross-connect capacity. The PNI8160 also has eight software-programmable OC-3-to-OC-48 or STM-1-to-STM-16 ports, two OC-768/STM-256 ports, and 160 Gbps of digital-cross-connect capacity. All 10 port interfaces provide complete read and write access to section and line overhead, path-trace access; pointer processing; alarm detection and insertion; and

section-, line-, and path-performance monitoring.

Next-generation SONET features include virtual rings, multiring termination, and SONET mesh. The nonblocking cross-connect offers full STS-1/STM-0 granular transport-level processing with "hitless grooming" across all ports and time slots, as well as support for hairpinning, broadcast, multicast, and drop and continue.

The company manufactures the device in a 0.13-micron CMOS process and packages it in a 1521-pin flip-chip BGA package. Maximum and typical power-dissipation figures are 8 and 6.4W, respectively. Both versions are currently available for sampling, and prices are \$1250 and \$2500 (1000), respectively.—by Nicholas Cravotta

► **Parama Networks**, 1-408-247-7180, www.paramanetworks.com.

► **Online retail sales reached \$52.3 billion last year from \$33.7 billion in 2001, according to comScore Networks Inc.**

Adaptive-computing platform yields flexible hardware control

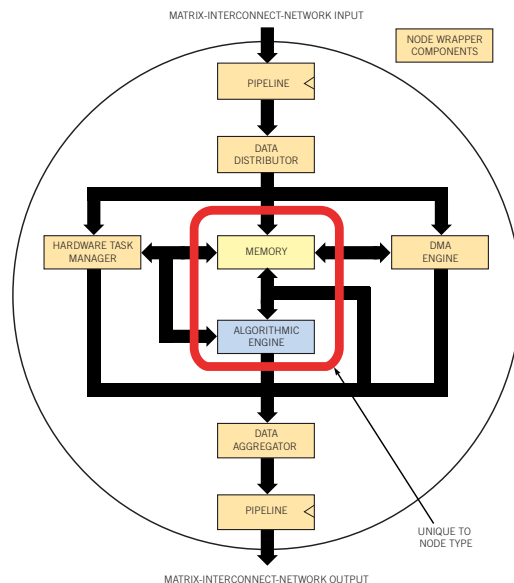
QUICKSILVER HAS INTRODUCED its first product in the adaptive-computing market. This technology allows designers to dynamically modify the hardware architecture of a device, depending on the functions a device requires at a given time. This technology gives designers the flexibility of choosing which applications it will execute at a given time and the ability to do so with the additional speed of dedicated hardware, instead of software.

The QuickSilver Adapt2000 ACM (adaptive-computing-machine) combines both products and business arrangements. Part of the introduction, the Adapt2400 IC, offers four hardware primitives that you can arrange and duplicate in a number of ways to implement the equivalent of reprogrammable, reconfigurable ASIC. The primitives, or nodes, connected to each other by a MIN (matrix-interconnect-network) structure that steers the data among the

computing nodes. The structure of each node is regular; the only difference among them is the size of the memory and the algorithmic engine.

The AXN (adaptive-execution node) offers DSP-like functions and can be useful in matrix manipulations. The DBN (domain bit-manipulation node) allows bit operations, such as decoding or checksum calculations. You can also include on the device PSN (programmable scalar node), a four-stage-pipelined RISC processor node, as well as the XMC (external-memory-controller) node. You can use four to 128 nodes in your architecture.

QuickSilver has also formed a technology pool that aims at creating a family of IP (intellectual-property) products that it shares both internally and with its customers. The details of the license allow for a number of scenarios from freely usable IP to license bearing IP blocks. The \$300,000 cooperative license provides customers with ac-



Adaptive computing allows designers to modify the hardware architecture of a device, depending on the functions it requires at any given time.

cess to the technology pool, which includes the RTL description of the Adapt2400 device; verification suites and documentation; and source code to the compilers, assemblers, and other software tools and the appropriate documentation. Three pay-as-you-go phases allow customers to evaluate and benchmark, explore and analyze the design, and complete the product.

The fourth component of

the ACM platform, the In-Spire software-development kit, provides a simulation platform and a configuration mechanism and allows you to integrate the device in a larger system through a SystemC-interface mechanism. The tool-set perpetual license costs \$50,000 per seat.

—by Gabe Moretti

► **QuickSilver Technology**, 1-408-574-3300, www.quicksilvertech.com.

Handheld DMMs offer non-contact ac-voltage sensor

THE SHOCKING TRUTH is that accidentally coming into contact with ac-line voltage is no fun and, on occasion, can be lethal. Following the philosophy that it should do its utmost to keep all of its customers in the best of health, Meterman, the company that makes the bright-red handheld multimeters, provides noncontact ac-voltage sensing in all of its new XP series instruments.

To prevent accidental contact with live ac circuits, the company not only ships the meters with sturdy, well-insulated probes, but also adds the VolTect feature, which operates even when you have switched off the battery power for all other functions. Simply hold down a button immediately below the LCD and bring the display end of the instrument near a conductor that may be energized. If the conductor is energized, the meter emits a buzzing sound, and an LED next to the VolTect button glows. You can

then treat the conductor with the respect it deserves and use the insulated probes to measure the conductor's ac voltage. List prices for the three XP meters range from \$39.95 to \$79.95.—by Dan Strassberg

► **Wavetek Meterman Test Tools**, 1-877-596-2680, www.metermantesttools.com



To determine whether a conductor is carrying a potentially dangerous ac voltage, you just place the display end of this XP series DMM near the conductor and press the VolTect button. If the instrument detects an electric field, an LED glows, and the meter emits a buzzing sound.