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WITH A DESIGN THAT CONSERVES CURRENT DRAIN, YOU CAN POWER YOUR PERIPHERAL DEVICE DIRECTLY FROM THE HOST COMPUTER'S USB PORT.

Stealing USB-port power

IN ADDITION TO UPGRADING the data-handling capability of a desktop computer's aging serial and parallel ports, the USB also provides a voltage source that you can use to power external peripherals. **Table 1** summarizes the requirements that the USB specification places on equipment (**references 1** and **2**). As the **table** shows, the host equipment provides a 5V supply capable of only 2.25W of power in the worst case. In some cases, this power is not enough for the peripheral, and you must use an alternative power source, such as a wall adapter or an offline power supply. In other cases, this power is much more than necessary, and you can use low-cost, linear regulators to generate the supply voltages for the peripherals. If you elect to use the port voltage, the USB-power limit necessitates the use of high-efficiency power-supply designs and complicates the system trade-offs of cost, efficiency, and size.

The USB specification includes detailed requirements on current limitations through the power interface. For example, when a device connects to the USB port, the current surge to charge a bypass capacitor could create a glitch on the host-equipment supply. The USB specification resolves this problem by limiting the initial power surge in two ways: The peripheral device is allowed only a less-than-10-µF bypass capacitor, and the charge drawn from the bus is limited to 50 µC over a specified time. Once you connect the device to the USB port, the specification imposes further limits on current draw. The host first recognizes any peripheral as a low-power device, which is limited to less than 100 mA of current. The peripheral can then ask the host to recognize it as a high-power device through a process called enumeration. Once enumeration is complete and permission is granted, the peripheral current limitation increases to 500 mA. The USB specification also includes a suspend mode that supports remote wake-up. This mode limits quiescent current to a total of 500 µA for a low-power device and 2.5 mA for a high-power device; it often requires switches to power down portions of the peripheral's electronics.

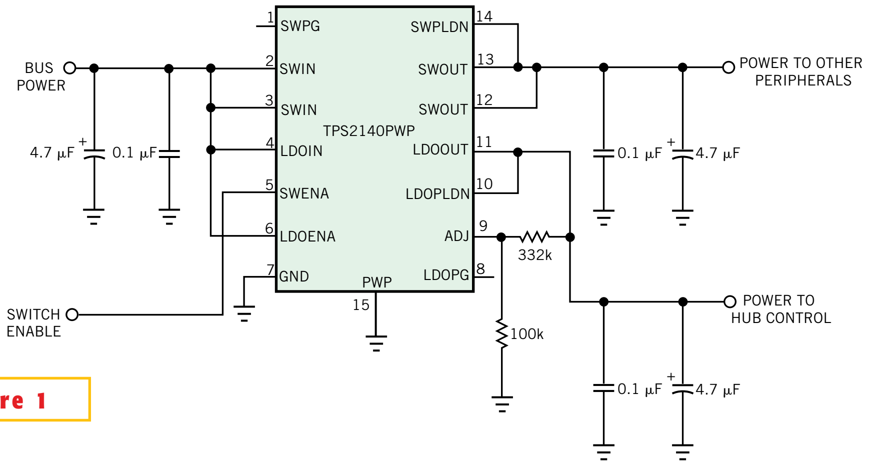


Figure 1

A typical USB IC provides internal-switch power segmentation and limiting.

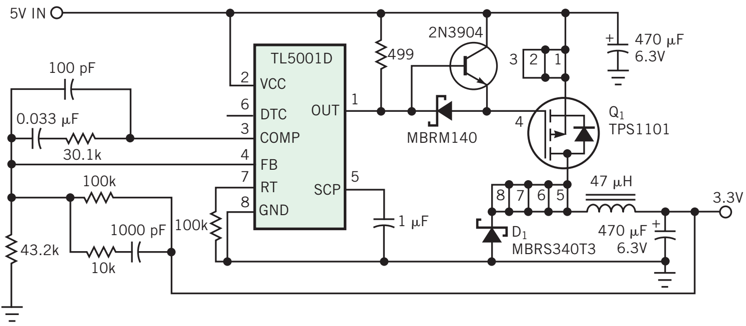
The USB specification has been active for almost a decade; Version 1.0 was released in November 1995. Many products that were designed to meet the original Version 1.0 specification do not fully meet the current-limit requirements. Excessive current may be no problem with a single product connected to a PC; however, multiple products connected in a hub arrangement will activate overcurrent in the hub. Version 2.0 promises to be more rigorous.

INRUSH LIMIT AND POWER SEGMENTATION

You can configure USB products as single peripherals connected directly to a host or a set of peripherals connected through hubs to the host. In the single-peripheral case, the current-limiting requirements rarely become problematic unless you place a large input capacitor across the power-supply voltage. In the hub case, current limiting is required because the nature of the peripherals that you plug into the hub is unknown.

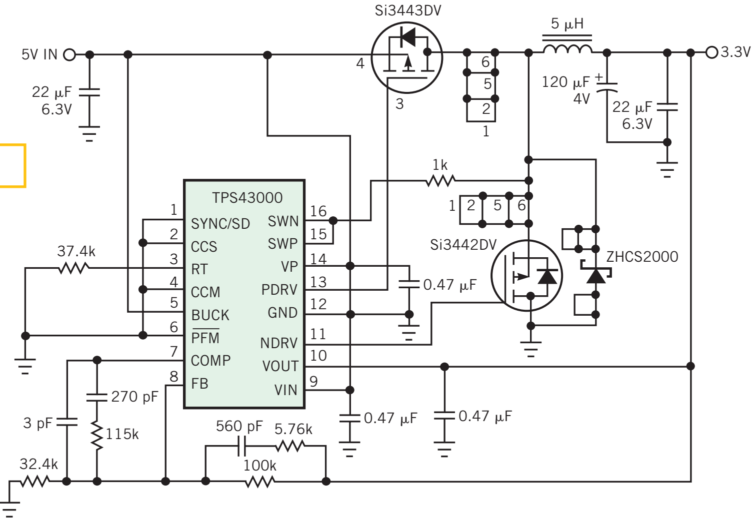
You can implement the current limits using discrete power devices with external control circuits or with switches integrated into the controllers. In higher power applications, the discrete approach usually yields a lower cost option. However, an in-

Figure 2



When power is an issue, a low-cost nonsynchronous buck regulator increases efficiency.

Figure 3



You can improve efficiency over a wide load range with an external-switch synchronous buck regulator.

tegrated approach is attractive in lower power applications. Because USB involves low voltages and currents, a number of manufacturers are developing ICs targeting these markets. **Figure 1** presents a typical circuit. The first output is an adjustable linear regulator that you can configure for a 0.9 to 3.3V output. You use this output to power the hub controller and other electronics. The second output is a switched output that powers the peripherals connected to the hub.

The integrated approach provides a number of desirable features. Devices are much more rugged than those from a discrete approach, because a thermal limit monitors the pass-element temperature and shuts down the device if it detects an overtemperature. The switch provides two-level current limiting to prevent a glitch on the host power bus. Initial power-up current is limited to 100 mA until the output reaches 93% of the input voltage. Once the USB controller is enumerated, the current limit is raised to 500 mA, which is typical of the high-power peripherals.

Table 2 compares the internal- and the external-switch approaches. The pass elements are of higher resistance in the internal-switch approach because the silicon-die area is more costly in the internal switch, because more mask levels are involved in an IC's device structure than in a simple MOSFET. Typically, ICs use more than 20 mask levels; a MOSFET uses eight to 10 levels. An internal-switch approach occupies less than 60% of the area that an external-switch approach occupies. The higher level of integration eliminates at least two semiconductor packages and the resulting poor interconnect efficiency. In addition, the higher level of integration provides higher reliability, because it requires no bond wires and solder joints. The overtemperature protection of the internal switch further enhances reliability. External switches offer no cost-effective method for measuring the MOSFET temperature to protect it from shorted loads. Current foldback and power-cycling techniques can help, but they do not provide the robustness of the thermal shutdown. The last column of **Table 2** presents a cost comparison between the two approaches. The costs are almost the same and bear a closer examination on each requirement. Generally, the costs are so close because the external-switch approach uses multiple semiconductor packages, and the integrated-switch approach uses only one package. Each of the packages has its own overhead of assembly and test, making the overall system-level costs nearly equal.

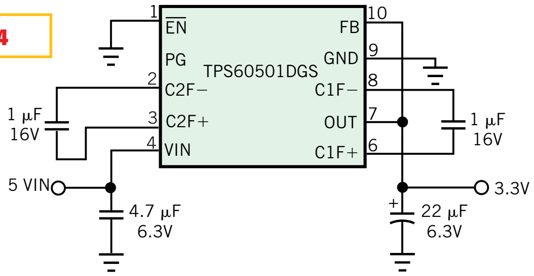
LOW-VOLTAGE DIGITAL ELECTRONICS

You can generate low voltages, such as 3.3V, from the USB in several ways. Assuming 95% efficiency, the maximum current for a 3.3V output is limited to 0.65A due to the 2.25W input-power limitation. You can use linear regulators, switching power supplies, and charge pumps to produce these lower voltages. Switching power supplies may be synchronous or conventional. Synchronous supplies are more efficient but costly; however, you can use them to get as much power from the USB as possible.

The linear-regulator approach is the lowest cost and highest density option for generating lower voltages from the 5V USB bus. When power is not an issue, a linear regulator is the circuit of choice. However, when power becomes an issue, switching regulators can more efficiently power the peripheral. **Figure 2** shows one of the lowest cost buck-switching-regulator options available. In this circuit, the switching of the FET, Q$_1$, is controlled to "buck" the average voltage presented to the output filter, which then smoothes the switching waveform. An external FET provides flexibility in the design, allowing you to use a device with a lower on-resistance than you would use with an integrated FET controller and possibly achieve greater efficiency. The downside to this circuit is that the lack of controller integration requires the use of an external FET and drive circuit, making the circuit relatively large.

The circuit in **Figure 2** dissipates a large percentage of the overall power loss in the freewheeling diode, D$_1$. The circuit in **Figure 3** replaces this diode with an N channel FET, making it a synchronous

Figure 4



A step-down charge pump yields a small circuit area.

buck converter and significantly improving the converter efficiency. Using this circuit, you can realize efficiency improvements over a wide load range. At light loads, pulse skipping can decrease gate-drive losses. The converter senses when the output voltage drops to 2% less than the nominal-voltage setpoint. At that point, the converter switches until the output reaches an upper threshold and then puts itself into sleep mode as the load again discharges the output capacitor to the lower threshold. This circuit provides excellent efficiency but costs more than the circuit in **Figure 2**. Its circuit area is also slightly smaller than that in **Figure 2**, mainly because the controller can operate at maximum frequencies of 1 MHz. This capability allows for a noticeably smaller inductor and smaller I/O capacitors.

Integrating the top FET, bottom FET, drive circuit, and feedback compensation into the controller provides for a small, integrated, and efficient converter option. It is becoming popular, because it is generally simple to design and has a short design-cycle time. Software is available that aids in the design, enabling nonexperts to design power supplies. Controllers such as the TPS5431x and TPS5461x Swift series provide such integration but are more costly because of added performance and features.

Circuit area can often be a critical design parameter. The step-down charge pump in **Figure 4** is one option with small circuit area. It requires only four ceramic capacitors and a charge-pump controller. The controller uses internal FETs that connect two flying capacitors in various series or parallel configurations, dumping their energy to the output. The input voltage and the load automatically set the internal FET configuration. At loads heavier than 150 mA, the controller acts as a low-dropout regulator and stops using the switched capacitors altogether. Maximum output current is limited to 0.25A, which limits this circuit to only low-power applications. Efficiency is 80 to 90% for light loads of 1 to 50 mA but drops off to approximately 65% above that level when operating in low-dropout mode. The cost of the design in **Figure 4** is among the lowest, due to the low cost of the ceramic capacitors.

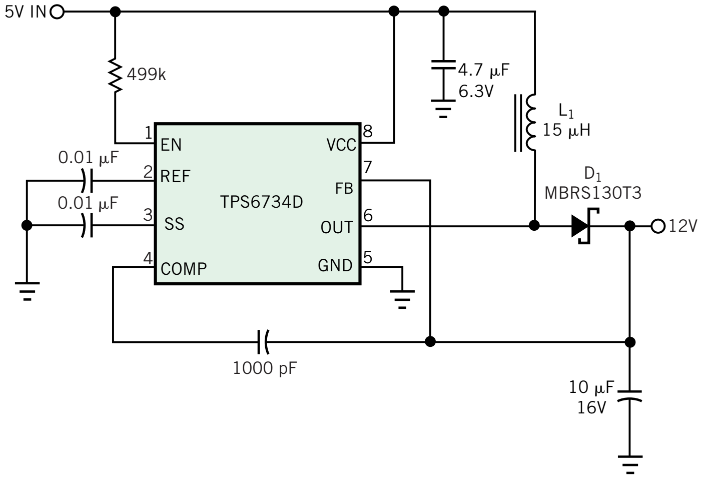
Table 3 summarizes the low-voltage step-down options. It also lists efficiency, cost, and circuit area. So what's the right choice? Your first choice should be a linear regulator when you can afford the losses. Then, look at charge pumps and determine their losses based on conversion ratios. After that, evaluate nonsynchronous regulators. Finally, look at synchronous regulators. In each case, the system cost and size increase, but more power is available for the load. A second level of trade-off in the switching power supplies involves deciding between internal and external FETs. The cost is usually lower with external FETs, but the design time, component count, and size are smaller with internal FETs.

HIGHER VOLTAGE ANALOG

Higher legacy voltages, such as 5 and 12V, are often required to power analog circuits. The loading on these outputs is typically not as heavy as the their digital-voltage counterparts, usually less than 100 mA. The boost regulator in **Figure 5** provides 12V and as much as 120 mA while operating over the 5V USB output-voltage range. In this design, the controller integrates the FET and the feedback-resistor network, minimizing total parts count. A drawback of this approach is that the circuit block provides no current limit. If you short the 12V to ground, nothing in the V_{IN}, L_1, or D_1 path limits current.

An alternative topology, a SEPIC (single-ended primary-inductance converter), can overcome this shortcoming by providing built-in current limiting. Also,

Figure 5

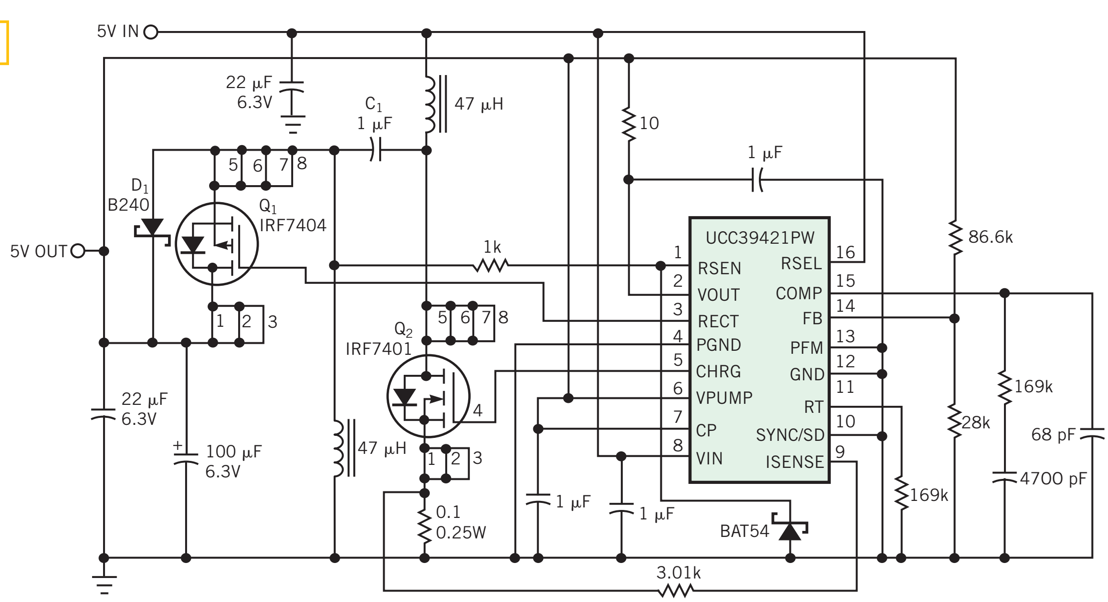


A boost regulator provides 12V at as much as 120 mA from the USB port.

TABLE 1—REQUIREMENTS FOR USB PERIPHERALS

Parameter	Requirement
Voltage	4.4 to 5.25V (low-power device) 4.75 to 5.25V at upstream connector (high-power device)
Maximum quiescent current	500 µA (low-power device)
Minimum-power current	100 mA
Maximum-power current	500 mA
Maximum power draw	2.25W
Maximum input capacitor	10 µF
Maximum inrush	50 µC

Figure 6

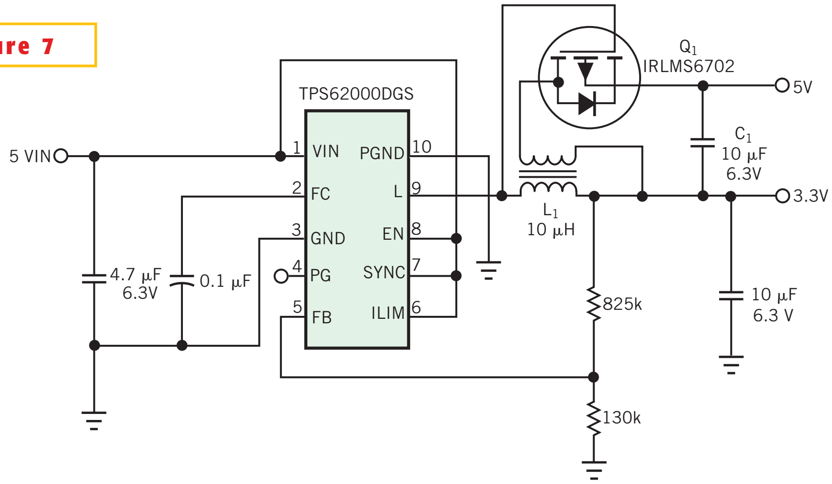


The synchronous SEPIC converter operates over a wide input-voltage range.

the SEPIC conversion ratio extends above and below the input voltage, unlike the boost regulator, whose ratio includes only voltage greater than V_{IN}. Because the USB voltage can range from 4.5 to 5.5V, the SEPIC that **Figure 6** shows makes an excellent choice for a 5V output. This SEPIC uses a synchronous rectifier, Q$_1$, to reduce the losses in the output diode and improve efficiency by several percentage points. D$_1$ conducts only during the on/off transitions of Q$_1$ to prevent the intrinsic diode of Q$_1$ from conducting. Additional benefits include low input ripple currents and inherent current limiting. On the negative side, the SEPIC requires the addition of the dc blocking capacitor, C$_1$. The blocking capacitor and the output capacitors must handle large pulsing currents. They require a high-rms ripple-current rating and have a low equivalent series resistance to minimize the output-ripple voltage. Ceramic capacitors are usually chosen because of their high ripple-current rating and low cost.

Figure 7 shows another option for providing dual output voltages from a single synchronous buck converter. When the bottom-side FET (internal to TPS62000) conducts, FET Q$_1$ turns on, and output capacitor C$_1$ charges with an additional voltage developed across the secondary of L$_1$. The turns ratio between the two windings of L$_1$ determines the level of the auxiliary voltage. The voltage across C$_1$ is stacked on the 3.3V-regulated output, so for a 5V auxiliary output, the circuit needs to develop an additional 1.7V across L$_1$'s secondary. A 2-to-1 turns ratio works well in this application. For low current levels, the voltage drops developed across the internal bottom FET and Q$_1$, which turn on in phase with each other, are small and often cancel each other out. These FET drops may not significantly add to the output-voltage-tolerance error, and good regulation is possible.

Figure 7



A synchronous buck converter with an auxiliary output winding provides dual output voltages.

Table 4 presents a comparison of some

TABLE 2–A COMPARISON OF INTERNAL- AND EXTERNAL-SWITCH APPROACHES

Power-manager implementation	Switch resistance (mΩ)	Circuit area (in.^{2})	Overtemperature protection	Relative cost
Internal switch	100	0.30	Yes	0.8
External switch	50	0.5	No	1.0

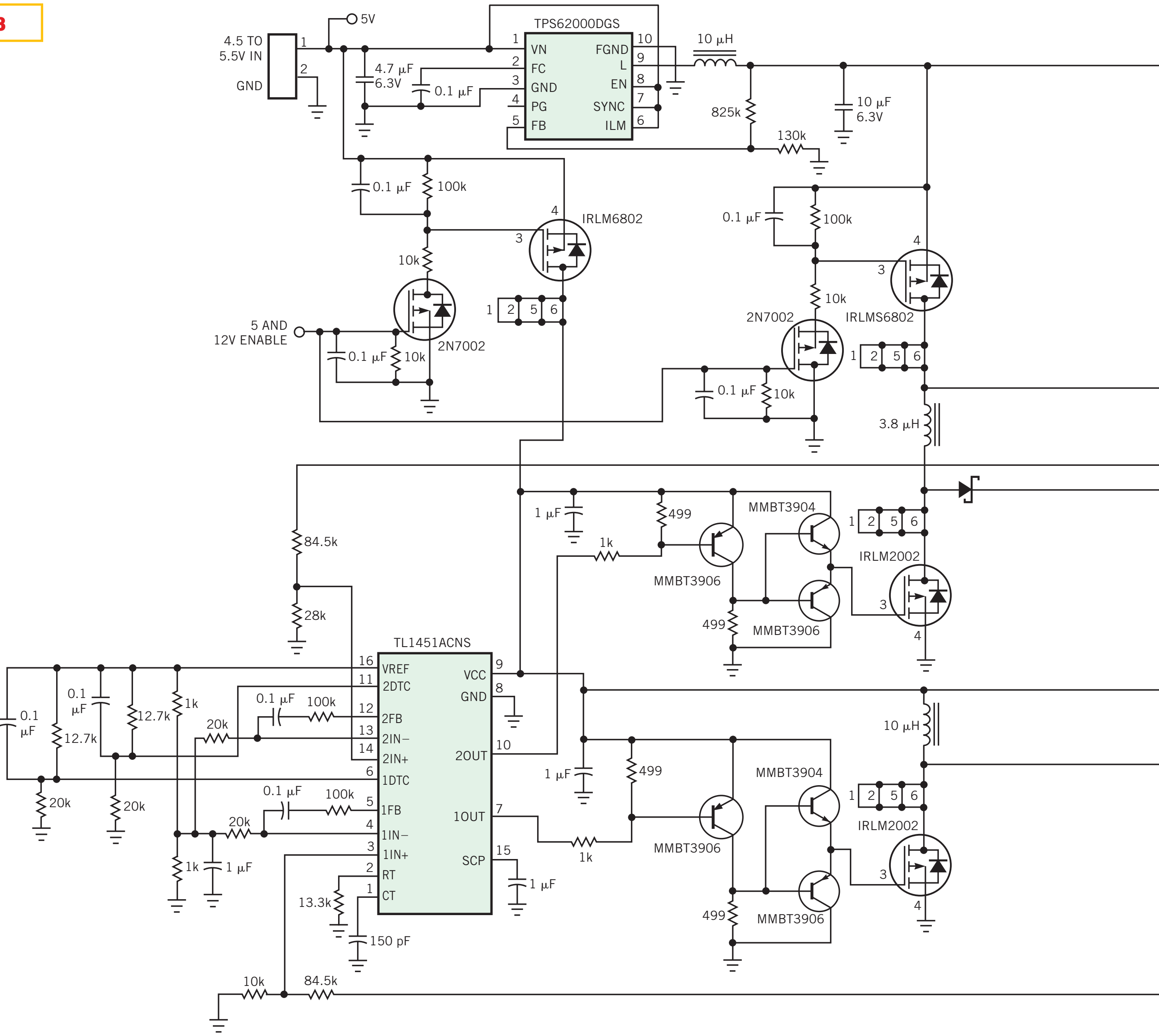
TABLE 3—SUMMARY OF LOW-VOLTAGE STEP-DOWN OPTIONS

Topology	Internal switch	Typical efficiency (%)	Relative cost	Area (in.^{2})
Linear	Yes	66	0.4	0.1
Nonsynchronous buck	No	87	1	1.2
Nonsynchronous buck	Yes	85	1.5	1.1
Synchronous buck	No	96	2	1.0
Synchronous buck	Yes	95	2.5	0.7
Charge pump*	Yes	60 to 90	0.7	0.15

*Current limited to 0.25A; efficiency depends largely on input voltage.

of the options for generating higher voltages for analog loads. Here again, the decision involves trade-offs among cost, performance, and loss. If power is not a problem, the first choice to consider is a charge pump. When loss becomes an issue, a switching regulator may become warranted. The first circuit to consider, particularly if you are using a buck regulator, is the auxiliary winding scheme of **Figure** 7. It has the lowest cost and least degradation of efficiency. Next comes the SEPIC and the boost regulator. The need for short-circuit protection determines which approach is best. You choose a boost regulator for its higher efficiency if current limiting is unnecessary or if the system can accommodate it elsewhere. There are also trade-offs in synchronous

Figure 8

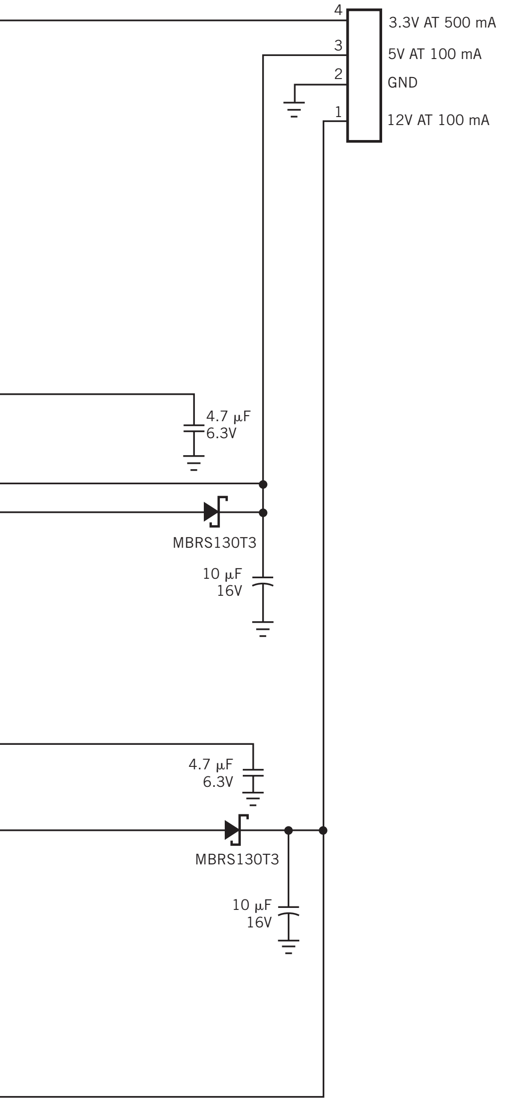


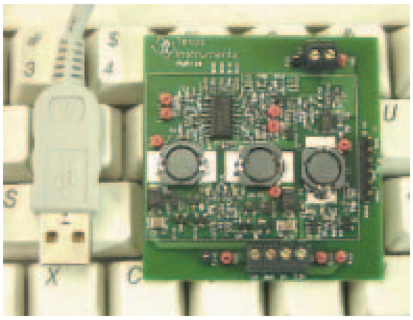
This complete USB power supply has 3.3, 5, and 12V outputs.

TABLE 4—SELECTION CRITERIA FOR HIGHER VOLTAGE REGULATORS

Topology	Internal switch	Current limit	Typical efficiency (%)	Relative cost	Area(in.^{2})
5 to 12V boost	No	No	86	2.8	0.7
5 to 12V boost	Yes	No	85	3.2	0.6
5 to 5V SEPIC*	No	Yes	89	5.6	1.0
5 to 5V SEPIC	Yes	Yes	85	5.5	0.9
3.3 to 5V charge pump**	Yes	Yes	65 to 75	2	0.2
Synchronous buck with auxiliary winding	Yes (synchronous buck) ***No (auxiliary)	Yes	95	1	0.3

***Synchronous operation.**
****TPS60133 charge-pump controller; 0.3A maximum output current.**
*****Cost and area of auxiliary winding only.**





A sample DSL-modem power supply optimized for low cost and efficiency measures only 1.5×3 in.

Figure 9

and nonsynchronous operation, as well as internal and external switches, as in buck regulators.

USB-POWERED DSL-MODEM POWER SUPPLIES

The circuit in **Figure 8** is an example of a complete USB-powered power supply with 3.3, 5, and 12V outputs. The overall efficiency was measured while powering the 3.3V at 0.32A, 5V at 0.05A, and 12V at 0.05A is 89.5%. This efficiency allows the input power to remain below the 2.25W maximum limit. In operation, only the 3.3V output is allowed to power up at turn-on, and the bus controller holds the 5 and 12V-enable pin low. The system draws no more than 100 mA off the 3.3V output during power-up in low-power mode. Enumeration then comes from the bus controller to allow the 5 and 12V to power up. The design uses a boost topology for both the 5V and the 12V output, and the 3.3V output powers the 5V power-stage input. The controller for both boost regulators is the low-cost dual TL1451A. The approach for this design example targets low cost and high efficiency, rather than small area. **Figure 9** shows a photograph of the completed hardware, which measures 1.5×3 in.

The 2.25W of available input power and the peripheral-load requirements drive the design of a power supply for the USB application. The design process should involve a careful analysis of load currents followed by a program to minimize them. Once you determine the loads, the power-supply engineer should develop multiple block diagrams involving the topologies described above to develop the lowest cost and lowest power, USB-compliant approach requiring the least area. The breadth of ICs to support these designs is diverse, and designers can strive for maximum integration, minimum cost, or ease of use.□

REFERENCES

1. USB Specification, Revisions 1.1 and 2.0.
2. USB Implementers Forum Web page, www.usb.org.

AUTHORS' BIOGRAPHIES

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