hands-on project

By David Marsh, Contributing Editor

Motorsport accelerates prototype design

GETTING IDEAS TO MARKET FAST IS FREQUENTLY THE KEY TO A PRODUCT'S SUCCESS. BUT WHEN TIME-SCALES ARE SERIOUSLY SHORT, IT'S VITAL TO CHOOSE FLEXIBLE DESIGN APPROACHES AND RESPONSIVE BUSINESS PARTNERS. HERE, A MOTORSPORT PROJECT THAT INCLUDES THE UNITED KINGDOM'S FIRST APPLICATION OF A BRAND-NEW 32-BIT MICROCONTROLLER COMES TO LIFE.

As industry insiders acknowledge, the need for speed drives every aspect of the motorsport industry—on and off the track. At the highest echelons of the sport, competitive need frequently overrides considerations, such as cost and long-term return on investment, that typify mainstream commercial projects. In particular, cost frequently takes a back seat to the speed at which you can complete a new project. Even so, it comes as something of a surprise when commercial success depends on embedding intelligence and communications to take a development project from design brief to functional prototype within just two months. Without a suitable microcontroller to power the project from the outset, the prospects of success look distant and likely to force decisions that even the most pragmatic automotive engineers dislike. At times like this, normally reclusive hardware designers realise that capable, responsive, and, above all, *willing* business partners are key to success—as the story of "Project Hercules" demonstrates.

Developed for sports-car and endurance-racing events, Project Hercules is an intelligent power-control system that actively manages all of a vehicle's electrical circuits, including mission-critical channels, such as the engine-management system. The microcontroller phase of the project calls for a plug-in board to provide a supervisory control and data-acquisition interface between the underlying power-control hardware and the car's onboard systems. In an industry in which reliability is crucial, each stage of any project receives layers of testing that culminate in customer approval for a system to compete in championship events. Partially for this reason, the initial phase of the power-control system comprises a modular design that can run as a stand-alone system. To provide the best reliability at the least risk, this stand-alone system is as simple as possible and uses as many tried-and-tested elements as is practical. The ability to run as a stand-alone system also suits cars that don't carry central intelligence, providing cost savings to that market sector. Because the commissioning company, motorsport-system designer TJCW (Tony James Component Wiring), also serves many industrial customers, it's important for the project's technology to be as reusable as possible.

Accordingly, the stand-alone prototype of Hercules' power-control system comprises two pc boards. A motherboard accommodates the power devices with their control elements and power supplies. A plug-in I/O signal-conditioning board provides the interface between the car's various logic signals and switch-panel hardware. The motherboard makes extensive use of smart-power FETs from Infineon Technologies and International Rectifier. Together with external control logic, such FETs can reduce $R_{DS(ON)}$ power dissipation to negligible proportions to enable the packing density that vehicles such as Le Mans/GT prototype sports cars and endurance-spec touring cars require. Some smart-power FETs also provide an analogue feedback signal that's proportional to output current (**Reference 1**). Given a suitable microcontroller and firmware, it's possible to design a system that permits teams to run custom power-control strategies. For example, you might choose to temporarily disable the alternator to minimise engine power losses during a qualifying lap.

FLEXIBLE I/O ENABLES MULTIPLE USES

The requirement to run as a stand-alone system or under processor control demands flexible input-signal switching. In stand-alone mode, inputs debounce switch-panel hardware and protect the downstream logic. In processor-control mode, tristate logic disconnects almost all input switches as serial-communication links assume control; few inputs, such as the park-ground signal that controls the wiper's automatic-parking mechanism, remain connected. Further, most cars require circuits such as the engine-management system to be present with the master-switch positive supply, the ignition-on supply, or both, with no dedicated external switching. Regardless of the condition that enables each circuit in the end user's application, design-for-test considerations demand independent hardware- and software-channel control to support automatic-test-and-calibration routines. Finally, because the initial switch architecture may be unable to accommodate all end-user applications without hardware revisions, changes must be inexpensive and easy to make.


Photo courtesy Hitex

As a result, the I/O board is a low-cost module that can change without affecting other boards. Able to withstand continuous ±25V input levels and ±15-kV ESD strikes, Maxim's MAX6818 octal switches protect sensitive logic from environmental conditions and provide a nominal 40-msec debounce time (**Reference 2**). The chips consume a maximum of 20 μA from a 5V supply and include undervoltage-lockout protection to guarantee reliable start-up operation. Better still, the MAX6818 includes input pullup resistors of 63 kΩ/channel. You might wonder whether a 63-kΩ pullup is strong enough to work in a noisy automotive application, but no problems have been evident, even with the unshielded wiring that feeds Hercules' signal inputs. The MAX6818 also includes change-of-input-state and tristate output controls that can simplify microcontroller interfacing. Importantly, the MAX6818 is specified for industrial-temperature-range operation and comes in 20-pin SSOPs that occupy less than 8×8 mm of pc-board space—and all for less than €3 (1000).

The MAX6818s feed several PLDs (programmable-logic devices) that gate input-switch signals with status information, such as whether the ignition is on. The PLDs also provide the tristate interface that allows the processor board to assume executive control. In the initial design, the PLDs were Atmel's ATF16V8CZ devices, which have very low average power consumption, helping to constrain Hercules' full-load internal temperature rise to around 20°C. Costing around €2.50 (100), such "zero-power" PLDs employ input-transition-detection circuits that switch the device from active to standby mode after about 75 nsec of inactivity. In standby mode, the device turns off its internal fuse array to reduce power consumption from around 100 mA to some 25 μA, while pin-keeper circuits maintain stable I/O conditions. This theory sounds fine, but in practice, some PLD outputs failed to track their inputs. Further analysis reveals that a slowly changing gating signal fails to wake the devices out of standby to update the output states; however, even sharpening this signal in a Schmitt trigger fails to provide reliable operation within the Hercules application. Substituting Cypress low-power PLDs (PALCE16V8L) provided an interim fix. But each of these parts consumes around 40 mA of quiescent current, which is similar to the current that the entire motherboard requires!

Today's approach routes a 250-Hz clock signal to each zero-power PLD to guarantee that it updates correctly. But a far better option that's under evaluation may substitute a single device from the Xilinx CoolRunner XPLA3 family, whose members provide 32 to 512 macrocells and 36 to 260 I/O pins. Suggested by PLD expert Arthur Wright, principal of First Time Designs, CoolRunner PLDs are fully CMOS structures that don't rely on input-transition techniques or dedicated power-down pins to reduce quiescent consumption to less than 100 µA. Running from a 3.3V supply, the 5V I/O-tolerant XPLA3-series includes JTAG-port in-system programmability to minimise pc-board rework and redesign. Available now, the midrange XCR3128XL offers 128 macrocells and 108 I/O pins in a 144-pin TQFP for around €11 each from the Xilinx Web site (see **sidebar** "For more information"). If you're prepared for a 60-Mbyte download, you can download the ISE WebPack design tool set for free. Also notice that Xilinx now offers the CoolRunner-II family, which is optimised for 1.8V operation to suit wider portable product applications.

Other I/O-board functions include controlling the car's indicator and wash/wipe systems. In a conventional vehicle, timer relays control these systems, but this approach can't meet TJCW's requirement to remove inelegant peripherals from the wiring loom's structure. In stand-alone mode, an AT90S2313 microcontroller from Atmel's AVR family drives the indicator and wash/wipe logic; in processor-control mode, the I/O pc board's ability to cede control means that teams can experiment with alternative wash/wipe strategies to suit differing climatic conditions. The AT90S2313 is a 20-pin device that has 15 independently programmable I/O lines, of which three serve in-system programming needs. (An external multiplexer can preserve I/O pin count.) On-chip memory comprises 128 bytes of RAM and 2 kbytes of flash, together with 128 bytes of EEPROM that you can use to store calibration constants. Other features include an analogue comparator, 8- and 16-bit timer/counters with programmable clock prescalers, a full-duplex UART, and internal and external interrupt sources. The catalogue distribution price is around €8 (250).

Atmel's decision to support the AVR family from the outset with a free development environment and low-cost tools, such as the ICE200 ICE (in-circuit emulator), proved decisive for another project in 2000. For around €200, you get a real-time ICE that nonintrusively emulates most AVR parts at full speed using a bond-out version of the AVR core. The ICE comes as standard with a variety of pods to suit eight- to 40-pin DIL devices, and an SMD kit is now available for around €120. Third-party AVR software support includes the QuickBasic-like Bascom compiler from MCS Electronics for around €80, and Imagecraft's optimising ANSI-C compiler for around €500; evaluation versions are available at the companies' Web sites. You can download the latest versions of Atmel's AVR Studio suite from the company's Web site or from the AVR Forum at www.avrfreaks.net. Of course, the microcontroller landscape has moved on, and a feasibility study today may favour another vendor. Notably, some Microchip parts now have JTAG debugging capabilities and low-cost ICE support to complement competitive software tools. The recently announced PIC18xxx family includes members such as the PIC18F458, which features a CAN version 2.0B port to supplement the chip's 32 kbytes of flash and typical microcontroller peripherals—all for around €7 (100).

AT A GLANCE

- ▷ Small-volume projects emphasise speed and flexibility over cost.
- ▷ Enthusiastic partners are key to meeting deadlines.
- ▷ BDM/OCDSs halve tool-chain costs.
- ▷ Complex 32-bit microcontrollers can simplify design.
- ▷ Don't ignore potential hardware-layout issues.

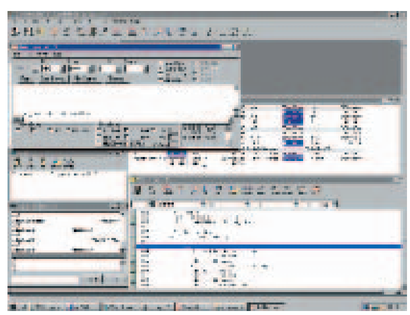

Figure 1 Getting this Tasking CrossView debugger screen is the first step to TriCore development success.

The I/O board carries three PC-104 stack-through connectors that plug into the motherboard, with the processor board becoming the top board in a three-pc-board stack. A custom-made enclosure and pc-board mounting hardware ensure that the composite assembly withstands the mechanical shock loadings that plague competition vehicles. Harwin's €3 (100) PC-104 connectors are very rugged and specified for −55 to +105°C operation. With mechanical detailing by ex-Lotus Formula One designer Martin Ogilvie at Prototype Car Designs, the Hercules enclosure provides around 0.5 mm clearance between the lid and the top connector. This clearance ensures that even if the pc-board mounts break, the boards can't separate and should survive and work through an accident situation.

CHOOSING PROCESSORS ISN'T TRIVIAL

With the stand-alone prototype complete and with encouraging bench- and field-test results available, project management approved the second development phase that requires processor control. Here, the real pressure started when a customer requirement to run the processor-controlled Hercules in an event-specification car demanded that the first prototype appear within just eight weeks. Worse, this period straddled Christmas and New Year's. Although this situation is normal within motorsports, most other industries simply aren't geared up to respond with similar alacrity. In a marketplace in which volumes are low and timescales are uncompromisingly short, it's imperative to select partners who will unquestionably provide support. It's therefore a tribute to all the project's commercial partners that the first prototype came to life with around 12 hours to spare.

The first obstacle, choosing a microcontroller, is always challenging. According to a recent survey, engineers rate these criteria as their first thoughts when choosing new processors: available software tools (66.9%); price (50.7%); available I/O (39.5%); available hardware tools (35.2%); and code compatibility (26.7%, **Reference 3**). Hercules has slightly different perspectives. With almost 200 signals to handle, the project has demanding I/O capabilities that include 32 channels of ADC, two CAN (controllerarea-network) ports, and at least one serial port. Industrial or extended operating-temperature range is essential but comes as standard with devices in this market segment. And although available development tools are a prerequisite for any project, processor price and code compatibility are virtually irrelevant in this project's context. Crucially, the processor and its support circuitry must fit within the limited space that Hercules offers and contribute as little as possible toward power dissipation (see **sidebar** "Don't neglect physical issues").

These considerations suggest a processor with extensive I/O and sufficient on-chip memory to run the application without requiring any peripherals other than power supplies and support circuits. Hercules is undemanding of computational power, but reliability is key, so the processor must include comprehensive error-trapping mechanisms. Together, these requirements suggest a 32-bit machine that carries the memory, I/O, and reliability-enhancing features, but in which the computational power is wasted. The guiding principle of "simplest is best," together with familiarity with various 68x and x86 architectures, suggests that microcontrollers such as Infineon's SAB167CS and Motorola's MC68376 may suit the need. Each of these devices

DON'T NEGLECT PHYSICAL ISSUES

With today's emphasis on hardware integration and structured software design, it's easy for development projects to relegate mundane issues, such as physical circuit layout. Although PC-104 connectors ideally suit the layout of Hercules motherboards, their central arrangement challenges the processor board and its various buses and peripherals. The limiting factors for the project's processor pc board combine a maximum outline of 230×135 mm with the necessity for an autorouter to connect each of the 192 connector pins. As always, it's desirable that the production version of the pc board is as small as possible and occupies the minimum number of layers using commodity track-and-spacing rules—say, eight layers maximum and 6-thou (0.15-mm) rules. But the prototype boards conservatively consume every available square mil and prudently include a wire-wrap area (**Figure A**).

Figure A The initial TriCore board occupies as much area as possible and includes a prototyping area for those afterthought-engineering exercises.

Initial routing tests show that the best 16-bit microcontroller and peripheral combination requires far more layout effort than a more highly integrated device, such as the TC1775B. Also, using the TC1775B eases circuit design, and there are fewer parts to procure. But with no experience in BGA technology, the biggest design challenge involves escaping the 304 pins that occupy the four outer rows of the 1.27-mm-pitch, 23×23-pin package. (The central 5×5-pin matrix carries power and ground connections to the processor's 2.5V core.) Other issues include choosing SMD (solder-mask-defined) or NSMD (non-solder-mask-defined) pads to connect the package to the board. Although NSMD pads follow the conventional space between copper land and the surrounding solder mask, an SMD pad uses the solder mask to overlap the copper to define the land area (**Figure B**).

Amkor supplies the TC1775B's package, and the company's original information suggests that SMD pads improve reliability (**Reference A**). Inspecting the TriBoard's pc board suggests that this board uses SMD pads, supporting the decision to use SMD technology. However, a later Amkor document suggests that NSMD pads are as much as 3.1 times more reliable than SMD (**Reference B**). You also need to consider the routing issue: Motorola's AN1231 application note shows that 1.27-mm-pitch SMD pads restrict track-and-space rules to 6 thou (0.15 mm) compared with 8 thou (0.20 mm) for NSMD types. Because many pc-board-design packages apply global clearances for the solder-resist mask, it's also easier to implement NSMD pads. Otherwise, you may need your pc-board supplier's help to mask the PBGA area. For these reasons, future PBGA designs will use NSMD technology. In the event, four signal layers and 6-thou (0.15-mm) track-and-space rules wouldn't allow the Pulsonix pc-board-design package's autorouter to complete the board's routing. Bob Williams, marketing director at Pulsonix, rescued this situation using Zuken's Cadstar Route Editor autorouter.

"If Route Editor can't route it, nothing can," says Williams. Realistically, more time and another approach should allow the Pulsonix router to succeed. Then, using what sales manager Philip King calls its heroic turn-around-time service, Newbury Electronics fabricated, assembled, and delivered the board within a week. Newbury also hand-masked the SMD pads that provide perfect connectivity (**Figure C**).

Other hardware lessons include the desirability of adding external SRAM to your prototype TriCore design. Without external SRAM, the Hitop debugger can't download programs to flash memory. You then need expensive hardware just to flash a board. Alternatively, build a simple "wiggler" to interface a PC's parallel port with the 16-pin OCDS-1 header on your target (**Figure D**). Evaluation software such as PLS' elegant Universal Debug Engine can then program the target's flash. For around €3000, HighTec's Gnu C/C++ compiler and the PLS

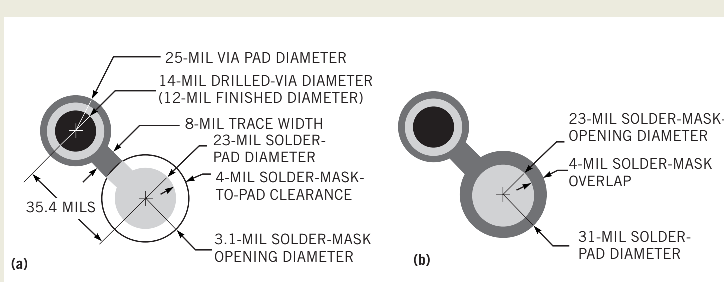

Figure B Compare non-solder-mask-defined pads (a) with solder-mask-defined pads (b), which employ the pc board's solder-resist mask to define the BGA's land areas.

has most of the features that the application demands and, with appropriate peripherals, can meet the remainder. But remaining questions concerning tool-chain support and pc-board space require test routing to prove. Because tool-chain support is easier to assess in a limited timescale, it takes priority.

Although a huge range of development aids is available for Motorola processors, such as P&E Microsystems' less-than-€500 BDM (background-debug-mode) tools, the general perception is that Motorola serves high-volume sales and that support for low-volume projects is patchy. Conversely, experience with Infineon reveals a highly responsive company, but the full tool chain to support SAB167CS development is costly. Phytec's starter-kit board for the single-CAN port SAB167CR derivative costs around €215, and the bundled evaluation version of Keil's C-compiler is a joy to use. But, because the SAB167 is a traditional 166 machine, you need a conventional bond-out processor ICE for emulation, and the tool-chain costs for a full-blown project quickly approach €12,000. You also need the space around the processor to accommodate the ICE connection system. It's worth noting that later processors, such as the C161U and C165UTAH, carry Infineon's OCDS (on-chip debug sys-

Universal Access Device complete a powerful but affordable development system. Without a GUI or an IDE, the Infineon-sponsored port of the Gnu compiler is no thing of beauty, but HighTec stresses the product's cross-platform capabilities. If you build a Linux PC, you can access a superb range of tools for free to support Gnu's native environment (**Reference C**). For the Windows environment, 2Step's principal programmer, Steve Robinson, believes that it's minimal work to provide a user-friendly front end in VisualBasic. Hardwarewise, the compiler cannot currently support the TriCore's peripheral-control processor, but the basic chip is so powerful that many applications won't need to offload peripheral control from the core.

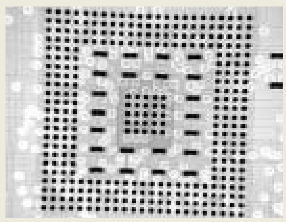

Figure C

Inspection X-ray photos show that the PBGA perfectly connects with the pc board's SMD pads.

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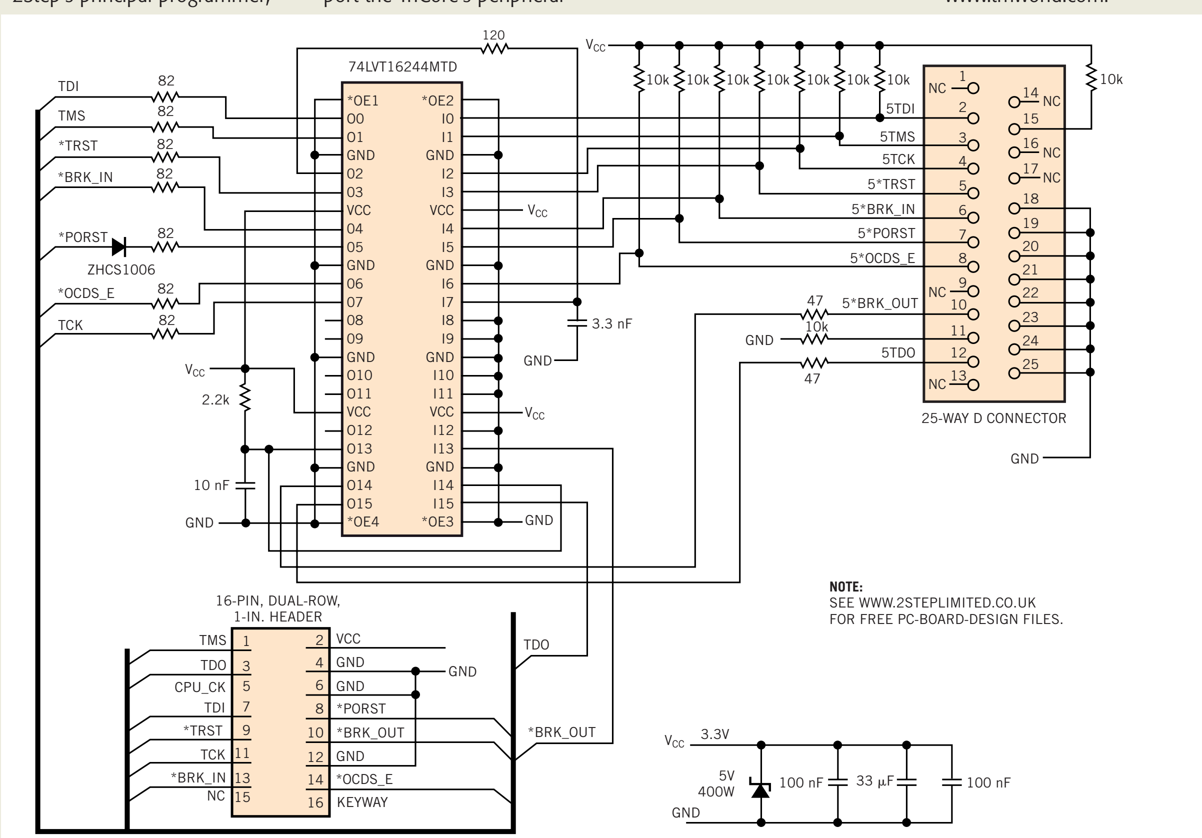

Figure D

With appropriate driver software, a simple hardware wiggler provides a low-cost method of programming target flash memory.

tem), which works via the JTAG port, lowering midrange tool-chain costs to around €4500 and reducing ICE-connection requirements to a simple header.

32-BIT μCs REPRESENT VALUE FOR MONEY

For low-volume projects for which unit cost isn't key, the relative value that BDM/OCDS tools provide, together with the advantages that a top-flight 32-bit microcontroller offers, are compelling. Another argument reasons that you can never have enough computing power and that what you don't use today, you'll need for another project. Lastly, if you're going to commit to a new architecture, get the best futureproofing possible. These observations focus attention on Motorola's MPC555 PowerPC and Infineon's TC1775B TriCore, which target automotive applications. Both devices partially fulfill Hercules' I/O demands and add a plethora of features that are immediately useful and safeguard future needs. Of these two, the MPC555 initially looked most attractive; the device carries sufficient on-chip flash to fulfill the application's needs. The TC1775B requires external code memory.

The MPC555 features a 40-MHz core with a floating-point unit, 448 kbytes of in-system-programmable flash, 26 kbytes of static RAM, and a memory-protection unit. It also offers two CAN 2.0B ports, 32 analogue inputs, and a flexible I/O system. Two timer/processor units and a multichannel serial module further suit Hercules. And, you can get started with the MPC555 using very low-cost tools, such as Intec Automation's development board kit, which costs around €1000, including P&E's BDM debugger and the freeware Gnu C/C++ compiler. But, although the MPC555 has been in production for some time, distribution enquiries reported a 12-week leadtime, effectively taking the device out of contention. Further enquiries also suggest that the MPC555 has the reputation of being very hard to program. Clearly, such user perceptions are highly subjective.

Alternatively, the TC1775B derivative of Infineon's TriCore architecture is a brand-new chip and was qualified only this year, meaning that there was no distribution stock. But Infineon's UK microcontroller products manager, Wendy Walker, approached TriCore product manager Bjoern Steurich in Munich to source the development samples that allowed the project to proceed. With the exception of having no on-chip flash, the 329-pin TC1775B is a better fit for Hercules than the 272-pin MPC555 because the TC1775B's PBGA package offers yet more available I/O. The TriCore carries a range of peripherals, including two CAN ports that augment the chip's main core, a DSP block, and a peripheral-control-processor subsystem. On-chip user memory comprises 32 kbytes of data SRAM, 32 kbytes of code scratchpad SRAM, and 8 kbytes of SRAM, making it suitable for battery backup. This last feature is useful to maintain control-state settings between test runs, when it's likely that technicians will disconnect the car's master-switch power. And from a programmer's perspective, it's relatively easy to port 166 code onto a TriCore, providing a familiar entry point. In production quantities, the TC1775B's guide price is around €20 (50,000); low-volume distributor pricing is around €30 for a 162-piece reel.

The TriCore also has an encouraging choice of ICE and similar tools from vendors including Abatron, Ashling Microsystems, Hitex, Lauterbach, PLS, and Signum Systems. Compiler vendors include Green Hills Software, HighTec, and Tasking; yet more tools appear at Infineon's Space Program Web site at www.spacetools.com. Most hardware tools and software debuggers exploit the TC1775B's OCDS Level 1 capability that provides access to on-chip hardware and runtime control via a 16-pin header (**Reference 4**). But top-spec tools from vendors such as Ashling, Hitex, Lauterbach, and PLS can access a 40-pin OCDS Level 2 connector to support real-time trace reconstruction. Level 1 suits applications such as Hercules that run few time-critical processes from a simple scheduler, such as a block of analogue-to-digital conversions. But with an eye to future projects, OCDS Level 2 capability suits demanding applications such as powertrain management with multiple time-critical processes running under RTOS supervision.

Figure 2 The Hitex Hitop debugger intuitively views and reports processor and peripheral conditions.

Infineon's TriBoard kit is the starting point for TC1775B development. Made by TQ Components, the kit comprises a 100×160-mm pc board that carries the processor, 4 Mbytes of burst-mode flash, and 1 Mbyte of SRAM, together with clock sources and power supplies. There's an array of I/O connections that feed four 80-pin headers, into which you can plug optional breakout boards for easy access to signal lines. The board communicates with a PC using a "wiggler" parallel-port interface to its OCDS-1 system; a DB9 connector hosts RS-232 serial communication. Separate headers carry the second RS-232 port and signals to both CAN ports. Two further headers provide access to the OCDS-1 and OCDS-2 lines to suit external hardware tools. The starter-kit CD furnishes comprehensive documentation that usefully includes the circuit diagrams. You also get three manuals that describe the TriCore's architecture, system units, and peripheral units. Software support includes Infineon's DaVE (digital application virtual engineer), which automates processor setup scripts; evaluation versions of the Hitex Hitop debugger and Tasking's C-compiler; and the Space Program development-tools-sampler CD. Available from Hitex, the kit includes an ac adapter and costs around €420; a set of four breakout boards costs €120.

SUCCESS REWARDS PATIENCE

When you're armed with the TriBoard kit, you'll need some patience to get up and running. First, locate all the software components that you need. After some experimentation, the most straightforward strategy loads the Hitop debugger and the Tasking demo compiler from the Hitop debugger-starter-kit CD. According to the documentation, you need a Win NT/2000 machine to support the wiggler driver, but a Win 98 machine has been running it without protest. Notice that the Hitop setup process immediately fails if you don't have a sound card in your machine, so run Setup.exe from the hitop_tc1775 subdirectory. Problems such as this one waste time, and there are several others to overcome. For example, to preserve default paths, install the Tasking software in its default directory. If you then follow the instructions in the TriBoard manual under "Starting a new Tasking EDE project," you should compile, upload, and run the getting-started project that's on Infineon's Starter Kit CD. When you see the Tasking CrossView debugger display and the RS-232 activity monitor in **Figure 1**, you've overcome the first hurdle.

The Hitop debugger is more powerful than CrossView but tricky to get going, despite some useful notes (**Reference 5**). In particular, the View-User facility that displays the processor's system and peripheral units is highly intuitive, with mappings that closely reflect the TC1775B's user-manual conventions (**Figure 2**). Tasked with writing the prototype code for Hercules, 2Step Ltd's principal programmer, Steve Robinson, found that several support calls resolved issues such as which files Hitop and the Tasking demo need to run and the location of these files. But when you're successful, Hitop facilitates uploading programs to the TriBoard's SRAM or programming its flash. Notice that running programs from flash can be as much as three times faster than SRAM due to the TC1775B's support for burst-mode memories (AMD's Am29BL162CB on the TriBoard).

Because Hercules is the first TriCore application to surface in the United Kingdom, it's not surprising that there were some "teething" troubles. Thanks to assistance from Infineon field application engineer Karl Smith, the board's hardware worked perfectly the first time. But commissioning the tool chain was challenging. The demo version of the Tasking compiler is Version 1.3, but the full product is currently Version 1.4, which has substantial differences that seemingly include incompatibility with Infineon's DaVE software. (The Web site now suggests that Version 1.5 is shipping.) The defacto standard for TriCore development, Tasking's product is doubtlessly technically excellent, but it is abstruse. Amazingly, for a compiler that targets embedded applications, no example of how to use the TriCore's peripherals or subsystems exists. Robinson of 2Step also observes that to further automate the building process, the later version obscures the locations of key files. Until you understand what's going on, this situation creates havoc.

Enter Hitex UK's TriCore expert, Mike Beach. One Saturday last February, he visited 2Step's lab to configure the tool chain, build the project, and download the object code that sent Hercules to its critical test debut. The basic OCDS-1 version of the Hitex Tanto-TC costs around €3800, and the Tasking compiler costs €4800, including 12 months of updates. For more demanding applications, the Tanto-TC with its trace unit costs around €8700 to exploit the processor's OCDS Level 2 features.□

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