

Figure 2

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(Sfr1) SFR - EBU Part 2 .Bus Configuration [BUSCON0...3;ADDSELO...3]
Write Protection                               BUSCON0:00020A81          BUSCON1:00020000
Adr.Latch Duration Control                     Enabled                   Enabled
Byte Control Signal Timing                     0                         0
Address Generation Control                     chipselect mode          chipselect mode
Multiplier Control Read                       Demuxed address          Demuxed address
Wait State Control                             Multiplier is 1          Multiplier is 1
Active Wait Level Control                     Disabled                 Disabled
Address Setup Control                           Low active               Low active
Data Width Control                             Cycle 0 is not generated Cycle 0 is not generated
WAITRDC                                        32-bit data             32-bit data
WAITWRC                                        5                         0
HOLD.C                                        2                         0
HOLD.C                                        0                         0
RECOUC                                        0                         0
Multiplier Control Wait                       Multiplier is 4          Multiplier is 1
ADDSEL0: B0000061                             ADDSEL1: A0000071
Memory Region Base Address                    30000                    20000
Memory Region Address Mask                    6                         7
Mirror Enable Control                          not mirrored into segment 0xB not mirrored into segment 0xB
Region Enable Control                          enable                    enable

Write Protection                               BUSCON2: E80261FF          BUSCON3: E80261FF
Adr.Latch Duration Control                     Disabled                 Disabled
Byte Control Signal Timing                     3                         3
Address Generation Control                     control mode             control mode
Multiplier Control Read                       Demuxed address          Demuxed address
Wait State Control                             Multiplier is 1          Multiplier is 1
Active Wait Level Control                     Disabled                 Disabled
Address Setup Control                           Low active               Low active
Data Width Control                             Cycle 0 is not generated Cycle 0 is not generated
WAITRDC                                        32-bit data             32-bit data
WAITWRC                                        48                        48
HOLD.C                                        7                         7
HOLD.C                                        3                         3
RECOUC                                        3                         3
Multiplier Control Wait                       Multiplier is 16         Multiplier is 16
ADDSEL2: A0000001                             ADDSEL3: A0000001
Memory Region Base Address                    20000                    20000
Memory Region Address Mask                    0                         0
Mirror Enable Control                          not mirrored into segment 0xB not mirrored into segment 0xB
Region Enable Control                          enable                    enable

No register currently selected

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The Hitex Hitop debugger intuitively views and reports processor and peripheral conditions.