



What if bigger isn't better?

Our ability to put more functions and more gates onto one die—whether you call it an SOC (system on chip), an ASIC, or just one big IC—is increasing rapidly. Driven by submicron design and fabrication and supported by better EDA tools and libraries, you can

pack millions of subcircuits onto your silicon. The situation may make you think that a custom, one-IC architecture—perhaps with a few oddball, smaller scale devices supporting it—will capture every design.

But one factor has me wondering about the general viability of these huge ICs, and perhaps it should worry you, too. Reading a recent article discussing the Apple iPod reminded me that this concern was lingering in the back of my mind (**Reference 1**). The article notes that despite volumes of tens of thousands of pieces per month, Apple's designers chose standard, albeit advanced, medium-complexity ICs for the unit. Their reasons were varied: They looked at the risks associated with a large IC, the time to first shippable silicon, and of course, the cost per part. If this mass-market application—driven by size, cost, and complexity—couldn't afford a custom SOC, which ones could?

In theory, a single IC should be less expensive than several smaller ICs, in terms of the direct cost of parts as well as the indirect costs of component handling, pc-board real estate, power, and interconnect functions. But several counterbalancing factors exist—even as leading-edge wafer sizes reach 300 mm, and feature sizes drop to less than a micron. The cost of a mask set is in the \$1 million range (and that first mask set may not be the shippable design), and the cost of the fab facility is in the \$1 billion stratosphere. At the same time, larger dice

may not make use of wafer space as efficiently as smaller dice do. Thus, the upfront, one-time costs associated with getting your first qualified IC may simply overwhelm any per-piece savings, unless your volumes are quite high. Further, your first-time successful design risk is even harder to quantify, and the cost of

In the end, the challenge of engineering is not only the skillful execution of the design itself but also the examination of alternative system architectures and structures that meet often-conflicting design goals and constraints. You might find that smaller building blocks, cleverly combined, provide the most attractive alternative for your situation.

REFERENCE

1. Sherman, Erick, "Inside the Apple iPod Design triumph," *Electronics Design Chain*, www.design-chain.com, Summer 2002.

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missing a market window is severe.

And there's the problem. Few products these days can anticipate such high volumes for a long enough period. Perhaps a mainstream microprocessor from Intel or AMD, a processor for a cell phone, or the core functions of a moderately priced DVD player will have the necessary numbers, but I suspect the list is fairly short. For the rest of the design world, the volumes simply aren't going to happen, so you face the trap of the seductive siren song of more functions and bigger ICs versus realistic sales numbers and technology traps.

Luckily, you do have alternatives. Programmable ICs may be cost- and design-time-effective alternatives, as are semistandard ICs, which vendors partially fabricate and then finish to your requirements. Reconfigurable ICs may do the job as well. Or, you can consider a combination of standard medium-scale, off-the-shelf ICs, which provide a fast time to market at a low risk but perhaps at higher parts and board-space cost.

