



Capacitor layout matters

HAVE TOO MUCH NOISE on the 3.3V inputs to my ASIC. An FFT analysis of the noise indicates that it peaks at 125 and 300 MHz. The noise is coincident with the edges of the 25-MHz clock that the ASIC drives out onto my backplane.

You have said many times to keep power and ground breakouts on all ASICs very short and provide all bypass capacitors with power and ground vias tangential to their pads. Unfortunately, a group in another country did this board, and they did not take these precautions. The power and ground breakouts are 8-mil tracks with a length of 130 to 250 mils. The bypass capacitors are

bypass capacitor, not the values of types of capacitance. To obtain less inductance without changing the layout, you'd have to install capacitors with negative lead inductance. If you find any such capacitors, let me know—maybe we can use them to make a time-travel circuit!

Seriously, to demonstrate the deleterious effects of the breakout

extending each VCC via toward the nearest ground via with a square of copper, again using paper under it, and then hand-soldering a surface-mounted bypass capacitor directly between the copper foil and the ground via.

Only by re-laying out the card with the power and ground vias directly adjacent to the bypass capacitors will you exceed whatever improvements you gain by exchanging your breakouts for squares of copper. You should eliminate the ASIC breakouts on power and ground pins as well.

If you are fighting a culture that doesn't believe in layout inductance, try this scenario. Resolder each capacitor to just one of its pads, standing on end like a tombstone. Then use wire-wrap wire to connect the top end of each capacitor to its other pad. This step increases the series inductance of each capacitor and should result in a marked increase in the VCC noise. Your system may not even function. Such a demonstration convinces people that layout *really matters*. □

WILL CHANGING THE VALUE OF THE BYPASS CAPACITORS HELP REDUCE MY NOISE?

0805 0.01- μ F capacitors with 20-mil-wide breakouts that are 130 to 150 mils long on each end. There are six capacitors on each side of the 160-pin PQFP package, which has 27 power pins and 27 ground pins.

Will changing the value of the bypass capacitors help reduce my noise? I know I can fix the problem with a new layout, but I need a way to reduce the noise with the current artwork as well.

—Doug Collier, Nortel Networks

Your problem is likely caused by the layout, which has more than tripled the inductance of each

traces, solder little squares of copper 150 mils long and 300 mils wide in parallel with each breakout trace. You must press down the squares against the board with paper under them so they don't short anything out, and you must solder them from every power or ground via to its respective destination. Take careful before-and-after measurements to document the extent of improvement.

Alternately, if the back of your board is clear, you can replace the capacitors on the front of the board with better ones on the back. Do this step on the back by

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