



32-BIT MICROPROCESSORS

Company name	Device family or device	CPU frequency	Bus interface (address/data) (bits)	Instruction width (bits)	Operating voltages (V)	Typical power at maximum frequency	Power-down modes	DSP/multiplication hardware support (bits)	FPU	Caching
Altera www.altera.com Enter No. 330	Excalibur: EPXA1 EPXA4 EPXA10	133, 166, or 200 MHz	32/32	16, 32	1.8, 2.5, 3.3	2W (FPGA-logic dependent)	Low-power mode (EPXA1)	32×8, user definable	Can be added in FPGA	8-kbyte instruction/data
	Nios	As much as 125 MHz	16/16 or 32/32	16	1.5, 1.8, 2.5, 3.3, or 5		Clock reduction via static design	250 MHz, 36×36 DSP block, two-cycle 16×16, 1-bit/clock, user definable	Can be added via custom instruction	
AMD www.amd.com Enter No. 331	Au1000 Au1100 Au1500	266, 333, 400, or 500 MHz	32/32	32	1 to 1.2/2.5 or 3.3	200 mW to 1.2W	Idle, sleep	MAC		16-kbyte instruction/data
	ElanSC520	100 or 133 MHz	PCI Revision 2.2	32	3.3/5 tolerant	1.6W			Yes	16-kbyte write-back
ARC International www.arc.com Enter No. 332	Tangent-A4	Implementation specific	24/32 instruction address, 32/32 data	32	Implementation specific	0.5 mW/MHz (0.18 micron at 1.8V)	Sleep	16/24-bit and dual 16 MAC, XY memory, modulo, bit-reverse, preincrement/post-increment two 32×32 options	Can be added	Up to 32-kbyte instruction/data, direct-mapped, two- or four-way-set associative, line locking
	Tangent-A5	Implementation specific	32/32	32/16	Implementation specific	Implementation specific	Sleep	Dual 16-bit MAC, dual 16 multiply-subtract, XY memory, 32×32 or dual 16×16 options	Can be added	Up to 32-kbyte, single-, two- or four-way
ARM www.arm.com Enter No. 333	ARM7 Thumb	100 to 133 MHz	AHB 32	8, 16, 32	1.2	0.06 to 0.2 mW/Hz	Yes	Yes, DSP		Up to 8-kbyte unified
	ARM9 Thumb	180 to 250 MHz	AHB 32	16, 32	1.2 to 1.8	0.25 to 0.8 mW/Hz	Yes	Yes		4- to 16-kbyte instruction/data
	ARM9E	180 to 250 MHz	One or two AHB 32	8, 16, 32	1.2	0.4 mW/Hz	Yes	Yes, DSP	Coprocessor	Configurable
	ARM10E	266 to 350 MHz	Dual AHB 64	8, 16, 32	1	0.5 to 0.6 mW/Hz	Yes	Yes, DSP	Coprocessor	16- to 32-kbyte instruction/data
	Secure-Core	80 to 110 MHz			1.8	0.21 to 0.35 mW/Hz	Yes	Yes, DSP, cryptography		
Fujitsu Microelectronics America www.fma.fujitsu.com Enter No. 334	FR Series	25 to 66 MHz, subclock 32.768 kHz	32/32, external: 24/16	16	2.3 to 5.5	230 mW	Sleep, stop, subclock mode, timer	DSP macro/32×32 with barrel shifter and bit search		Up to 4-kbyte instruction
Hitachi Semiconductor www.semiconductor.hitachi.com Enter No. 335	SH7047F	50 MHz	32/32	16	4.5 to 5.5	220 to 235 mA (50 MHz/5V)	Four	32 multiplier (32×32+64)		
	SH7145F	50 MHz	32/32	16	3.3	160 to 220 mA (50 MHz/3.3V)	Four	32 multiplier (32×32+64)		
	SH7706	133 MHz	32 (29 bits external)/32	16	1.9 internal, 3.3 I/O	475 mW	Four	32 multiplier (32×32+64)		16-kbyte four-way
	SH7750R	240 MHz	32 (29 bits external)/64	16	1.5 internal, 3.3 I/O	345 mW	Four	32 multiplier (32×32+64)	Single-precision (32 bits), double-precision (64 bits)	16-kbyte instruction, 32-kbyte data
	SH7751R	240 MHz	32 (29 bits external)/32 and 32-bit PCI bus	16	1.5 internal, 3.3 I/O	382 mW	Four	32 multiplier (32×32+64)	Single-precision (32bits), double-precision (64 bits)	16-kbyte instruction, 32-kbyte data
IBM www.chips.ibm.com Enter No. 336	403GA 403GCX	25 to 80 MHz	32/32	32	3.3	0.51W (80 MHz)	Wait: 30 mW, sleep: 0.1 mW	32×32		2- to 16-kbyte instruction, 1- to 8-kbyte data
	405GP/CR	200 to 266 MHz	32/8, 16, 32	32	2.5 or 3.3	2W (GP: 266 MHz)		16×16 MAC/32×32		16-kbyte instruction, 8-kbyte data
	405GPr	266 to 400 MHz	32/8, 16, 32	32	2.8 or 3.3	1.3W (333 MHz)		16×16 MAC/32×32		16-kbyte instruction/data

	Memory	Memory controller	MMU	Package selection	Timers	Serial, parallel I/O	Interrupts	ADC/DAC	Additional features	Price (10,000)
	32- to 256-kbyte SRAM, 16- to 128-kbyte dual-port SRAM	SDRAM, flash	Dual 64-entry TLB	484, 672, 1020 FBGA	32-bit, watchdog	UART, parallel can be added in FPGA	Can be added in FPGA		ARM922T core with 4000, 16,000, or 38,000 logic elements; AMBA/AHB1/AHB2 buses; JTAG debug and ETM9 trace; optional 10/100-Mbps Ethernet	\$45 to \$500
	Up to 12 64-kbyte RAM blocks, multiple configuration register file	SRAM, SSRAM, SDRAM, flash		TQFP, RQFP, PQFP, BGA, FBGA	32-bit, watchdog, PWM, configurable	RS-232, SPI, Ethernet, GPIO, IDE, PCI, configurable	As many as 64, configurable		Custom instructions, simultaneous multiple master bus	License- and royalty-free in Altera PLDs
		SRAM, SSRAM, SDRAM, flash	Yes	324, 399, 424 PBGA		Two to four UARTs, 32 to 48 GPIOs, USB host/device, AC97, I ² S, up to two SSI, IrDA, PCI	Yes		One or two Ethernet, LCD controller, two secure digital controllers	\$29.50 to \$34.38 (400 MHz)
		SDRAM		388 PBGA	Programmable interval, general purpose, software, real-time clock, watchdog	Two 16650 UARTs, synchronous serial, 32 PIOs, PCI bus Revision 2.2	22 levels		JTAG debug	\$23.38
	Up to 16-kbyte RAM, scratchpad	SRAM, external bus-mastering capability		User option	Two free-running 32-bit, user definable	Up to eight UARTs, optional parallel/JTAG port, user definable	16 (three levels), as many as 16 more		Optional: 10/100-Mbps Ethernet MAC, Bluetooth, USB 1.1 host/device controller	License per application
	Implementation specific	Implementation specific		Implementation specific	Implementation specific	Implementation specific	16 (three levels), as many as 16 more		Optional: 10/100-Mbps Ethernet MAC, Bluetooth, USB 1.1 host/device controller	License per application
			MMU				Yes		Jazelle (Java)	License
			MMU and MPU				Yes			License
	Configurable		MMU and MPU				Yes		Jazelle (Java)	License
	Configurable		MMU and MPU				Yes		Jazelle (Java)	License
			MPU				Yes		SecureCore	License
	Up to 512-kbyte flash, up to 160-kbyte SRAM	DRAM, DMA		100/160 QFP, 100/120/144 LQFP, 100 SQFP, 144 FBGA	UART, SIO, 16-bit reload, free-running, PWC, timebase, PPG, PWM	SIO, CAN, UART, I ² C, up to 120 PIOs	As many as 24 external	Up to 16-channel, 8/10-bit ADC; up to three-channel, 8-bit DAC	LCD, stepper motor, comparator, input capture, output compare, sound generator	From \$5
	256-kbyte flash, 12-kbyte RAM	Seamless interface to ROM, SRAM		100 QFP	Five 16-bit (MTU), two 16-bit (CMT), six-phase PWM, watchdog	Three serial channels, CAN	49 internal, five external	Two eight-channel, 10-bit	Data-transfer controller, on-chip debug	\$15.50
	256-kbyte flash, 8-kbyte RAM	Seamless interface to ROM, SRAM		144 LQFP	Five 16-bit (MTU), two 16-bit (CMT), watchdog	Four serial channels, I ² C	51 internal, nine external	Eight-channel 10-bit	Four DMACs, data-transfer controller, on-chip debug	\$14
	See cache	Seamless interface SDRAM, SRAM, ROM,	Yes	176 FPC, 208 TBPAV	Three 32-bit, real time, watchdog	Two serial channels	24 internal, 22 external	Four-channel 10-bit ADC, two-channel 8-bit DAC	Four DMACs, smart-card interface, on-chip debug	\$11
	See cache	Seamless interface SDRAM, SRAM, ROM	Yes	208 FPE, 256 BP	Three 32-bit, real time	Two serial channels	34 internal, 16 external		Eight DMACs, smart-card interface, on-chip debug	\$22
	See cache	Seamless interface SDRAM, SRAM, ROM, + PCI controller	Yes	208 FPE, 256 BP	Five 32-bit, real time	Two serial channels	39 internal, 16 external		PCI controller, eight DMACs, smart-card interface, on-chip debug	\$27.95
		DRAM, DMA	64-entry TLB, variable page size (GCX)	160 PQFP, 160 PBGA	Four	RS-232	Six external			\$11
	4-kbyte SRAM	32-bit PC100/133 SDRAM with ECC, DMA	64-entry TLB, variable page size	316/413/456 PBGA	Four	Two UARTs, I ² C, GPIO	Seven external		32-bit PCI, Ethernet MAC	\$25
	4-kbyte SRAM	32-bit PC100/133 SDRAM with ECC, DMA	64-entry TLB, variable page size	456 PBGA	Four	Two UARTs, I ² C, GPIO	Seven external		32-bit PCI, Ethernet MAC	\$25

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	NPe405L	133 to 266 MHz	28/8, 16	32	2.5 or 3.3	1.8W (266 MHz)		16×16 MAC/32×32		16-kbyte instruction, 8-kbyte data
	NPe405H	133 to 266 MHz	32/8, 16, 32	32	2.5 or 3.3	2.5W (266 MHz)		16×16 MAC/32×32		16-kbyte instruction, 8-kbyte data
	440GP	400 to 500 MHz	32/8, 16, 32	32	1.8, 2.5, or 3.3	Less than 4W (400 MHz)		16×16 MAC/32×32		32-kbyte instruction/data
	EM603e	200 MHz	64/32	32	2.5 or 3.3	4W (200 MHz)	Doze: 1.5W, nap: 150 mW, sleep: 120 mW	32×32, fixed-point unit	IEEE-754 compatible, single/double precision	L1: 16-kbyte instruction/data
	740750	300 to 533 MHz	64/32	32	2 to 2.1/1.8, 2.5, 3.3	6W (500 MHz)	Doze: 2.3W, nap: 250 mW, sleep: 200 mW	32×32, fixed-point unit	IEEE-754 compatible, single/double precision	L1: 32-kbyte instruction/data, external, L2: as much as 1 Mbyte
	750CXe	400 to 600 MHz	64/32	32	1.8/1.8, 2.5	6W (600 MHz)	Doze: 4W, nap: 950 mW, sleep: 700 mW	32×32, fixed-point unit	IEEE-754 compatible, single/double precision	L1: 32-kbyte instruction/data, L2: 256-kbyte with ECC
	750FX	600 MHz to 1 GHz	64/32	32	1.4, 1.8, 2.5, or 3.3	Estimated 3.6W (800 MHz)		32×32, fixed-point unit	IEEE-754 compatible, single/double	L1: 32-kbyte precision instruction/data, L2: 512-kbyte with ECC
IDT www.idt.com Enter No. 337	RC32332 RC32334	100, 133, or 150 MHz	23 (26 for RC32334)/32	32	3.3	1.5 to 1.8W	Wait	Four instructions		8/2-kbyte instruction/data, two-way set associative
	RC32351 RC32355	100 to 150 MHz	26/32	32	2.5 or 3.3	1.5W	Wait	Four instructions		8/2-kbyte instruction/data, two-way set associative
Improv Systems www.improvsys.com Enter No. 338	Jazz	As much as 200 MHz	16/32	32	User definable	20 mW	Halt, sleep, idle	DSP operations, saturation, bit reverse/16×16, 32×32, custom operations	User definable	
Infineon Technologies www.infineon.com/ microcontrollers Enter No. 339	TC111B	96 MHz	32/16/8	16, 32	1.8 or 3.3	900 mW	Idle, sleep, deep sleep	Dual MAC, signed fraction, modulo, bit reverse, pre-increment/postincrement, saturation, rounding		8-kbyte instruction, 8-kbyte data
	TC1765	40 MHz	32/16/8	16, 32	2.5 or 3.3 to 5	675 mW	Idle, sleep, deep sleep	Dual MAC, signed fraction, modulo, bit reverse, pre-increment/postincrement, saturation, rounding		1-kbyte instruction
	TC1775	40 MHz	32/16/8	16, 32	2.5 or 3.3 to 5	675 mW	Idle, sleep, deep sleep	Dual MAC, signed fraction, modulo, bit reverse, pre-increment/postincrement, saturation, rounding		1-kbyte instruction
	TC1920	100 MHz	32/16/8	16, 32	1.8 or 3.3		Idle, sleep, deep sleep	Dual MAC, signed fraction, modulo, bit reverse, pre-increment/postincrement, saturation, rounding		8-kbyte instruction
Intel Corp www.intel.com Enter No. 340	80386SSX 80386SX 80386DX	25, 33, or 40 MHz 16, 20, 25, or 33 MHz	32/32	32	5	300 mA				
	80386EX 80386XTB	25 or 33 MHz 25 MHz	32, external: 26/16	32	3.3 to 5	250 to 320 mA	Idle power-down			
	80486DX2 80486DX4	50 or 66 MHz 100 MHz	32/32	32	3.3, 5 tolerant	IntelDX4: 825 to 1075 mA; IntelDX2: 318 to 395 mA	Stop; auto halt/idle power-down		32-, 64-, 80-bit formats	8- or 16-kbyte instruction/data, write-back
	80486SX 80486GX 80486SSX 80960 Cx	33 MHz 33 MHz 33 MHz 16 to 40 MHz	32 16 32 32/32	32	3.3, 5 tolerant 5/5	220 to 289 mA, 180 to 220 mA 1034 mA	Stop clock, auto halt power-down Wait	Yes		8-kbyte instruction/data, write-through 1- to 4-kbyte instruction, 1-kbyte data

	Memory	Memory controller	MMU	Package selection	Timers	Serial, parallel I/O	Interrupts	ADC/DAC	Additional features	Price (10,000)
		32-bit PC100/133 SDRAM with ECC, DMA	64-entry TLB, variable page size	324 E-PBGA	Four	Two UARTs, I ² C, GPIO	Seven external		Two 10/100 Ethernet, 32-channel HDLC	\$23
		32-bit PC100/133 SDRAM with ECC, DMA	64-entry TLB, variable page size	580 E-PBGA	Four	Two UARTs, I ² C, GPIO	Seven external		32-bit PCI, four 10/100 Ethernet, 32-channel HDLC, eight-port HDLC	\$60
	8-kbyte SRAM	32/64-bit DDR-266 SDRAM with ECC, DMA	64-entry TLB, variable page size	552 CBGA	Nine	Two UARTs, I ² C, GPIO	13 external		32/64-bit PCI-X, two Ethernet MACs	\$75
			Four IBAT/DBAT registers; 128-entry, two-way-set-associative, TLB; software reload	255 CBGA	Two		One external			\$21
			Four IBAT/DBAT registers; 128-entry, two-way-set-associative TLB; hardware reload	255/360 CBGA	Two		One external		Thermal-assist unit, performance monitor	\$45
			Four IBAT/DBAT registers; 128-entry, two-way-set-associative TLB; hardware reload	256 PBGA	Two		One external		Thermal-assist unit, performance monitor	\$38
			Eight IBAT/DBAT registers; 128-entry, two-way-set-associative TLB; hardware reload	292 CBGA	Two		One external		Thermal-assist unit, performance monitor	\$60
		×32 SDRAM, 8/16/32-bit ROM/flash	32-entry TLB	208QFP (RC-32334 housed in 256BGA)	Three 24-bit	One or two 16550 compatible, 12 to 16 PIOs	Four, more via PIO		Two or three external devices via V2.1 PCI bridge, EJTAG debug	\$16 to \$19
		×32 SDRAM, 8/16/32-bit ROM/flash	32-entry TLB	208 QFP	Three 24-bit	Two 16550 compatible, USB 1.1, I ² C, 36 PIOs	Four, more via PIO		10/100-Mbps Ethernet port, 25-Mbps SAR, 8-Mbps TDM, EJTAG debug	\$22
	As man as four segmented SRAM ports/processor	Denali				Uses shared-memory access with SRAMs	Multiple levels		Composer tool suite customizes instructions, datapath, software-development tools	License
	1.5-Mbyte eDRAM, 68-kbyte SRAM	EBU (PC100 support)	Yes	388 PBGA	Six 32-bit (usable as 8- and 16-bit)	PCI, fast Ethernet, SSC/SCI, ASC (IrDA), 16×50, MMCI, 96 PIOs	24 external, 86 internal		Peripheral-control processor	\$63
	48-kbyte SRAM	32-bit, glueless, burst mode		260 PLBGA	Three 32-bit, 34×24-bit, 64×16-bit	TwinCAN, two SSC/SPI, two ASC, 77 I/Os, 24 analog inputs	More than 100 IRQ nodes	Dual 12-channel 8/10/12-bit ADC	Two four-channel DMAs, prescaler, duty cycle, phase discrimination, digital PLL	\$19
	92-kbyte SRAM	32-bit, glueless, burst mode		329 PBGA	Three 32-bit, 34×24-bit, 64×16-bit	TwinCAN, J1850, two SSC/SPI, two ASC, 11×16-bit parallel	More than 100 IRQ nodes	Dual 16-channel 8/10/12-bit ADC	Peripheral-control processor, prescaler, duty cycle, phase discrimination, digital PLL	\$25
	164-kbyte SRAM	32-bit, glueless, burst mode	Yes	260 PLBGA	Six 32-bit	TwinCAN, J1850, SSC/SPI, three ASC, 2 I ² C		Dual 14-bit CODEC	Peripheral-control processor, PLL	\$25
				132 PGA/PQFP			Maskable, NMI			\$5.12 to \$5.20
		Refresh-control unit		100/132 PQFP, 144 TQFP, 208 SQFP, 168 PGA	32-bit down-counter, watchdog	UART, SIO, three 8-bit GPIO	10			\$5.90 to \$21
				168 PGA, 196 PQFP, 176 TQFP, 168 PGA, 196 PQFP			Reset, maskable, NMI			\$8 to \$10.40
		Yes					Reset, maskable, NMI		Supervisor protection	\$15.20 to \$26.33; \$16.80 to \$29.28
							Reset, maskable, NMI			\$28.75 to \$33.25; \$6.40 (SSX) \$27.09 to \$67.56

32-BIT MICROPROCESSORS (CONTINUED)

Company name	Device family or device	CPU frequency	Bus interface (address/data) (bits)	Instruction width (bits)	Operating voltages (V)	Typical power at maximum frequency	Power-down modes	DSP/multiplication hardware support (bits)	FPU	Caching
	80960 HX	25 to 80 MHz	32/32	32	3.3 or 5	1578 mA	Halt, wait	Yes		8- or 16-kbyte instruction/data
	80960Jx 80960VH	16 to 100 MHz	32/as much as 32	32	3.3, 5 tolerant	480 to 690 mA	Halt	Yes		2- to 16-kbyte instruction, 1- to 4-kbyte data, stack frame
	80960Sx 80960Kx	10 to 25 MHz	32/16 or 32	32	5/5	340 to 420 mA		Yes	SB/KB only	512-byte instruction
	Pentium III	800 MHz	32/32	32	1.15	11.2W	Autohalt, stop grant, sleep, deep sleep		Yes	L1: 16-kbyte instruction/data, L2: 512-kbyte
	Celeron	650 MHz	32/32	32	1.15	8.3W	Autohalt, stop grant, sleep, deep sleep		Yes	L1: 16-kbyte instruction/data, L2: 256-kbyte
	Pentium 4	2000 or 2400 MHz	36/32	32	1.5	52.4 to 57.8W	Autohalt, stop grant, sleep, deep sleep		Yes	L1: 8-kbyte data, 12,000 decoded micro operations, L2: 512-kbyte
	Mobile Pentium 4-M	1700 MHz	36/32	32	1.3	30W	Autohalt, stop grant, sleep, deep sleep, deeper sleep		Yes	L1: 8-kbyte data, 12,000 decoded micro operations, L2: 512-kbyte
	Xeon	2000 MHz	32/32	32	1.5	58W	Autohalt, stop grant, sleep			Internal L1 and L2 caches
MIPS Technologies www.mips.com Enter No. 341	4Kx 4KEx 4KSx M4K	200 to 250 MHz	32/32	32	Process dependent	0.1 to 0.3 mW (0.13 micron)	Wait	One-cycle 16×16, 32×16, two-cycle 32×32		0 to 64-kbyte instruction/data
Mitsubishi Electric & Electronics USA www.mitsubishi-chips.com Enter No. 342	M32R/ ECU	32, 40, 64, or 80 MHz	32/32, external: 22/16	16, 32	2.7 to 3.3 or 5	600 mW		16×16, 32×16, 32×32 MAC instructions	IEEE single precision for M32R/ECU#5	
Motorola www.motorola.com/semiconductors Enter No. 343	ColdFire family	40 to 220 MHz	32	32, 16, or 8-bit dynamic 32-bit	3.3 or 5	1.3 to 4.2 mW/MHz	Doze, variable operation	MAC or EMAC/frequency hardware divide		1- to 16-kbyte instruction, up to 8-kbyte data
	MPC500 family	40 or 56 MHz	24/32	32-bit	2 or 5	800 mW	On, doze, sleep, deep sleep	Integer multiply and divide	Double precision	
	603e PowerPC	100, 133, 200, 266, or 300 MHz	32/32 or 64	32, 64	2.5 or 3.3	4W	Nap, doze, sleep	Single-precision multiply-add array	NaN, zero, infinity, normalized	16-kbyte instruction/data, four-way-set-associative
	MPC7410	400, 450, 500, or 533 MHz	32/32 or 64	32	1.8/1.8 to 3.3	5.3W	Nap, doze, sleep	Altivec: 128-bit vector unit	Three-cycle pipeline single/double-precision	L1: 32-kbyte instruction/data, backside, L2: 512-kbyte, 1- or 2-Mbyte
	MPC7440 MPC7450	533 to 700 MHz	32 to 36/64	32	1.8/1.8 to 2.5	13.3 to 15.9W	Nap, doze, sleep	Altivec: 128-bit vector unit	IEEE-754 single/double precision	L1: 32-kbyte instruction/data, L2: 256-kbyte, backside, L3: 1- or 2-Mbyte
	MPC755	300, 350, or 400 MHz	32/32 or 64	32	1.8 or 2, 1.8 to 3.3	4W	Nap, doze, sleep		Three- or four-cycle pipeline single/double precision	L1: 32-kbyte instruction/data, backside L2: 256-kbyte, 512-kbyte or 1-Mbyte
	MPC826X	100 to 266 MHz	18/32, external: 8 to 64 (configurable)	32	2.5 or 3.3; HiP4: 1.8/3.3	2.5W	Nap, doze, sleep, automatic for idle units		IEEE-754 compatible, single/double precision	16-kbyte instruction/data
	MPC8XX	50 to 80 MHz	32/32	32	3.3 or 5		Doze, sleep, deep sleep, power-down			Up to 16-kbyte instruction/data
National Semiconductor Corp www.national.com Enter No. 344	Geode GX1 family	200 to 333 MHz	64/64, external: PCI 32 (multiplexed)	8, 16, 32, 48	Core: 1.8 to 2.2, I/O: 3.3	1.2W at 2V, 00 MHz (80% active idle)	Active idle: 0.6W, standby: 170 mW, sleep: 140 mW (1.8V, 200 MHz)	8, 16, 32×8, 16, 32, MMX instructions	IEEE-754 compatible, single-precision, 64 or 80 bits	16-kbyte instruction/data

Memory	Memory controller	MMU	Package selection	Timers	Serial, parallel I/O	Interrupts	ADC/DAC	Additional features	Price (10,000)
2-kbyte RAM	GMU		168 PGA, 208 PQFP	Two 32-bit		Eight, NMI		Supervisor protection	\$34.60 to \$106.17
1-kbyte RAM	SRAM, flash		132 PGA/PQFP, 196/324 PBGA	Two 32-bit	I ² C	Programmable, high-speed controller		16/16 global/local 32-bit registers, high-bandwidth burst bus, JTAG	\$9.98 to \$68.17 \$44.20 to \$68
	Yes		84 PLCC, 80 QFP, 132 PGA/PQFP			Four, direct/handshake			\$7.98 to \$16.66; \$10.64 to \$39.03
	DMA		Micro-FCBGA					Dual-processor capable, streaming SIMD extensions	\$273
			Micro-FCBGA					Streaming SIMD extensions	\$116
			Micro-FCPGA2					NetBurst microarchitecture, rapid execution engine, hyperpipelined, advanced dynamic execution SSE2 instructions	\$191, \$393
			Micro-FCPGA					NetBurst microarchitecture, rapid execution engine, hyperpipelined, advanced dynamic execution, SSE2 instructions	\$236
			603 INT3					Hyperthreading technology	\$219
Configurable	Optional	16 dual-entry jTLB with variable page size or FMT mechanism		Optional				Synthesizable core, UDI, SmartMIPS ASE for code compression with cryptography acceleration	License
Up to 768-kbyte flash, Up to 40-kbyte RAM			144 to 240 QFP, 255 FBGA	As many as 64 multi-junction channels	As many as six SIOs, as many as to 2 CAN, up to 21 × 8-bit parallel	As many as 31 sources	Up to 32-channel, 10-bit	JTAG debug, wait controller	\$20 to \$45
4- to 96-kbyte SRAM	DRAMC, SDRAMC		144 LQFP, 160 MapBGA, 160QFP, 196MapBGA, 208QFP	Two to four 16-bit	I ² C, I ² S, QSPI, USB, UART, USART, FEC, GPIO	Three to eight external	12-bit	HDL software module, enhanced digital audio peripherals and software	\$6.99 to \$24.99
Up to 1.0-Mbyte, up to 50-kbyte SRAM	Four chip selects, 4-Gbyte (instruction)		352/388 PBGA	As many as three TPU3s, 12 PWMs, modular I/O with 22 channels	As many as four SCIs, two SPIs, more than 72 GPIOs	48 internal, eight external	Up to 40-channel on-chip	Real-time clock, JTAG/BDM, works in -40 to +125°C ambient temperature	\$20 to \$56
		4-Pbyte virtual; 4-Gbyte physical	240 CQFP, 255 CBGA, 255 PBGA			Yes			NA
		128-entry, two-way-set-associative, four BAT	360 CBGA/PBGA					MESI cache coherency, MPX bus, four-stage pipeline	\$58 to \$99
		128-entry two-way-set-associative, four BAT	360/483 CBGA					MESI cache coherency, MPX bus, four-stage pipeline	\$129 to \$300
		128-entry, two-way-set-associative; four BAT	360 PBGA					MESI cache coherency, MPX bus, four-stage pipeline	\$45 to \$78
	12 memory banks	Separate MMU for cache, memory	480 TBGA	Four 16-bit (usable as two 32-bit)	Four SCCs, three FCCs, two multi-channel HDLCs, four GPIOs (120 bits)	37 sources		IMA, TC layer, and PCI	\$75.60 to \$135
	Eight memory banks, DRAM, SIMMs, SRAM, EPROM, flash	Separate MMU for cache, memory	256/357 LPBGA	Four 16-bit (usable as two 32-bit)	Up to four full-duplex SCCs, two full-duplex SMC, four GPIOs (59 bits)	15 to 23 internal, seven or eight external		Simultaneous Ethernet/ATM, Utopia II multi-PHY/Slave, background debug	\$16.13 to \$51.91
	64-bit SDRAM, 66 to 100 MHz, four 168-pin DIMMs, 512-Mbyte total		352 EBGA					2-D graphics accelerator, display controller, PCI-host controller	\$29 to \$38

32-BIT MICROPROCESSORS (CONTINUED)

Company name	Device family or device	CPU frequency	Bus interface (address/data) (bits)	Instruction width (bits)	Operating voltages (V)	Typical power at maximum frequency	Power-down modes	DSP/multiplication hardware support (bits)	FPU	Caching
	Geode GX2 family	200 to 366 MHz	64/64, external: PCI 32 (multiplexed)	8, 16, 32, 48	Core: 1.2 to 1.4, I/O: 3.3	1 to 2W typical power (80% active idle)		8, 16, 32×8, 16, 32, MMX and 3DNow instructions	IEEE-754 compatible, single-precision, 64 or 80 bits	16-kbyte instruction/data
	Geode SOC family	200 to 300 MHz	64/64, external: PCI 32 (multiplexed)	8, 16, 32, 48	Core: 1.8 to 2, I/O: 3.3	1.6W at 1.8V, 233 MHz 2.1 at 2V, 266 MHz (80% active idle)	Active idle: 1.5W, standby: 110 mW	8, 16, 32×8, 16, 32, MMX instructions	IEEE-754 compatible, single-precision, 64 or 80 bits	16-kbyte instruction/data
Nazomi www.nazomi.com Enter No. 345	KCHIP Family JA108	104 MHz	Universal 16-bit SRAM interface	32	1.8/2.8, 1.8/3.3	150 mW	Suspend, standby			8-kbyte instruction/data
NEC Electronics www.necel.com Enter No. 346	V850/V850S	2 to 33 MHz/20 MHz	8/16	32	2.7 to 5.5	46 mW	Halt, stop	16×16+32		
	V850ES	2 to 20 MHz	8/16 (bus sizing)	32	2.2 to 5.5	30 mW	Halt, stop	16×16+32		Yes
	V850E	4 to 133 MHz	8/16/32 (bus sizing)	32	3 to 3.6	416 mW	Halt, stop	32×32+32		
NetSilicon www.netsilicon.com Enter No. 347	NET+Works Family	33 to 55 MHz	28/32	16, 32	1.5, 2.5, 3.3			Yes		
	NET+ ARM 40	33 MHz, 33 MHz, 33 MHz	28/32	16, 32	3.3	15 mW/MHz (maximum)		Yes		4-kbyte instruction/data
	NET+ ARM 50	44 MHz	28/32	16, 32	2.5/3.3	480 mW		Yes		8-kbyte instruction/data
	NET+ ARM 20M	44 MHz	28/32	16, 32	2.5/3.3	480 mW		Yes		
Oki Semiconductor www.okisemi.com Enter No. 348	ML670100	20 to 25 MHz	23/16	16, 32	2.7 to 3.6 or 3 to 3.6	60 mA	Stop, halt	Yes		
	ML671000	24 MHz	23/16	16, 32	3 to 3.6	70 mA	Stop, halt	Yes		
	ML674000 ML674001 ML67Q4002 ML67Q4003	33 MHz, 33 MHz, 33 MHz	24/16	16, 32	3 to 3.6	70 mA	Stop, halt	Yes		
Philips Semiconductors www.philips.semiconductors.com Enter No. 349	ARM7	As much as 50 MHz	32/32	16, 32	1.8/3.3	40 mW	Idle, power-down	32×32 MAC, DSP-core		
PTSC www.ptsc.com Enter No. 350	Ignite I, Ia	100 MHz	32 (multiplexed)	8	3.3 or 5	165 or 350 mW	Stop, halt	Yes	IEEE single/double precision	Single-cycle random access supported
	Ignite Ib/Iib/Illb/IvblIb.a, Ivb.a	200 to 400 MHz	32/8, 16, 32	8	1.8	81 to 110 mW	Stop, halt, sleep and dynamically variable frequency clock (0-maximum)	Yes	IEEE single/double precision	Single-cycle random access supported
QuickLogic Corp www.quicklogic.com Enter No. 351	QL902M	As much as 175 MHz	32/32	32	1.8 core, 3.3 I/O	Depends on programmable-logic usage		18 MAC blocks (8×8 multiply with 16 carry add)		16-kbyte instruction/data
Sharp Micro-electronics of the Americas www.sharpsma.com Enter No. 352	LH79520	77.4 MHz	26/32	16/32	1.8 core, 1.8 or 3.3 I/O 5 tolerant	55 mA	Standby: 35 mA; stop 1: 500 μA, stop 2: 18 μA	Yes		8-kbyte instruction 8-kbyte data
	LH7A400 LH7A404 LH7A405	200 MHz	26/32	16/32	1.8 core, 1.8 or 3.3 I/O, 5 tolerant	180 to 200 mA	Halt: 6 to 7 mA, standby: 20 to 35 μA	Yes		8-kbyte instruction/data

Memory	Memory controller	MMU	Package selection	Timers	Serial, parallel I/O	Interrupts	ADC/DAC	Additional features	Price (10,000)
	64-bit SDR (66 to 133) or DDR (133 to 266) SDRAM, four module banks, 1-Gbyte total		368 BGA						\$39 to \$41
	64-bit SDRAM, 66 to 100 MHz, two module banks, 512-Mbyte total		432 EBGA, 481 TEPBGA	Watchdog, ACPI	Three UARTs, parallel-printer port, IR, three USBs, as many as 27 PIOs			2-D graphics accelerator, display controller, PCI-host controller, audio	\$41 to \$45
Internal RAM	SRAM, ROM, flash		132 TFBGA (8×8 mm)					EJTAG debug, external resonator	\$5.59
Up to 512-kbyte ROM/flash, up to 24-kbyte SRAM			LQFP, FBGA	As many as eight-channel, 16-bit	UART, CSI, I ² C	17 external	Up to 12-channel, 10-bit	-45 to +85°C operation	\$8 to \$12
Up to 256-kbyte ROM/flash, up to 16-kbyte SRAM			LQFP, FBGA	As many as 10-channel, 8/16-bit	UART, CSI, I ² C	Eight external	Up to 16-channel, 10-bit	-45 to +85°C operation	\$8 to \$16
Up to 512-kbyte ROM/flash, up to 32-kbyte SRAM	EDO SDRAM, SRAM		LQFP, FBGA	As many as 10-channel, 16-bit	UART, CSI, I ² C	32 external	Up to eight-channel, 10-bit	-45 to +85°C operation	\$16 to \$25
	SRAM, SDRAM, DRAM		208 PQFP/177, 208 BGA	Two 26-bit, watchdog, bus	UART, HDLC, SPI, 1284, PIO	Four to 36 external		10/100BaseT Ethernet MAC, DMA, coprocessor interface	\$9.95 to \$24.95
Cache optionally configurable as 8-kbyte RAM	SRAM, SDRAM, DRAM		208 PQFP	Two 27-bit, watchdog, bus	Two (UART, HDLC, SPI), four 1284s, 24 PIOs	Four		10/100BaseT Ethernet MAC, 10-channel DMA, coprocessor interface	\$24.95
Cache optionally configurable as 16-kbyte RAM	SRAM, SDRAM, DRAM		208 PQFP, 208 BGA	Two 27-bit, watchdog, bus	Two (UART, HDLC, SPI), four 1284s, 40 PIOs	36		10/100BaseT Ethernet MAC, 10-channel DMA, coprocessor interface	\$13.95 to \$16.95
	SRAM, SDRAM, DRAM		208 BGA	Two 27-bit, watchdog, bus	(UARTs, HDLC, Two SPI), 16 PIOs	28		10/100BaseT Ethernet MAC, 10-channel DMA	\$9.95
128-kbyte ROM, 4-kbyte SRAM	SRAM, DRAM, MASK ROM, flash		144 LQFP	Multifunction timer (auto reload, capture, compare-output, PWM), watchdog	UART, SIO, 72-bit GPIO	19 internal, nine external	Eight-channel, 8-bit	ARM7TDMI core	\$7
4-kbyte SRAM	SRAM, DRAM, MASK ROM, flash		128 QFP	Multifunction timer (auto reload, capture, compare-output, PWM), watchdog	Two UARTs, 64-bit GPIO	13 internal, nine external		ARM7TDMI core, USB1.1 device controller	\$6.50
8- to 16-kbyte SRAM, up to 4-kbyte boot ROM, up to 512-kbyte flash	SRAM, DRAM, SDRAM, EDO-RAM, MASK ROM, flash		128 TQFP, 144 LQFP/LFBGA	Multifunction timer (auto reload, capture, compare-output, PWM), watchdog	One or two UARTs, SIO, 32- or 40-bit PIO	18 or 20 internal, five or nine external	Four or eight-channel, 10-bit	ARM7TDMI core, I ² C supported	\$5 to \$8
128- to 384-kbyte flash, 32- to 64-kbyte SRAM			81 LFBGA, LQFP	Two 32-bit, watchdog	UART, SPI, I ² C, USB, PCM/IOM, PIO	As many as 24, two to 16 external	Four-channel, 8-bit ADC, 8-bit DAC	Voice codec, CVSD, Bluetooth support	\$12 to \$15
	Yes		100 PQFP	VPU	Hardware baud-rate generation	Eight			License
Configurable	Optional		144LQFP		Configurable	Eight		Synthesizable core	License
16-kbyte SRAM, 82.9-kbits dual-port SRAM (128×18, 256×9, 512×4, 1024×2)	SDRAM, flash, SRAM, EPROM	32-bit entry TLB	516 PBGA, 1.27 mm pitch	Four 32-bit	One modem-control serial, one IrDA-compliant serial	Seven		2016 programmable-logic cells (equivalent to 75,000 ASIC gates)	\$60
32-kbyte SRAM	SRAM/ROM/Flash/SDRAM, 2× DMA channels	WinCE enabled	176 LQFP	Four 16-bitx PWM, WDT, RTC	Three 16550 UARTs, SPI, Microwire, TI's SSI, 64 PIOs	Six external		Color LCDC, advanced TFT support, vectored interrupt	\$16.70
80-kbyte dual ported SRAM	SRAM/ROM/flash/SDRAM/(CPU/LCDC) Sflash/SROM, 10 to 12 DMA channels	WinCE enabled	256/324 PBGA	Three 16-bit, real-time, up to two PWM, watchdog	Three UARTs, SPI, MicroWire, SSI, AC'97, 60 PIOs	Eight external, vectored	10-channel 10-bit ADC touch screen controller	Java JIT compiler, color LCDC, TFT support, MMC/SD, smart-card interface, DC-DC interface, device/host USB 1.1	\$29 to \$42

32-BIT MICROPROCESSORS (CONTINUED)

Company name	Device family or device	CPU frequency	Bus interface (address/data) (bits)	Instruction width (bits)	Operating voltages (V)	Typical power at maximum frequency	Power-down modes	DSP/multiplication hardware support (bits)	FPU	Caching
STMicroelectronics www.st.com Enter No. 353	STPC	66 to 133 MHz	64	32	3.3					
	ST40RA (SH-4 core)	150, 166, or 200 MHz	14/64 DDR SDRAM bus 26/32 peripheral bus 32 (multiplexed) PCI 66 MHz bus	16	1.8 or 3.3	980 mW	Three	64-bit FPU with vector operations	IEEE-754, single and double precision, 3-D vector and matrix, transcendental functions	8-kbyte instruction, 16-kbyte data, RAM/cache mode
SuperH www.superh.com Enter No. 354	SH4-202 core	266 MHz (worst case)	32 internal, 29 external, 8 to 1024 (definable), 64-bit request and response paths	16	1.2	180 mW	Sleep, standby, module standby, clock-domain frequency control	Four 32×32 floating-point multipliers, three 32 floating-point adders	IEEE-754, single and double precision, 3-D vector and matrix, transcendental functions	16-kbyte instruction, 32-kbyte data, two-way-set-associative, LRU, write-back/write-through selectable, RAM/cache mode
Tensilica www.tensilica.com Enter No. 355	Xtensa V	350 MHz	32, 64, 128 (configurable)	16/24	1.5 or 1.8, 2.5, 3.3	0.2 mW/MHz (0.13 micron)	Power-down, selective disable	User-customized DSP instructions or five Vectra DSP-coprocessor options/16×16, 32×32	Optional, IEEE-754 compatible	Configurable: 0- to 32-kbyte instruction/data, four-way-set-associative
Toshiba America Electronic Components www.toshiba.com Enter No. 356	TLCS 900/H1	8 to 40 MHz	24/16	8, 16, 32	3 to 3.6	30	Idle 2: 4.5 mA, idle 1: 2 mA, stop: 1 μA	16×16 to 32 (signed/unsigned)		
	TLCS900/H2	20 MHz	24/16	8, 16, 32	4.5 to 5.5	90	Run: 50 mA, idle: 5 mA, stop: 0.5 μA	16×16 to 32 (signed/unsigned)		
	TMPR-1940-CYAF	32 MHz	32, external: 8 or 16	16/32	2.7 to 3.6	165 mW (ROM)	Stop, sleep, slow	One-cycle MAC		
	TMPR-1940-FDBF	32 MHz	32, external: 8 or 16	16/32	2.7 to 3.6	280 mW	Stop, sleep, slow	One-cycle MAC		
	TMPR-3911BU 3911BxB	58.9 MHz	32	32	2.6/3.3	150 mW	Doze, sleep	One-cycle 32×32+64 MAC		4-kbyte instruction, 1-kbyte data, direct map, two-way-set-associative
	TMPR-3912AU-92 3912XB-92	92 MHz	32	32	3.3	360 mW	Doze, sleep	32×32+64 MAC		4-kbyte instruction, 1-kbyte data, LRU, two-way-set-associative
	TMPR-3922CU	129 MHz	32	32	2.7/3.3	500 mW	Doze, sleep	One-cycle 32×32+64 MAC		16-kbyte instruction, 8-kbyte data, LRU, two-way set associative
	TMPR-3927BF	133 MHz	32	32	2.5 or 3.3	1W	Reduced frequency, dose, halt	32×32+64		8-kbyte instruction, 4-kbyte data, LRU, two-way set associative
Transmeta Corp www.transmeta.com Enter No. 357	Crusoe TM5800 UTM5500	As much as 800 MHz	32	32	0.9 to 1.3	1W	Autohalt, quick start, deep sleep	Yes	Yes	L1: 64-kbyte instruction, 64-kbyte data, L2: 512-kbyte
Triscend www.triscend.com Enter No. 358	A7 configurable family	As much as 60 MHz	32, external: 20 to 32/8 to 32	16/32	2.5 or 2.5 to 3.3	1.65W	Power-down, selective disable	32×32+64 MAC/32×8, options available		8-kbyte unified cache
Xilinx www.xilinx.com Enter No. 359	MicroBlaze (soft CPU) PowerPC 405GP (Virtex-II Pro)	150 to more than 300 MHz	32 (Core-Connect)	32	1.5 to 3.3, depending on target FPGA	0.9 mW/MHz (V2Pro)		User definable DSP, two-cycle 32×32 multiply, 32×32 bit multiply/divide		16-kbyte instruction/data (V2Pro)

Memory	Memory controller	MMU	Package selection	Timers	Serial, parallel I/O	Interrupts	ADC/DAC	Additional features	Price (10,000)
	64-bit DRAM controller, 64-bit SDRAM UMA controller				PCI, ISA, EIDE, PCMCIA, I ² C, keyboard, mouse, USB			VGA, SVGA, TFT controller, video-input/output port	\$30 to \$38
RAM/cache mode, 8-kbyte RAM/data cache	64-bit SDRAM/DDR, flash, burst flash, SRAM, SDRAM, peripherals on peripheral bus	64-entry fully-associative UTLB; four-entry fully associative microITLB	372 PBGA	Three 32-bit	Two UARTs, 24 PIO	17 internal, four external + NMI		Five-channel DMA, RTC, JTAG, real-time trace	\$19.95 (166 MHz)
RAM/cache mode, 16-kbyte RAM/data cache	External (implementation dependent)	64-entry fully-associative UTLB; four-entry fully associative microITLB		Three channel 32-bit, watchdog, real-time with alarm and calendar functions	Full-duplex serial with 16-byte send/receive FIFOs, modem control, baud-rate generator	16 priority levels, four external cascadable IRLs, 128+ interrupts	Implementation dependent	SuperHyway VSI-compliant interconnect, UDI (JTAG), 1-kbyte debug RAM, AUD trace	License
Configurable: up to 128-kbyte ROM, up to 256-kbyte RAM		Optional		As many as three 32-bit		As many as 32			License
Up to 256-kbyte ROM, 10-kbyte RAM	SDRAM	Yes	100 LQFP, 144 LQFP	As many as eight 8-bit, one or two 16-bit, 22-bit watchdog, RTC,	As many as three UARTs, synchronous SIOs, SEI, CAN, IrDA, I ² C, as many as 70 PIOs	Nine CPU, 40 internal, four external, seven	Up to 12-levels channel, 10-bit	Four 32-bit register banks, eight micro-DMA channels, LCD controller	\$6 to \$8
Up to 512-kbyte ROM, 16-kbyte RAM	Yes		100 QFP, 160 QFP, 100 LQFP	As many as eight 8-bit, as many as four 16-bit, 22-bit watchdog	Two UARTs, synchronous SIOs, two SEI, CAN, as many as 70 PIO	18 internal, 10 external, seven levels	Up to 12-channel, 10-bit; two-channel, 8-bit DA converter	Four 32-bit register banks, eight micro-DMA channels, LCD controller	\$4.25 to \$7
256-kbyte mask ROM, 10-kbyte SRAM			100 LQFP	Four 16-bit, four 8-bit, watchdog	Four UARTs/SIOs, I ² C bus/SIO, 77 PIOs	12 external, NMI	Eight-channel, 10-bit		NA
512-kbyte flash, EEPROM, 16-kbyte SRAM			100 LQFP	Four 16-bit, four 8-bit, watchdog	Four UARTs/SIOs, I ² C bus/SIO, 77 PIOs	12 external, NMI	Eight-channel, 10-bit		NA
	SDRAM, DRAM, SRAM, ROM, flash	32-entry, 4-kbyte pages	176 LQFP, 177 BCSP	Real-time, watchdog	CHI, UART, IrDA, SPI, 39 PIOs	As many as 39 external		Codec interface (soft modem, voice recognition/synthesis)	\$10
	SDRAM, DRAM, SRAM, ROM, flash	32-entry, 4-kbyte pages	208 LQFP, 217 FBGA	Real-time, watchdog	CHI, UART, IrDA, SPI, 39 PIOs	As many as 39 external		Codec interface (soft modem, voice recognition/synthesis)	\$18
	SDRAM, DRAM (EDO), SRAM, ROM, flash	64-entry, page sizes: 4-kbyte to 4-Mbyte	208 LQFP	Two, watchdog	CHI, UART, IrDA, SPI, 48 PIOs	As many as 48 external		Companion chip TC6358TB	\$28
	SDRAM, SGRAM, DIMH flash, SMROM, SRAM, ROM	64-entry, page sizes: 4-kbyte to 4-Mbyte	240 PQFP	Three	Two UART, 16 PIOs	Six external		Debug-support unit	\$20
	64-bit DDR, SDR	Yes	474 BGA						\$85 to \$200
4-kbit×32-bit (upper-half optionally used as trace buffer)	8-, 16-, or 32-bit SRAM, flash, SDRAM, four DMA	Eight protected, cacheable, resizable memory regions	128 LQFP, 208 QFP, 280/484 BGA	Two 16-bit, 32-bit watchdog, can add timers	Two 16C550s, can add (HDLC, SPI, I ² C), 83 to 189 PIOs	15, special fast, can add more		As many as 40,000 on-chip programmable-logic gates, as many as 120 user-definable I/O pins	\$9.95 to \$19.95
72- to 3456-kbyte 216 to 10,006 kbit (V2Pro)	SDRAM, DDR, SRAM, Flash (soft IP)	Embedded MMU in V2Pro	Virtex/E, Spartan-II, Virtex-II, Virtex-II PRO	CoreConnect-enabled timer/counters, watchdog; PIT, FIT and WDT for V2Pro	CoreConnect-enabled UART, I ² C, GPIO, SPI, 16450/550, EMAC 10/100	CoreConnect-enabled controller		556 multipliers and 1200 I/O and 125,126 logic cells, chip-scope Pro for FPGA debugging	NA