



64-BIT MICROPROCESSORS

Company name	Device family or device	CPU frequency	Bus interface (address/data) (bits)	Instruction width (bits)	Operating voltages (V)	Typical power at maximum frequency	Power-down modes	DSP/multiplication hardware support (bits)	FPU	Caching
ArTile Microsystems www.artilemicro.com Enter No. 365	TX7901	200 to 266 MHz	32/64	2×64	1.5 core, 3.3 I/O	2.5W			Single/double precision	32-kbyte instruction/data
Broadcom Corp www.broadcom.com Enter No. 366	BCM1125 BCM1125H	400 MHz to 1 GHz	256 (internal bus)	64	1.2	4W (400 MHz) 5.5W (600 MHz)		8-bit MDMX	64-bit paired-single and MIPS-3D	L1: 32-kbyte instruction/data per core, L2: 256-kbyte shared, four-way set associative
	BCM1250	600 MHz to 1 GHz	256 (internal bus)	64	1.2	10W (800 MHz)		8-bit MDMX	64-bit paired-single and MIPS-3D	L1: 32-kbyte instruction/data per core, L2: 512-kbyte shared, four-way set associative
MIPS Technologies www.mips.com Enter No. 367	20Kc	600 MHz	64/64	64	1	2.5 mW/MHz (0.13 microns)	Wait	32×32, 32×64, 64×64	64-bit paired-single with MIPS-3D	32-kbyte instruction/data
	5Kc 5Kf	310 to 350 MHz	Definable	64	Process dependent	0.17 to 1 mW/MHz	Wait	32×32, 32×64, 64×64		0- to 64-kbyte instruction/data
NEC Electronics www.necel.com Enter No. 368	VR4121	168 MHz	32	32	2.5 core, 3.3 I/O	270 mW	Full speed, standby, suspend, hibernate			16- to 32-kbyte direct mapped instruction, 8-kbyte data
	VR4122	150 or 180 MHz	64, external: 32/16	16, 32	1.8/3.3	350 mW	Standby, suspend, hibernate			32-kbyte instruction, 16-kbyte data, direct mapped
	VR4131	More than 200 MHz	64, external: 32/16	16, 32	1.5 core, 3.3 I/O	220 mW	Standby, suspend, eXsuspend, hibernate	One clock 32×32+64 multiply-add instruction		16-kbyte instruction/data, two-way set associative
	VR4181	66 MHz	64, external: 32/16	16, 32	2.5 or 3.3	125 mW	Standby: 57 mW, suspend: 38 mW, hibernate: 16 mW			4-kbyte instruction/data
	VR4181A	131 MHz	Internal 64 bits, external 32, 16 bits	32 and 16	2.5 core, 3.3 I/O	250 mW	Standby: 100 mW maximum, suspend: 50 mW maximum, hibernate: 165 μW maximum			8-kbyte instruction/data, direct mapped
	VR4310	133 or 167 MHz	64, external: 32	32	3.3	1.2 to 2.5W				16-kbyte instruction, 8-kbyte data
	VR5000	200 or 250 MHz	64, external: 64	32	3.3	5W	Standby	MAC IEEE-754 compliant, 32×32 and 32×16 multiply	IEEE-754, 32 and 64/32-bit floating-point arithmetic and floating-point multiply	16-kbyte instruction, 8-kbyte data, two-way set associative
	VR5432	167 to 200 MHz	64, external: 32	32	2.5 core, 3.3 I/O	1.8W		MAC plus special instructions and ALUs, 32×32+64 MAC, barrel shift	IEEE-754, 64/32-bit floating-point arithmetic and floating-point multiply	32-kbyte instruction/data, two-way set associative

	Memory	Memory controller	MMU	Package selection	Timers	Serial, parallel I/O	Interrupts	ADC/DAC	Additional features	Price (10,000)
	Up to 1-Gbyte	133-MHz SDRAM, built-in ECC, aligned burst transaction	48 dual-entry	484 PBGA	Three 24-bit	Dual 32-bit/66-MHz PCI 2.1, dual UART, SPI, GPIO	As many as eight external		Dual-Ethernet MAC, dual-issue superscalar, synthesizable core, multimedia instructions	\$20
	12-kbyte trace buffer	64-bit DDR, SDRAM, 200-MHz DDR, ECC protected	64 dual-entry, 4-kbyte to 64-Mbyte page	899 BGA	Yes	32-bit/66-MHz PCI, two serial (synchronous or asynchronous), GPIO	Yes		Two 10/100/1000-Mbps MACs, HyperTransport, PCMCIA, JTAG, fully coherent	\$99 (400 MHz)
	12-kbyte trace buffer	Two 64-bit DDR, SDRAM, 200-MHz DDR, ECC protected	64 dual-entry, 4-kbyte to 64-Mbyte page	860 BGA	Yes	32-bit/66-MHz PCI, two serial (synchronous or asynchronous), GPIO	Yes		Three 10/100/1000 MACs, HyperTransport, PCMCIA, JTAG, fully coherent	\$419 (700 MHz)
			48 dual-entry TLB, eight-entry μ TLB, 4-kbyte to 16-Mbyte page						Full custom hard core, dual-issue, seven-stage pipeline	License
	Configurable	Optional	16, 32, or 48 dual-entry TLB with variable page size		Optional				Synthesizable core, coprocessor interface	License
		66 MHz	32 double-entry, fully associative TLB, 4-kbyte to 1-Gbyte page	224 FPBGA	Four 32-bit	115-kbps serial	Yes	Yes	Clock-generator unit	\$23
		ROM, synchronous 66-MHz DRAM, flash	32 double-entry TLB, 1- to 256-kbyte page	224 FBGA	Four 32-bit	115-kbps serial	Yes	Yes	Clock-generator unit	\$25 to \$30
		ROM, synchronous 100-MHz DRAM, flash	32 double-entry TLB, variable page size 1- to 256-kbyte, 32-bit addressing	224 FBPGA	Real-time	Two 16550-compatible, serial debug, synchronous three-line clock			Programmable clock management for each peripheral	\$25
		66-MHz, ROM, EDO DRAM, SDRAM, SROM, flash	32 double-entry TLB, variable page size 1- to 256-kbyte, 32-bit addressing	224 FBGA	Four 32-bit	115-kbps serial	Yes	Yes	Clock-generator unit	\$10 to \$15
		Memory controller for ROM, synchronous 66-MHz DRAM, and flash memory	32 double-entry TLB, variable page size 1- to 256-kbyte, 32-bit addressing	240 FBGA	Four 32-bit	1.5-Mbps serial I/O	Yes	Four-channel 10-bit ADC, 10-bit DAC	Clock-generator unit, ISA-bus-subset interface, USB host/slave interface	\$15 to \$20
		Use 4375 or third party	32 double-entry TLB, 4-kbyte to 16-Mbyte page	120 QFP	32-bit		Yes	Yes	Clock-generator unit, JTAG, sync interface	\$10 to \$15
		83/100 MHz	48 double-entry TLB, 4-kbyte to 16-Mbyte page	223 BPGA			Yes		Dual-issue superscalar, L2 cache interface	\$40 to \$50
		83/100 MHz	48 double-entry TLB, 4-kbyte to 1-Gbyte page	208 PQFP	Two 32-bit				Dual-issue superscalar, JTAG, N-Wire/N-Trace, 32-bit SysAD bus	\$20

64-BIT MICROPROCESSORS (CONTINUED)

Company name	Device family or device	CPU frequency	Bus interface (address/data) (bits)	Instruction width (bits)	Operating voltages (V)	Typical power at maximum frequency	Power-down modes	DSP/multiplication hardware support (bits)	FPU	Caching
	VR5500	300 to 400 MHz	64-bit internal and external with a 32-bit option	32	1.5 core, 3.3 I/O	1.5W		MAC with multiple floating-point units, 32×32 and 64×64 floating point, integer multiply, integer multiply-accumulate	IEEE-754, 32- and 64-bit floating-point arithmetic and floating-point multiply	32-kbyte instruction/data, two-way set associative, line locking plus four pending instructions and blocking plus instruction prefetch
	VR7701	400 MHz	64	32	1.5 core, 2.5 memory, 3.3 I/O	2W	Standby	MAC with multiple floating-point units	IEEE-754, 64/32-bit floating-point arithmetic and floating-point multiply	32-kbyte instruction/data, two-way set associative, line locking plus four pending instructions and blocking plus instruction prefetch
PMC-Sierra MIPS Processor Division www.pmc-sierra.com Enter No. 369	RM5200	250, 300, or 350 MHz	32/64	32	1.65, 1.8/2.5, 3.3	Less than 1W (400 MHz)	Standby	MAC/MAD/MADU, multiply (three-operand and cycle)	One- or two-cycle, single/double precision	32-kbyte instruction/data, two-way set associative
	RM7000	300, 350, 400, 450, 500, 550, or 600 MHz	64	32	1.8, 1.5, 1.2/3.3, 2.5, 1.5	4W (400 MHz)	Standby	MAD/MADU, multiply (three-operand and cycle)	Single/double precision	16-kbyte instruction/data, L2: 256-kbyte, four-way set associative, line locking, write back/through
	RM9000X2	1000 MHz	64/8, local bus: 8, 16, 32	32	1.2, 2.5, 3.3	5W		Yes	IEEE-754	16-kbyte instruction/data, L2: 256-kbyte four-way set associative
SandCraft www.sandcraft.com Enter No. 370	SR71010	600 to 800 MHz	64	32	1.2, 1.5/3.3	5W (600 MHz)		MAC instructions/single- and double-precision operations	IEEE-754-compatible, decoupled from integer pipeline	L1: 32-kbyte instruction/data, four-way set associative, L2: 512-kbyte, L3: 2- to 16-Mbyte
	SR71040	600 to 800 MHz	64	32	1.2/3.3	3W (600 MHz)		MAC instructions/single- and double-precision operations	IEEE-754-compatible, decoupled from integer pipeline	L1: 16-kbyte instruction/data, L2: 128-kbyte
Sun Microsystems www.sun.com/microelectronics Enter No. 371	Ultra-SPARC IIe series	400 or 500 MHz	64 with ECC, external: PCI 32	32	1.5/3.3	10W	Full, one-half, one-sixth frequency with SDRAM self-refresh	32×32, 64×64, 128×128	IEEE 754-1985 single/double precision, 1596.5-1992 quad precision	16-kbyte instruction/data, two-way set-associative, indexed/tagged, write-through, direct-mapped, L2: 256-kbyte
SuperH www.superh.com Enter No. 372	SH5-103 core	400 MHz (worst case)	32 or 64, 8 to 1024, separate 64-bit request and response paths	16 or 32	1.2	Less than 400 MHz	Economy, sleep, quick-wake-up standby, deep standby, module (peripheral) stop, clock-domain gearing	Two-, four-, and eight-way SIMD packed arithmetic in 64-bit registers, permute, shuffle, extract, conversion	IEEE-754, single and double precision, 3-D vector and matrix, transcendental functions	32-kbyte instruction/data, four-way set associative, LRU, write-back/write-through selectable, cache locking
Toshiba America Electronic Components www.toshiba.com Enter No. 373	TMPR-4927ATB	200 MHz	64, external: 20 to 28/8 to 32	32	1.5/3.3	1.2W	Halt	One-cycle 64×64 MAC	IEEE-754-compliant, single/double precision	32-kbyte instruction/data, four-way set associative, FIFO, lock
	TMPR-4955AF200	200, 300, or 333 MHz	32	32	1.5/3.3	450 or 600 mW	Halt, doze	One-cycle 64×64 MAC	IEEE-754-compliant, single/double precision	32-kbyte instruction/data, four-way set associative, FIFO, lock
	TMPR-4925XB, 4926XB	200 MHz	32, external: 20 to 28/8 to 32	32	1.5/3.3	0.9W	Halt, doze, reduced frequency	One-cycle 64×64 MAC	IEEE-754-compliant, single/double precision	16-kbyte instruction/data, four-way set associative, FIFO, lock

	Memory	Memory controller	MMU	Package selection	Timers	Serial, parallel I/O	Interrupts	ADC/DAC	Additional features	Price (10,000 unless otherwise noted)
		133 MHz	48 double-entry fully associative TLB, variable 4-kbyte to 1-Gbyte page	272 BGA	Two 32-bit timers for 11 events		6 bits of addressing enabled		Dual-issue superscalar, JTAG N-Wire/N-Trace, 32/64-bit SysAD bus, ×2 to ×5.5 clock modes	\$35 to \$42
		133-MHz DDR/SDRAM controller	48 double-entry fully associative TLB, variable 4-kbyte to 1-Gbyte page	500 PBGA	Two 32-bit timers for 11 events	Two-channel UART, clocked serial interface	6 bits of addressing			\$97
		48 dual entries map 96 pages (4-kbyte to 16-Mbyte)		128/208 QFP			Optional exception vector			\$15
			64 dual-entry TLB maps, 128 pages	256/304 BGA				10 external, NMI		\$100
	8-kbyte scratch RAM linear address mapping	DDR, SDRAM, 200-MHz DDR, DMA	64 dual-entries, 4-kbyte to 256-Mbyte page	656 SBGA				10 external, NMI, 256 levels, intra-CPU	CAN DMA packet header to L2 and put remainder into main memory	NA
			64 dual-entry TLB, 4- to 256-kbyte page	304 BGA				10 extended		\$100
			64 dual-entry TLB, 4- to 256-kbyte page	256 BGA				10 extended		\$50
		64-bit SDRAM interface, four DIMMs, up to 2-Gbyte	Dual 64-entry, 8- to 4096-kbyte page	Socketable 370 ceramic PGA	Two 63-bit	32-bit, 66-MHz, 3.3V PCI 2.1 compatible, four GPIO	As many as 48		Energy Star power management	\$145 to \$225
	Implementation dependent	Implementation dependent	64-entry fully associative UTLB, four-entry fully associate microTLB		Three channel 32-bit, watchdog, real time with alarm and calendar functions	Full-duplex serial with 16-byte send and receive FIFOs, modem control, baud-rate generator	As many as 64	Implementation dependent	SuperHyWay VSI compliant interconnect, SHdebug run-time control and trace on-chip debugging	License
		Four-channel SDRAM	48-entry fully associative TLB	420 TBGA	Three	PCI 2.1 32-bit/66-MHz, two serial, up to 16 PIO, ACLC	12 internal, six external		EJTAG debug	\$25
		Four-channel SDRAM, NAND Flash	48 double-entry TLB	160 QFP					EJTAG debug	\$15 to \$20
			48-entry fully associative TLB	256 PBGA	Three 32-bit, real time	PCI 2.2 32-bit/33-MHz, two serial, up to 32 PIO, SPI, ACLC, PCMCIA	21 internal, eight external		EJTAG debug	\$20