

Altera

THE EXCALIBUR FAMILY OF EMBEDDED-PROCESSOR FPGA devices includes an ARM922T processor subsystem to Altera's programmable-logic architecture, enabling complete SOPC (system-on-programmable-chip) designs. These ARM-based Excalibur FPGA devices allow stand-alone processor operation and FPGA programming of the device without the need to configure the entire chip. Designers can focus on the remaining logic and IP (intellectual-property) blocks required to complete SOPC designs and dynamically customize the design without worrying about the long lead-times and early specification commitments that you generally associate with an ASIC design flow. The Excalibur device family is well suited for both ASIC-prototyping quantities and low-to-moderate-volume production.

The Nios embedded processor is a configurable processor that supports all of Altera's look-up-table programmable-logic devices, including the high-performance Stratix device family. The Nios processor employs a pipelined RISC architecture, with a compiler-friendly instruction set that delivers a 33- to 125-MHz operating speed while executing most instructions in one clock cycle. The processor has a user-configurable 32- or 16-bit data path, with both variants using a 16-bit instruction size. Users may add to the processor's ALU as many as five custom instructions, including single-cycle, combinatorial, and multicycle operations. Each module supports a 32/16-bit A and B input, an 11-bit prefix, and direct access to external logic or memory. Nios includes several soft-core peripherals that connect to the processor using a bus-fabric architecture that allows multiple bus masters to operate simultaneously. The Nios processor includes a royalty-free, perpetual-development license for designs placed in Altera devices. ASIC and application-specific-standard-product licenses are available.

Development support: GNUPro is the fee-free, standard compiler package that supports development for both the Excalibur devices and Nios soft-core processors. For users who prefer ARM tools, Altera provides ARM's ADS (ARM Developer Suite) Lite for a nominal fee. ADS Lite covers the ARM922T processor that the Excalibur device family uses. Customers can evaluate Embedded Linux and other operating systems from Wind River Systems, Accelerated Technology, and Enea/OSE with the Excalibur Solutions Pack, which Altera ships with each Excalibur development kit. Debugging and tracing options are also available from Agilent, American Arium, ARM, Lauterbach, EPI, and Mentor.

The GNUPro tool kit from Red Hat is part of the Nios development kit and includes a compiler, an assembler, a debugger, and several utilities. The Nios Development Kit includes several soft-core peripherals, including a UART, timer, PIO, SPI, SSRAM, SDRAM, DMA, PWM, and IDE. Additional development kits support uClinux, Ethernet, and on-chip debugging with tracing. The development software automatically generates assembly and C-language macros. Developers can use the SOPC builder front-end and Quartus II back-end development tools to generate Nios-based systems. SOPC Builder automates integrating system components, such as IP blocks, memories, interfaces, and microprocessors, and generates the necessary bus logic, including arbitration, to connect any number of peripherals to the Nios CPU. Operating-system support includes uClinux, Nucleus Plus by ATI, NORTi by MiSPO, and KROS by Shugyo Design. Other third-party tools are available from Mentor Graphics, Sophia Systems, Viosoft, and Microtronix Datacom.

Analog Devices

THE ADUC8XX MICROCONVERTERS INTEGRATE an 8052 processor core with multichannel SAR or sigma-delta ADCs, dual 12-bit DACs, and 8- to 62-kbyte flash memory. These devices deliver self-calibrating data-acquisition precision of 16 to 24 bits. They accept low-level signals directly from a transducer. Most of the 8-kbyte flash devices can upgrade to 100% software-

hardware-compatible 62-kbyte devices.

Development support: The QuickStart Development System, incorporating an assembler, an in-circuit serial-port downloader, a serial port debugger, and analog-performance-analysis tools, supports the ADuC8xx devices. You can upgrade QuickStart to a full in-circuit, single-pin, nonintrusive, emulation system supporting assembly and C-Source debugging. The QuickStart development kit contains an evaluation board, sample microconverter chips, support cables and a power supply, and a software-development CD-ROM.

ARC

THE ARCTANGENT-A4 MICROPROCESSOR IS A synthesizable, user-customizable processor core for embedded ASIC, SOC (system-on-chip), and FPGA integration. It is a 32-bit RISC architecture with optional DSP extensions, and its base-case processor requires as few as 14,000 gates. Developers can configure and extend processor resources, including the instruction set, register files, I/O interfaces, interrupts, instruction/data caches, and condition codes. Special instruction sets include saturating ADD/SUB, NORMalize (find first bit), MIN/MAX, two 32×32-bit multipliers, and two 32-bit barrel-shifter/rotator blocks.

Developers can customize the processor with the ARChitect configuration tool and add custom logic in HDL. The synthesizable ARctangent-A4 processor and peripheral IP (intellectual property) supplied by ARC are portable to almost any process technology or foundry. The ARChitect tool generates RTL files and scripts for industry-standard logic-synthesis tools. Integrated peripherals include a 32-bit timer, a UART, a 10/100-Mbps Ethernet MAC (media-access controller), and USB.

The ARctangent-A5 microprocessor is a synthesizable, user-customizable, 32-bit RISC core for ASIC and SOC products. Developers can optimize the ARctangent-A5 processor for various criteria, including computational performance, signal processing, I/O throughput, power consumption, silicon area, and cost. The instruction set, register file, condition codes, caches, buses, and other architectural features are user-configurable and extendable. The synthesizable ARctangent-A5 processor and peripheral IP supplied by ARC are portable to almost any process technology or foundry.

At the heart of the ARctangent-A5 processor is a 32-bit four-stage pipeline RISC architecture and the mixed 16/32-bit ARCompact instruction set. The ARCompact ISA reduces code size and maximizes the instruction-expansion space. You can mix 16-bit encodings of frequently occurring instructions with the 32-bit instructions with no overhead or penalty. The instruction set is orthogonal, supporting ALU and load/store operations on all general-purpose registers. Most instructions operate in a single cycle and have optional conditional execution.

The ARctangent-A5 contains a dual 16-bit MAC (multiply-accumulate), dual 16-bit multiply-subtract, saturating addition/subtraction, division assist, saturate and round instructions, absolute-value calculation, and normalize, making it a configurable RISC/DSP core. It supports multiple CPU interfaces, allowing it to concurrently load, store, and process data using enhanced XY memory that supports eight pointers.

Development support: The ARC SOC development platform includes the ARChitect processor-configuration tool and other utilities for hardware development. Software-development tools include the MetaWare High C/C++ compiler, an assembler, a linker, a profiler, the SeeCode debugger, and an instruction-set simulator. Miscellaneous tools include the ARC Signal Visualization Tool for DSP development with Matlab, cycle-accurate simulators, and real-time trace debugging.

ARM

THE ARM7 FAMILY IS A RANGE OF low-power 32-bit RISC microprocessor cores optimized for cost- and power-sensitive consumer applications. Offering as many as 130 Dhrystone 2.1MIPS, the ARM7 family incorporates the Thumb 16-bit instruction set, enabling 32-bit performance at an 8/16-bit system cost. The family comprises the ARM7TDMI, ARM7TDMI-S, and ARM7EJ-S processor cores and the ARM720T cached-processor macrocell.

The ARM Thumb architectural extension, which ARM denotes with a "T" extension, is primarily a 16-bit subset of the 32-bit instruction set. During execution, the Thumb module, residing within the instruction pipeline, transparently decompresses the 16-bit instructions back to 32-bit instructions with no performance loss. The Thumb module adds about 6% to the core's die size but increases code density and avoids the memory requirements of using only 32-bit fixed-length instructions.

Cores with the "S" extension are synthesizable macrocells that allow configurability and tight coupling of the ARM processor core with SRAM, instruction and data caches, a write buffer, and an AMBA AHB (advanced-microprocessor-bus-architecture advanced-high-performance-bus) interface. Cores with the "E" extension include signal-processing extensions to the ARM instruction set for applications that would benefit from a mix of DSP and microcontroller performance. The DSP extensions include single-cycle 16×16 - and 32×16 -bit MAC (multiply-accumulate) implementations and zero-overhead-saturation extensions of arithmetic instructions, for use in the design of stable control loops and bit-exact algorithms. New instructions include the ability to load and store pairs of registers with a wider range of addressing modes and a new CLZ instruction that improves normalization in arithmetic operations and division performance.

ARM built the ARM9 family around the ARM9TDMI processor core. It incorporates the 16-bit Thumb instruction set, which improves code density by as much as 35%. The ARM9 Thumb family includes the ARM920T, ARM922T, and ARM940T cached-processor macrocells. The ARM9E devices are DSP-enhanced 32-bit RISC processors, suiting applications that require a mix of DSP and microcontroller performance. The family includes the ARM926EJ-S, ARM946E-S, and ARM966E-S processor macrocells. They include signal-processing extensions to enhance 16-bit fixed-point performance using a single-cycle 32×16 MAC unit, and they implement the 16-bit Thumb instruction for heavier code density. The ARM926EJ-S core includes ARM Jazelle technology to enable direct execution of Java byte codes in hardware.

The ARM10E family features new power-saving modes, a 64-bit load-store micro-architecture, an IEEE754-compatible floating-point coprocessor with vector operations, easy system integration, and a complete set of hardware- and software-development tools. The ARM10E family comprises the ARM1020E and ARM1022E processor cores, which have 32- or 16-kbyte caches, respectively, to address silicon-area and cost requirements. It also includes the ARM1026EJ-S, a fully synthesizable processor featuring ARM Jazelle technology for Java acceleration and extensive 64-bit internal busing.

The SecurCore family supports development for smart-card and secure ICs. In addition to very small die size, low power consumption, code density, and performance, the SecurCore family incorporates special security features to resist power and timing attacks. The ARM SecurCore family includes the SC100, SC110, SC200, and SC210 cores. The SecurCore family also offers Jazelle acceleration technology for the rapidly growing Java Card platform. The SecurCore family of microprocessors features a new secure processor design and an anti-counterfeiting methodology that helps resist invasion at the hardware and software levels, including physical tampering through reverse-engineering of the layout, power, or timing analysis or by directly probing the processor-chip surface. A key feature for security-sensitive applications is a "one-way information flow," which permits developers to customize cores by adding a range of security features known only to the card issuer or developer.

Development support: ARM designs microprocessor cores and macrocells for its licensees in a variety of flavors with considerations for low power. The ARM7, ARM9, ARM9E, ARM10E, and SecurCore families are base configurations; all implement the ARM instruction set for software compatibility across the full range of processor cores. ARM processors work with many leading third-party RTOS and tools vendors. ARM's tools provide an integrated development environment that includes software-development tools, code-generation tools and debuggers, and system-development and evaluation boards. ARM-development tools support all the cores in the ARM family and provide forward and backward compatibility. The ARM and Thumb compilers deliver optimized code for the higher code density and faster application code for ARM cores.

The board-level Integrator supports the integration of software and hardware IP (intellectual property), such as ARM's PrimeCell peripherals and associated drivers. The Evaluator-7T introduces the ARM family for new customers and students who want to acquaint themselves with and evaluate an ARM CPU and its software tools. The Evaluator-7T supports the full range of ARM7 instructions, including Thumb instructions, and can operate at a maximum speed of 50 MHz.

ARM debugging tools include the ICE (in-circuit emulator) tools Multi-ICE and MultiTrace, and the on-chip-debugging facilities EmbeddedICE and ETM (Embedded Trace Macrocell). MultiTrace is a trace-port analyzer that passively collects information from ARM-core-based designs that include an ETM. The ETM monitors the ARM instruction and data buses at full core speeds, using the MultiTrace analyzer to buffer the collected information before transmission to the trace-debugging tools.

Multi-ICE is JTAG-based and supports all ARM-core-based devices that include the Embedded-ICE logic. JTAG emulation allows users to start and stop the core via the connected debugger software. Users can then examine and modify registers and memory, and set breakpoints and watchpoints. Multi-ICE also provides support for downloading code, tracing, and real-time debugging with RealMonitor.

The ARM RealView Debugger is a leading component of ARM's new RealView development option. It delivers multicore-mixed-architecture debugging and OS awareness of applications for ARM-core-based designs. EmbeddedICE is a JTAG-based debugging environment that provides the interface between ARM's source-level symbolic debugger, ARMsds, and an ARM microprocessor embedded within any ASIC. The ARMsds debugger is available for PC-compatible and Sun workstation platforms. EmbeddedICE provides real-time address and data-dependant breakpoints; single stepping; full access and control of the ARM CPU; full access to the ASIC system, including full memory access (read and write); and full I/O system access (read and write). EmbeddedICE also allows the embedded microprocessor to access host-system peripherals, such as screen display, keyboard input, and disk-drive storage.

ARM offers cycle-accurate behavioral models for ARM 32-bit RISC processor cores. Most models are either available from ARM Partners or incorporated into ARM support packages from leading EDA-tool vendors. Design Signoff Models, with full timing capability, are an exception, as ARM offers limited direct availability.

The ADS (ARM Developer Suite) version 1.2 supports Windows-based software development for all ARM cores and processors, including Jazelle, StrongARM, and Intel Xscale devices. The suite includes compilers for C and Embedded C++, an assembler, and a linker for the ARM and Thumb instruction sets. The suite also includes a GUI debugger, instruction-set simulators, ROM-based debugging tools (ARM Firmware Suite), online documentation, an applications library, and real-time debugging and tracing support. Metrowerk's CodeWarrior Integrated Development Environment (PC-version only) supports ARM development. Both the integrator systems and the ARM Developer Suite include the ARM Firmware Suite v1.3. The suite packages low-level routines and libraries to help developers rapidly bring up applications

and operating systems on ARM-based development platforms.

ArTile Microsystems

ARTILE MICROSYSTEMS BASES THE Tx79xx family of processors on the MIPS 64-bit RISC architecture. The family includes special multimedia instructions and integrated MMUs and FPUs as well as standard products, and it's available in custom SOC (system-on-chip) configurations to integrate custom IP (intellectual-property), peripherals, and system interfaces. The TX7901 is a six-stage superscalar pipeline, dual-issue MIPS64 processor targeting multimedia/networking/printer applications by supporting 128-bit multimedia instructions.

Development support: ArTile offers reference platforms for its Tx79xx MIPS processors. Several RTOS environments, including Linux, VxWorks, and QNX, support these platforms, whose key features include ATX form factor and support for ATX power supply, four PCI slots, dual serial ports, dual SDRAM sockets, a dual Ethernet MAC (media-access controller), and a PHY/transformer. Cygnus tools from RedHat include the Gnu tools, GDB (Gnu debugger) and GCC (Gnu C compiler), to support development for Tx79xx processors. The processors support PC-tracing and debugging. ArTile offers a debugging-monitor program and drivers for all on-chip peripherals.

Atmel

ATMEL'S AT94K FPSLIC IS A FAMILY of programmable systems-on-chips that integrates a more-than-20-MIPS AVR RISC microcontroller and hardware multiplier with 5000 to 40,000 gates of FPGA. These devices include a 36-kbyte-maximum block of selectable instruction code/data SRAM and an industry-standard two-wire serial interface. The on-chip 8-bit RISC AVR processor has 16-bit instruction words, 8-bit data words, and the ability to do 32-bit arithmetic.

The devices include 129 16-bit fixed-length instructions, optimized so that single instructions can cover 90% of all microcontroller-unit operations. A two-stage pipeline and separate addresses for load and store operations enable single-cycle instruction execution, and 32 8-bit registers allow the CPU to simultaneously access multiple data, eliminating the need for most data-transfer operations and enabling smaller code sizes. FPSLIC's on-chip FPGA can accelerate digital filters; implement FIFOs that interface between two systems; and create custom peripherals, such as UARTs, standard or proprietary interfaces to DMA controllers, DRAM, or application-specific standard products used for SPI, endian converters, and serial-to-parallel converters.

Development support: The System Designer codesign environment integrates a code-development environment (a compiler, debugger, and instruction-set simulator) with a suite of FPGA design tools that includes automatic placement and routing, floorplanning, interactive timing analysis, and timing-driven design. The co-verification environment allows you to concurrently verify the hardware and software portions of the design within a unified environment and provides full visibility into the processor's program counter, memory, registers, peripherals, and FPGA performance at every stage during the HDL simulation. System Designer's HDL Planner module automates the FPGA design for designers who are unfamiliar with HDL design. The tool automatically generates syntactically correct Verilog or VHDL from point-and-click component generators.

The FPSLIC Starter Kit is available with a reconfigurable FPSLIC device, a prototype board, cables, a user manual, and a four-month complete FPSLIC-designer software license. Reference designs with boards are available for embedded Ethernet and motion-control applications. A low-cost FPSLIC daughterboard allows any AVR development kit to support

FPSLIC development.

Broadcom

BROADCOM BASES ITS SiBYTE FAMILY of integrated processors on the MIPS64 ISA (Instruction Set Architecture). The BCM1250 is an intelligent CMP (on-chip multiprocessor system) comprising two Broadcom SB-1 MIPS64 CPUs, scalable from 600 MHz to 1GHz, a shared 512-kbyte L2 cache, a DDR memory controller, and integrated I/O. All major blocks of the processor connect via the ZBbus, a high-speed, split-transaction multiprocessor bus. The bus implements the standard MESI (modified, exclusive, shared, invalid) protocol to ensure coherency among the two CPUs, the L2 cache, the I/O agents, and memory.

To support higher data rates, or in cases that do not require Ethernet protocol processing, the three Gigabit Ethernet MACs (media-access controller) can act as either three 8-bit or two 16-bit packet FIFOs. HyperTransport I/O fabric and a 32-bit PCI (rev 2.2) local bus provide the high-speed I/O. To support low-chip-count systems, the BCM1250 also includes a configurable generic bus that allows glueless connection of a boot ROM or flash memory and simple I/O peripherals. The system can run in big- or little-endian mode.

Residing within the BCM112x line, the BCM1125H and BCM1125 are integrated, single-core processors that feature the SiByte SB-1 64-bit MIPS CPU. Both products integrate an on-chip 256-kbyte L2 cache, a DDR memory controller that supports 8 Gbytes of memory, and a variety of peripherals. The memory controller can use standard DDR SDRAM or FCRAM and provides 25-Gbps of peak memory bandwidth. The two 10/100/1000 Ethernet MACs are optionally configurable to act as one 16-bit or two 8-bit FIFO interfaces. The ZBbus connects all functional blocks of the processor. Both processors are software-compatible with the BCM1250 and share the same development and modeling tools, firmware, and operating systems.

Development support: The standard GNU tool chain provides support for development. Support for operating systems includes VxWorks, Linux, and NetBSD. Corelis provides third-party debugging support. Evaluation boards are available with tools, firmware, and software drivers.

Cybernetic Micro Systems

AT THE CORE OF THE P-51 IS AN 8051 that includes all 8051 ports, registers, instructions, and an additional 16-bit square-root function, which resides in its special-function-register file. The 100-pin package also includes dedicated I/O and handshaking signals for a host controller or ISA/PC-104 interface. An internal 4-kbyte dual-port RAM interfaces between the host side and the peripheral 8051 side. Embedded applications use the P-51 as a peripheral, and the host downloads code to the internal 8-kbyte code RAM at reset.

The general-purpose-peripheral 8051-based P51 retains all 8052 features and addresses an (E)ISA/PC104 bus for connection to a host. Power-up resets the P51, and it remains reset while the host processor writes 8051 instructions directly into the P51's code RAM. These instructions begin executing when the host releases the P51 from reset. The ISA/PC104 interface enables the P51 to serve as a peripheral to almost any microprocessor, including an 8051.

Development support: Software development for the P-51 relies on standard 8051 development tools, such as American Raisonance C-compilers and 8051-compatible cross-compilers. The 8051 undefined operating code, 0A5h, is a breakpoint instruction for the P51 and allows the host to single-step the peripheral 8051. The built-in debugging features (breakpoints and single-stepping) allow in-circuit code development without an ICE (in-circuit emu-

lator).

Cygnal Integrated Products

CYGNAL'S C8051FXXX DEVICES ARE INTEGRATED, 8-bit mixed-signal microcontrollers that are 100%-compatible with the standard 8051 instruction set. The 8051 code-compatible CPU features a high-speed, pipelined architecture capable of 25-MIPS peak throughput. You can program the onboard, in-system-programmable flash memory in 512-byte sectors for both program storage and nonvolatile, user-data storage. User software manages the power to each chip subsystem. The onboard JTAG-based debugger uses no on-chip resources, providing nonintrusive, full-speed, in-circuit emulation using the production processor installed in the final application. This debugging system supports inspection and modification of memory and registers, setting breakpoints, watch points, single-stepping, and run and halt commands.

Development support: Every chip has built-in JTAG-debugging resources supporting single-stepping, memory inspection and modification, hardware breakpoints, and other functions. The \$99 to \$129 development kit includes a target board; a serial adapter; a power supply and cables; and the Cygnal IDE editor, assembler, and debugger, which integrates seamlessly with 8051 C compilers.

Cypress MicroSystems

DESIGNED FOR FLEXIBILITY, THE PSoC (Programmable System on Chip) microcontroller family integrates a fast 8-bit CPU, 8 to 16 kbytes of flash memory, SRAM, and programmable arrays of analog- and digital-system functions known as PSoC blocks. By selecting a PSoC device with the chosen combination of memory, pins, and PSoC Blocks, designers can replace thousands of fixed-function microcontrollers with a software-configurable device for many applications. PSoC devices can dynamically switch the analog and digital blocks between configurations during runtime to perform multiple functions.

Development support: Development for all PSoC microcontroller-unit devices starts within the free PSoC Designer software tool set. Using this GUI-based software suite, designers can program and reprogram chips with a few mouse clicks, by selecting the peripheral "building blocks" that best fit their applications. After a user selects the desired peripheral functions, the software automatically generates the register-bit settings to implement the peripheral set, as well as the application-programming interfaces and interrupt-service routines. The tool set also includes a full-function, low-cost emulator that features full-speed operation, complex breakpoints, and tracing capability.

Dallas Semiconductor

MAXIM/DALLAS SEMICONDUCTOR'S 8051-COMPATIBLE microcontrollers are available as 8051 drop-in, security, networking, and mixed-signal device families. These processors achieve a 12-to-one increase in instruction-set efficiency over standard 8051 devices. The 8051 drop-ins are fully pin- and code-compatible with traditional industry-standard 8051s. Additional features include dual data pointers, two serial ports, clock dividers, watchdog timers, EMI reduction, and power management. Maxim/Dallas Semiconductor offers these parts in Flash, EPROM, custom-mask-ROM, and ROMless versions.

The secure microcontroller products target applications that require strong protection of secret or proprietary information, such as electronic banking, financial transactions, and pay-TV-access control. These products offer security ranging from moderate user-selectable encryption keys to state-of-the-art encryption algorithms, such as DES3 (triple Digital Encryption

Standard) and PKI (Public Key Infrastructure).

The network family of microcontrollers target applications that connect embedded systems to multitiered networks. These microcontrollers bridge the Internet to RS-232-, SPI-, CAN (controller-area-network)-, 1-Wire-net-, IRDA-, 802.11-, and Bluetooth-connected devices. In addition to protocol bridging, the microcontrollers have resources for local closed-loop control that you can modify remotely via the network. You can run the TINI (Tiny InterNet Interfaces) platform on top of the DS80C390/400 microcontroller, so that the engineer concerned with device communication need not become an expert on TCP/IP network stacks and can focus on local-control challenges. Devices with these microcontrollers can modify preferences from a remote computer browsing the Internet.

Maxim/Dallas Semiconductor's mixed-signal family provides interfaces to the real world of analog signals with the high-precision, digital world of the microcontroller. Containing ADCs, DACs, and PWMs of varying resolutions and precisions, these devices target a variety of applications.

Development support: Hardware- and software-development tools are available through third-party suppliers to support development for all Maxim/Dallas Semiconductor microcontroller products. Full in-circuit emulators and prototype/development boards, as well as compilers, assemblers, linkers, and debuggers with full GUI interfaces, are also available.

Fujitsu Microelectronics America

FUJITSU SUPPORTS A RANGE OF APPLICATIONS WITH 8-, 16-, and 32-bit microcontroller families. The F2MC 8L microcontroller family offers a range of peripheral functions, memory sizes, and options. More than 30 device series are available, incorporating features such as ADCs and DACs, LCD and VFD (vacuum-fluorescent-display) drivers, I²C and UART interfaces, and ac and stepper-motor drivers. Each series offers 4 to 60 kbytes of mask ROM and 128 bytes to 18 kbytes of SRAM. All series offer a choice of mask-ROM sizes, and at least one member offers a one-time-programmable EPROM. The architecture includes an 8-bit CPU core; two 16-bit accumulators; seven dedicated 16-bit registers; and 32 register banks, each comprising eight 8-bit registers. Typical applications include metering, motion control, domestic appliances, automotive applications, and feature phones. The series offers a large memory space that contains an I/O area, a RAM area, a ROM area, an external area, general-purpose registers, and a vector table. In addition to 10 addressing modes, the series has special instructions for jumping, moving, multiplication, division, and subroutine calls. It also has bit-manipulation instructions for bit set and clear.

Available in three variants, Fujitsu's F2MC16L, LX, and F series 16-bit CPU cores feature bit, nibble, byte, word, long-word data types, and 23 addressing modes. The instruction set supports a 16-Mbyte address range using bank- or linear-addressing modes. On-chip registers, such as user and system-stack pointers, together with their supporting instructions, provide advanced support to real-time operating systems. All of the F2MC-16LX series and one of the F2MC16L series offer at least one device that has flash ROM as the user-programmable memory. Available block sizes are 64, 128, 256, or 384 kbytes divided into separately erasable and protectable sectors supporting a minimum of 10,000 erase cycles. The 5 and 3V devices require no second programming voltage. Special instructions include support for enhanced high-level languages and multitasking, enhanced pointer indirection, and barrel-shift operations.

Fujitsu's FR series RISC architecture is a 32-bit microprocessor core for control systems in high-performance automotive, consumer, and telecom applications. The processor executes the 16-bit instructions in one cycle and supports half-word external-memory and instruction-cache widths and double instruction fetches each bus cycle. The CPU employs a five-

stage pipeline and 32×32-bit multiplier with a barrel shifter and a bit-search unit that finds the first zero, one, or change in a data word. The general-purpose user-logic bus provides access to the on-chip flash ROM and CAN (controller-area-network) interfaces.

Development support: Fujitsu Microelectronics America and Fujitsu Limited provide a range of development tools and software support for all of Fujitsu microcontrollers. Third-party-partner Source Electronics Corporation provides programming, labeling, taping/reeling, and technical support.

Hitachi

HITACHI'S H8 TINY SERIES OF MICROCONTROLLERS offers 16-bit performance at 8-bit cost levels. Devices target cost-sensitive, space-constrained designs that require moderately high integration, such as appliances, white goods, HVAC equipment, power meters, low-end motor controllers, test instruments, and personal-information devices. The H8 Tiny microcontrollers integrate as much as 56 kbytes of single-voltage in-circuit-programmable flash memory or mask ROM, and include as much as 4 kbytes of RAM and a basic set of peripheral functions. The H8 families of devices support three modes to program the on-chip flash memory. In PROM mode, a high-speed gang programmer programs the flash memory. In Boot mode, a standard RS-232 serial port supports flash programming. In User Programming mode, application software running on the microcontroller writes and erases the flash memory.

The H8/300H family of microcontrollers comprises 16-bit devices integrated around the Hitachi H8/300H CPU core. They have a 16-Mbyte linear address space and 16 multipurpose registers. These microcontrollers operate at 25 MHz with an 80-nsec instruction-execution speed, and they are backward-compatible with chips in the H8/300 series. Hitachi's H8S 16-bit microcontrollers target systems to 33 MHz that require power efficiency. Nine power-down modes are available to help optimize system-power consumption. The microcontrollers support a 16-Mbyte memory-address space and include a range of high-function peripherals. H8S series devices have large on-chip F-ZTAT flash memory or as much as 512 kbytes of masked ROM and as much as 32 kbytes of SRAM.

The SH-2 microcontrollers offer moderate performance with low power consumption. The on-chip integrated peripherals include timers that simplify motor-control and industrial equipment designs. One microcontroller unit in the SH-2 series, the SH7047F, targets three-phase dc brushless motor-control applications by integrating 256-kbytes of flash, a CAN (controller-area-network) 2.0B port, three serial channels, and several 16-bit timers. For embedded systems that require external memory, the SH-2 series integrates a bus-state controller that enables a glueless interface to DRAM and SRAM. SH-DSP processors are RISC/DSP devices that combine an SH-2 RISC CPU and a 16-bit integer DSP unit into a multitasking core that uses three buses, a 4-kbyte cache, and 16 kbytes of X/Y RAM to maximize throughput. The devices execute RISC and DSP instructions from a single instruction stream. Versions have as much as 256 kbytes of on-chip flash, a USB, and an Ethernet MAC (media-access controller).

The SH-3 family of 32-bit RISC microprocessors integrates a 16-kbyte cache, 32-bit external bus, MMU, 32-bit MAC, barrel shifter, real-time clock, and UBC (user break controller). They are upward-code-compatible with SH-2 family chips. Some versions have a PLL; a JTAG SDI (serial debugging interface); and serial, PCMCIA, SmartCard, and IrDA interfaces. The SH3-DSP family combines a SH-3 RISC processor and a 16-bit integer DSP unit into a multitasking core with a four-bus structure, 16-kbyte cache, and 16 kbytes of X/Y RAM. Multichip modules use about 60% less board space by combining an SH-3 or SH3-DSP processor and as much as 32 Mbytes of SDRAM.

The SH-4 family comprises a range of integrated, two-issue superscalar floating-point

RISC microprocessors for high-performance embedded applications. They have a 16-byte data cache, 8-kbyte instruction cache, 64-bit external bus, 32-bit MAC and MMU, as well as an FPU with a 128-bit vector graphics engine optimized for 3-D graphics that can process as many as 7 million polygons per second. The chips' 3-D graphics capability and 120-MHz, 64-bit external bus deliver high data throughput for workstation-class performance.

Development support: Hitachi and third-party vendors, such as RedHat, Green Hills, and Microsoft, support software development with project builders, C/C++ compilers, assemblers, linkers, librarians, simulators, and debuggers. Operating-system support includes Microsoft's Windows CE, Wind River's VxWorks, ATI's Nucleus+, QSSL's QNX/Neutrino, Microware's OS9, Lineo's Linux, and CMX's CMX-RTX. Several debugging emulators support access to the on-chip-debugging features, and may support complex hardware breakpoints and a trace buffer with a maximum capacity of 32k cycles.

Evaluation design kits are available for evaluating these devices. Each kit consists of the appropriate development board with as much as 512 kbytes of on-chip flash memory and as much as 32 kbytes of on-chip SRAM, a generic serial cable, a power supply, and a 30-day trial version of Hitachi Embedded Workshop software, which includes the Hitachi Debugging Interface. The Hitachi Embedded Workshop code-development environment includes an integrated editor, C compiler, assembler, linker, librarian, and simulator; it also provides project generation, tools configuration, version control, and graphical analysis. The modular graphical Hitachi Debugging Interface allows full-control target-system features for debugging in C and assembly.

Improv Systems

IMPROV SYSTEM'S JAZZ PROCESSOR USES a VLIW (very-long-instruction-word) architecture comprising a mix of heterogeneously configured task engines, on-chip data and instruction memory, I/O modules, and the QBus global bus for on-chip task and control communications among processors. System designers can tailor each task engine to match the computational needs of specific tasks by adding or removing execution units. A task engine contains as many as 16 single-cycle integer-computation units from a collection of functional blocks that include ALUs, multiply-accumulate units, shifters, counters, and application-specific units. Designers can create task engines for 32- or 16-bit data paths and can add custom units and instructions using the Jazz PSA Composer. Memory-interface units connect the processor to shared- and private-memory blocks and I/O modules. Each memory unit has a 32-bit data path and can address 64 kbytes of data memory as word, half-word, and byte-wide read/write operations.

Users can incorporate specialized gate-level descriptions within the data path of the Jazz programmable processor and extend the programming environment to support these descriptions as special instructions. The Jazz Processor can act as an integrated peripheral to other host-oriented microprocessor options, such as ARM and MIPS, extending their functions for application-specific requirements.

Development support: The Jazz PSA Tool Suite provides an integrated development environment with advanced debugging, compilation, and analysis capabilities to support production-code development for Jazz PSA Platforms. A compilation system manages application-wide partitioning and allocation, coupled with advanced task optimization and code generation.

Infineon Technologies

THE 15 DEVICES IN THE C500 MICROCONTROLLER family are compatible in architecture and

software with the standard 8051 microcontroller family. Although they maintain all of the architectural and operational characteristics of the SAB 80C52/80C32, C500 microcontrollers differ in the number and complexity of their peripheral units, depending on the application they support. The C500 architecture contains a set of eight 16-bit registers to store data pointers, but the instruction set allows for handling of just one 16-bit data pointer (comprising two 8-bit pointers). This arrangement reduces code size while speeding execution of external accesses, because you need just one instruction—select a new data pointer—to execute a change of access.

The C166 microcontroller family offers varying performance levels (reaching 40-MHz clock speeds), peripheral support, and programmability. With a four- or five-stage instruction pipeline, all C166 devices execute the same basic instruction set based on a cross-licensed architecture that Infineon co-developed with STMicroelectronics. Target applications include industrial control, automotive electronics, PC-peripheral control, and consumer-electronics devices. In addition to C166-family devices, the C166S synthesizable core is available for SOC (system-on-chip) design as a core in the Synopsys DesignWare Star IP (intellectual-property) program.

The unified microcomputer/DSP TriCore architecture combines microcontroller and DSP functions, such as bit-manipulation capabilities in one instruction set, and operates as a single multitasking engine with fast context switching. In addition to TriCore-based devices, the TriCore-based TC-1MP microprocessor is available as a hardcore and fully synthesizable macro for SOC integration. The TC-1MP supports one to four coprocessors, tightly coupled to core, to implement custom or application-specific instructions. Combining a classic load/store RISC architecture with Harvard math capability, the superscalar TriCore core has three four-stage pipelines, enabling simultaneous execution of as many as three instructions and a maximum execution rate of seven operations in one clock cycle. You can freely intermix 16- and 32-bit instructions without degrading code-execution efficiency. Target applications for the core include servo control; audio-domain DSP, such as speech processing; data communications; modems; automotive systems; and portable applications, such as wireless phones and Internet appliances.

Development support: Infineon delivers support for embedded-microcontroller-system and applications developers in two ways. The SPACE (Semiconductor microcontrollers Partners for Applications using Chips for Embedded control, www.spacetools.com) acts as a clearinghouse for access to hundreds of third-party hardware and software tools for developers working with Infineon microcontrollers. DAVe (Digital Application virtual Engineer) is an interactive CD-based engineering-support tool distributed by Infineon. This application- and data-resource tool provides engineers with a single reference for information on all Infineon microcontroller products, including 8-, 16-, and 32-bit microcontrollers. It provides comparative information for all products and intelligent configuration wizards that generate C-level programming templates, including appropriate drivers for all on-chip peripherals and interrupt controls. It includes Web links to common compilers, such as Keil, Tasking, and Green Hills, providing a programmable software interface and access to software tool chains from these providers.

Integrated Device Technology

IDT's RC32XX FAMILY OF PROCESSORS integrates a 32-bit MIPS core with peripherals, such as an SDRAM controller, an on-chip arbiter supporting as many as three external bus masters, a general-purpose memory/IO controller, and a v2.2 PCI interface. These processors target networking, storage, and graphics peripherals.

Development support: Because a 32-bit MIPS core is the basis for all of IDT's proces-

sors, the third-party tools that support the MIPS architecture support all RC32xx devices. Applicable software-development tools include Multi from Green Hills, Code Warrior from Metroworks, and Tornado from Wind River. Operating-system support for these devices includes Accelerated Technology's Nucleus, Lineo and Monta Vista's Linux, Red Hat's eCOS, and Wind River's VxWorks. In-circuit emulators are available from Abatron, Corelis, Embedded Performance, Lauterbach, Macraigor, and Wind River. Application-specific reference platforms are available from Broadcom, Alcatel, and Jungo.

Intel

THE INTEL186 PROCESSOR IS A 16-BIT microprocessor targeting modems, public and private PBX (private-branch-exchange) switching systems, cellular phones, point-of-sale applications, and handheld terminals. The core architecture for these processors is the same as those developed for the PC industry, providing software compatibility and leveraging the PC-support infrastructure for the embedded designer. The upgrade paths for the Intel186 processor are the Intel386 and Intel486 microprocessors.

Intel bases the Intel386 DX, EX, and SX embedded processors on the 32-bit Intel386 architecture. Key features of these devices include PC compatibility, power management, low-voltage operation, and on-chip integration of peripherals, such as interrupt controllers, chip selects, counters, and timers. The static Intel386 SX microprocessor features clock-freeze mode and higher speed operation and is a pin-for-pin replacement for the dynamic Intel386 SX processor. The dynamic Intel386 SX microprocessor is an entry-level processor with a 16-bit external data bus and a 24-bit external address bus. It provides the performance benefits of a 32-bit architecture at the cost of a 16-bit hardware system. The dynamic Intel386 DX microprocessor offers a 50% performance increase over Intel386 EX and SX processors and can address 4 Gbytes of physical memory and 64 Tbytes of virtual memory.

The register-based 80386 architecture employs four general-purpose registers, four index/pointer registers, six 16-bit segment registers, and two 32-bit status and control registers. The Intel 8086 architecture uses 64-kbyte segments to extend addressing to 1 Mbyte. The 80386 also uses segmentation; however, because the general-purpose and index/pointer registers are now 32 bits, the segment limits extend to the full 4-Gbyte addressing range, and a segment register references a segment descriptor with a 32-bit base address. These descriptors also carry addressing-range and protection limits to prevent data accesses into code, into data that executes as code, and into inner privilege levels by outer levels. Hardware-descriptor registers hold segment-access rights and segment-base address and size limits. In protected-mode addressing, a 16-bit selector points to a segment descriptor and furnishes a base address. The base address adds to the 32-bit effective address, producing a 32-bit linear address, which the 80386 then uses as a physical or linear-page address. The 80386 has four code/data breakpoint registers and two control registers for debugging.

The standard 386 employs an SMM (system-management mode) for power management that enables code to control processor power without rewriting or revamping the operating software. The processor enters SMM via the system-management hardware interrupt, which sets the SMMs to reduce chip-power dissipation. Idle mode discontinues CPU processing but keeps the peripherals active, and power-down mode shuts down the chip.

The Intel486 microprocessor is a 32-bit microprocessor targeting embedded applications, such as terminals, embedded PC boards, industrial-control systems, scanners, printers, medical equipment, and entertainment systems. Current embedded-Intel386-processor users can take advantage of the Intel486 architecture to extend the performance of their embedded designs. The Intel SL Technology, featured in the Intel486 processors, allows system designers to build intelligent power-management capabilities into hardware, making these capabilities

independent of application software. It permits power management to be an integral part of the system, regardless the operating system or application you're using. The SL Technology improves power management by preventing power-management features from conflicting with other software.

The 486 builds on the 386 architecture by adding a more efficient memory bus; an on-chip FPU; an on-chip, unified, level-1 cache; and a RISC-like implementation for the core load/store instructions. The 32-bit 80486 implementation retains the i386's complex instruction set but relies on a pipelined RISC-like implementation to speed execution for simple load/store instructions. The standard 486 microarchitecture has a five-stage pipeline; stages D1 and D2 decode the complex instruction set. The 486 chips use 1- to 15-byte-long instructions for complex operations. The D1 and D2 decoder stages give the hardware time to delineate and decode the instructions waiting in the instruction queue. The instruction or byte-code queue holds 32 bytes for decoding. By fetching four words at once from off-chip or local memory, the hardware minimizes contention between data and instruction accesses of the cache.

To speed processing, the hardware loads and writes cache lines in four-word bursts. The DX4 has a unified, four-way, set-associative cache that implements a write-through policy: Writes to cache pass through to memory, which raises memory bandwidth. The 486's bus and cache implement a bus-snooping protocol for multiprocessor operation. The bus is more efficient than the 386's and has a two-clock single read or write. Four-word read bursts require five cycles and constitute most 486-bus accesses. The processors also support secondary level-2 cache for both single-processor and multiprocessor operation, as well as write-through/write-back protocols. The 486 has four code/data breakpoint registers and two control registers for debugging.

The standard 486 employs an SMM for power management that enables code to control processor power without rewriting or revamping the operating software. The processor enters SMM via a system-management hardware interrupt, which can set the SMMs to reduce chip-power dissipation. A halt instruction powers down most of the CPU's logic.

The i960 architecture family consists of high-performance, 32-bit embedded RISC processors targeting local- and wide-area networking, telecom applications, and imaging applications. The devices are code-compatible, offering a range of performance options and a migration path that preserves hardware and software investments.

The 16-bit, embedded MCS96/296 microcontroller families target event processing, high-speed I/O, and motor control. The MCS96's register-based architecture reduces accumulator bottlenecks and enables fast context switching—supporting bit, byte, word, and 32-bit operations. The MCS296 instructions include multiply-accumulate, indirect-autoincrement addressing, block-data move, and table-indexed jump instructions. The 8-bit MCS51/251 microcontroller families target event control for applications such as traffic-control equipment, input devices, and computer networking. The MCS-51 includes bit-manipulation instructions, including AND or OR with a carry bit for a 16-byte area of RAM and special-function registers. The MCS251 is a descendant of the MCS51 architecture, featuring 18-bit linear addressing and an extended instruction set for 16- and 32-bit arithmetic and logic instructions.

Development support: Numerous third-party vendors support the Intel architectures with assemblers, compilers, linkers/locators, remote software debuggers, software simulators, and integrated design environments for software development. Additional development tools include Windows-based software, evaluation boards and kits, in-circuit emulators, logic analyzers, single-board computers, and integrated device-programming support for Intel's embedded products. Operating-system support includes DOS, windowed operating systems, and a variety of RTOSs ranging from small, royalty-free microkernels to feature-rich GUI RTOSs.

Microchip Technology

THE PIC12 MICROCONTROLLER FAMILY PACKS the RISC-based PICmicro microcontroller architecture into eight-pin packages with a range of devices, from pure digital microcontrollers to devices with ADCs, onboard EEPROM, brownout reset, internal oscillator, analog comparators, 8/16-bit timers, watchdog timers, code protection, various power-saving modes, wakeup on pin-change, and internal pullup resistors. The family of products is available in ROM, OTP, and flash program memory and supports migrating to other family devices or to higher-pin-count devices, because the devices are code- and pin-compatible.

The PIC16 microcontroller family is upwardly compatible for PIC12 devices in 18- to 44-pin packages with a range of peripheral-integration options. Available peripherals include 8- to 12-bit ADCs, onboard EEPROM, analog comparators, voltage references, operational amplifiers, brownout reset, an internal oscillator, 8/16-bit timers with capture/compare and PWM modes, a watchdog timer, code protection, various power-saving modes, wakeup on pin change and internal pullup resistors. The devices feature hardware support for various communication protocols including I²C, SPI, AUSART, and USB. The family of products is available in ROM, OTP, and flash program memory and supports migrating to other family devices or to higher-pin-count devices, because the devices are code- and pin-compatible.

The PIC18 microcontroller family of devices is both socket and software upwardly compatible with the PIC16 and PIC12 families. The PIC18 family includes popular peripherals, such as MSSP (Master Synchronous Serial Port), SCI (Serial Communication Interface, RS485, RS-232), CCP (Compare/Capture/PWM), and CAN (controller-area-network) 2.0B Active for the most flexible option. Additional features include a power-on reset, power-up timer, oscillator start-up timer, programmable code protection, and power-saving sleep mode. Selectable oscillator options include a 4× PLL for the primary oscillator and a secondary 32-kHz oscillator clock input. The devices support a 25/25-mA sink/source, in-circuit serial programming over two pins, and a master synchronous serial port module with three-wire SPI and I²C master/slave modes of operation.

The rPIC microcontroller family of devices integrates PICmicro devices with UHF wireless-communication capabilities for low-power RF applications. The devices offer a small package outline and low external component count to support space-constrained applications. The devices offer six I/O pins, 33 single-word instructions, full-speed instruction cycle at 4 MHz, seven special-function hardware registers, an 8-bit real-time clock/counter with 8-bit programmable prescaler, a watchdog timer, and a direct LED drive. The on-chip 310/440-MHz transmitter enables designs to conform to US Federal Communications Commission Part 15 regulations and European ERC (European Radiocommunications Committee) 70-03E and EN 300 220-1 requirements. The transmitter features a VCO phase locked to quartz crystal reference, which allows narrow receiver bandwidth to maximize range and interference immunity.

Development support: Microchip provides in-circuit emulators (MPLAB-ICE 2000, ICEPIC), a software simulator (MPLAB SIM), a universal PICmicro macroassembler (MPASM Assembler), an in-circuit debugger (MPLAB ICD 2), device programmers (PICSTART Plus and PRO MATE II), and devices that support in-circuit serial programming. More than 130 third-party developers offer development systems for the PICmicro architecture. The software-development tools operate within the MPLAB integrated development environment and include a simulator, a macroassembler linker, and a C compiler for each architecture.

MIPS Technologies

THE MIPS32 4K FAMILY (4Kc, 4Km, 4Kp) is a set of synthesizable 32-bit MIPS RISC cores targeting low-power applications. It employs a single-issue five-stage pipeline with most instructions executed in one clock cycle and integrated four-way set-associative caches, each supporting as much as 16 kbytes of instruction and data cache. The 4Km and 4Kc employ a

32×16 single-cycle MAC (multiply-accumulate). The MIPS32 4K Family offers a number of power-management features, including low-power design, active power management, and power-down mode. The MIPS32 SmartMIPS 4KSc implements the MIPS32 architecture with SmartMIPS ASE (application-specific extension) and MIPS16e code compression as well as enhanced security features, such as execution-signature concealment and antihacker data security.

MIPS32 4KE Family (4KEp, 4KEm, 4KEc) is a set of synthesizable 32-bit cores based on the MIPS32 instruction-set architecture with optional MIPS16e code compression. It implements a single-issue, five-stage pipeline, fine-grain power management (clock gating), coprocessor port, and support for separate write-back caches and scratch-pad memories. The memory-management unit uses four-entry instruction and data TLBs (translation look-aside buffers) and a 16-dual-entry joint TLB with variable page sizes. The 4KE cores implement single-cycle 32×16-bit MAC instructions and two-cycle 32×32-bit MAC instructions. An optional enhanced JTAG block allows for single-stepping of the processor as well as instruction and data virtual-address breakpoints.

The MIPS32 M4K is a 32-bit MIPS RISC core targeting multiprocessor and deeply embedded applications. It implements the enhanced MIPS32 architecture and supports user-defined instruction-set extensions for stronger performance. MIPS16e code compression and the core's cacheless design keep the area small and the power consumption low. New instructions include insert field, extract field, rotate, and byte swap to improve packet handling. Hardware-prioritized vector interrupts minimize the interrupt latency and overhead. The M4K core provides multiple CPU semaphores for software-coherent systems and memory-synchronization support.

The MIPS64 5K Family (5Kc, 5Kf) is a set of synthesizable 64-bit processor cores based on MIPS64 instruction-set architecture with a limited dual-issue, six-stage pipeline, multiple cache-size options (0 to 64 kbytes), an optional IEEE 754-compliant FPU, and a coprocessor interface. You can organize each cache as direct-mapped, two-way, three-way, or four-way set-associative. The architecture includes special MAC, conditional move, prefetch, wait, and leading zero/one detect instructions. The MMU contains a configurable 16, 32, or 48 dual-entry joint TLB with variable page sizes, and four entries each of instruction and data micro TLBs.

The 5Kc core's instruction-scheduling mechanism eliminates pipeline stalls on cache misses and includes a load-scheduling slot. For software debugging, the 5Kc's EJTAG-debugging implementation supports instruction-software breakpoints, a single-step feature, and a dedicated debugging mode. Developers can schedule four instruction and two data hardware breakpoints. An optional test-access port forms the interface to an external debugging host and provides a dedicated communication channel for debugging of an embedded system.

The MIPS64 20Kc is a high-end 64-bit custom core that implements the MIPS64 instruction-set architecture and the MIPS-3D ASE (application-specific-extension) instructions to accelerate 3-D geometry processing. The 20Kc core is a dual-issue, seven-stage-pipeline processor core featuring a 32-kbyte, four-way set-associative instruction cache; a nonblocking four-way set-associative data cache; an MMU with a fully associative eight-entry data TLB; a fully associative 48 dual-entry instruction/data joint TLB; and an IEEE 754-compliant, MIPS-3-D capable FPU. The 20Kc core can issue two integer instructions, one integer and one floating-point instruction, or one floating-point operate instruction and one floating-point load/store instruction per cycle. The pipelined FPU executes single-precision, double-precision, and paired-single (two-way SIMD single-precision floating-point) instructions. The 20Kc core implements the MGB (MIPS-gigabytes-per-second) bus protocol, which uses a 64-bit multiplexed address/data input bus driven by a system controller and a 32-bit multiplexed address/data out-

put bus driven by the processor. The system interface supports split transactions, out-of-order-data return, external (system) interventions, and validations for coherent I/O.

Development support: MIPS Technologies and more than 70 independent suppliers provide software support for the MIPS architecture. MIPS Technologies provides development boards and development kits for software development and silicon integration. The development tools include tool chains from Green Hills, Mentor Graphics, and Wind River. Supported operating systems include VxWorks, WinCE, ThreadX, and Linux OS (from multiple vendors).

Mitsubishi Electric & Electronics USA

THE M32R/ECU FAMILY INTEGRATES a 32-bit RISC CPU, a 32×16 -bit MAC (multiply-accumulate) unit, and on-chip peripherals. The processor executes most instructions in one clock cycle using an instruction fetch, decode, execute, memory access, and write-back. The decoding stage dispatches instructions in order, and the remaining stages execute them out of order to hide memory-access latency. The MAC unit contains a single-cycle, 32×16 -bit multiplier and a 56-bit accumulator. The memory maps directly to the address space and has memory modes for internal instructions and data, for internal and external instructions, and for external memory only.

The M16C 16-bit family's RISC-like architecture takes advantage of both accumulator- and register-based architectures and features a three-stage pipeline. The M16C CPU is upward-software- and pin-compatible throughout the M16C family members, with 70% of instructions executing in three or fewer cycles. The M16C family can perform 1-, 4-, 8-, and 16-bit operations; it includes a repeat-MAC instruction that uses the hardware-multiplier circuit and can perform a 16×16 -bit multiply in five cycles. The M16C family supports a masked-ROM program-correction function that uses an address-match interrupt scheme to allow designers to correct two faulty mask-ROM program areas with an external EEPROM.

The M16C provides a comprehensive approach to EMI/EMS noise immunity that eliminates the need for extra board components to manage noise issues, such as ferrite beads, dumping resistors, and capacitors. Some of the M16C noise-management features include separate power-supply lines that feed to the chip to reduce mutual interference noise, a robust internal power supply, high-input pin reliability via digital filters, and an adjacent V_{CC} and V_{SS} layout, where closely located power supply and GND make it easier to prevent noise from affecting the V_{CC} /GND wiring.

The instruction formats for the M16C family are zero, short, quick, and general. Programs that use 8-bit registers use the zero and short formats. The quick instruction format is useful for creating frequently used subroutines with minimal bytes. The general instruction format allows the transfer of data between any two registers within the CPU or the 1-Mbyte address, which you can address linearly or as four chip-select areas. Other features of the M16C include a 4-byte prefetch queue for pipelining, a 16×16 -bit multiplier, a barrel shifter, and a user-selectable 8- or 16-bit-wide data bus. Each of the two register banks comprises six 16-bit general-purpose registers and one frame-base register. The frame-base register helps manage the stack for C functions with local variables. You can use two registers as four 8-bit registers and two others as address registers. An additional register bank contains a static base register, a dedicated interrupt-stack pointer, and a stack pointer for user programs.

The 740 family comprises of hundreds of devices built around an 8-bit, accumulator-based CISC architecture that offers bit manipulation, memory-to-memory data transfer, and data transfers between the index registers and accumulator. The 7600 series includes an integrated DMA interface, a software-programmable slow-external-memory interface, and a hold function for use when more than one device needs control of the external address and data

bus. Peripherals are memory-mapped into the special-function-register area of RAM. The 38000 series has a 64-kbyte linear-address space with as much as 60 kbytes of integrated memory. A memory-expansion mode enables external memory through an external 16-bit address bus and an 8-bit data bus.

Development support: Mitsubishi Electric offers a C compiler, an emulator, and an evaluation board for its M32R/ECU family. Third-party development tools for the M32R/ECU 32-bit family include Wind River's Tornado integrated development environment as well as the pRISM+ integrated development environment for the pSOSystem RTOS. Red Hat supplies the GNUPro software-development tool suite, including C and C++ compilers and debuggers. Diab Data supplies a C and C++ compiler.

Mitsubishi Electric offers StarterKit Plus evaluation kits and emulation, development, and debugging kits for most of its M16C family members. Mitsubishi Electric also supplies a fully integrated development environment, including a C compiler, an emulator, and an evaluation board. Third-party development tools for the M16C family include cross tools, emulators, RTOSs, and programmers. Cross tools include the Embedded Workbench set of C/EC++ cross-compiler and debugger tools and the IAR MakeApp family of visual development tools from IAR Systems, the OPENplus integrated development environment from GAIO Technology, and the Tasking embedded software-development tools from Altium. Emulators include the Ultra-M16C microprocessor-development system from Ashling Microsystems and the EMUL-M16C-PC in-circuit emulator from Nohau Corporation. RTOS support includes OPENplus G-OS from GAIO Technology, CMX-RTX from CMX Systems, and embOS from Segger Microcontroller Systems. Device programmers include the BP-1400, BP-1600, BP-2200, BP-2600, BP-3600, and BP-4600 from BP Microsystems; and the PS200 and PS300 from Data I/O Corporation.

Mitsubishi Electric offers StarterKit Plus evaluation kits and emulation, development, and debugging kits for many of its 740 family members. Mitsubishi Electric also supplies a fully integrated development environment, including a C compiler, an emulator, and an evaluation board. Third-party development tools for the 740 family include cross tools and programmers. Cross tools include the Embedded Workbench set of C/EC++ cross compiler and debugger tools and the IAR MakeApp family of visual development tools from IAR Systems. Programmers include the BP-1400, BP-1600, BP-2200, BP-2600, BP-3600, and BP-4600 from BP Microsystems.

Motorola

THE HC05 FAMILY COMPRISES GENERAL-PURPOSE devices that feature a variety of memory options. The on-chip serial-communications interface provides asynchronous communications, with software-selectable baud rates reaching 250 kbps. The high-speed, synchronous, four-wire SPI can drive off-chip displays and peripherals. All devices within the family include a 16-bit, free-running and programmable counter that works in conjunction with input-waveform measurement and output-waveform generation. A watchdog timer guards against runaway software in noisy environments.

The 68HC08 family incorporates an advanced serial-communication multiplex-bus controller operating according to the SAE J1850 Class B protocol. Target applications for the BDLC (byte-data-link-control) module are automobiles in which multiple BDLC microcontrollers can communicate over a single- or dual-wire bus to offer diagnostic capability and reduce the weight and bulk of wire harnesses.

The 68HC11 family comprises six major series of microcontroller units, each composed of many related devices. The 68HC11D3 chip, with 4 kbytes of ROM, offers an economical alternative for applications when you need advanced 8-bit performance with fewer peripherals and

less memory. The 68HC11 E series contains flexible I/O capability to best meet an application's needs. The 68HC11 F family offers extra I/O ports, 1 kbyte of static RAM, chip selects, and a 5-MHz nonmultiplexed bus. The 68HC11 K devices, such as 68HC11K4 and 68HC11KW1, offer high speed, an MMU, PWMs, and plenty of I/O. The 68HC11 KS family offers processing performance with large on-chip memories and an additional power-saving mode in lower-pin-count packages. The 68HC11 P family offers a power-saving, programmable, PLL-based clock circuit along with many I/O pins, large memory, and three SCI (serial-communication-interface) ports.

The 68HC12 family devices are expanded bus, 16-bit microcontrollers that operate from 3 to 5.5V. Other features include 4 kbytes of EEPROM, as much as 5 Mbytes of external addressing capability, a PLL, and dual SCI modules. The 68HC12 B family integrates both flash EEPROM and byte-erasable EEPROM on-chip. All devices in this family incorporate an advanced serial-communication multiplex-bus controller operating with either the BDLC module (68HC912B32 and 68HC12BE32) or the CAN (controller-area-network) module (68HC912BC32). The 68HC12 D family is the highest integrated device in this series of 16-bit microcontrollers. All devices in this family include dual SCI modules, a CAN Module for advanced serial communication, dual 10-bit ADC modules, large program and data memory arrays using both flash and byte-erasable EEPROM, a PLL, and keyboard interrupts.

The HCS12 family of microcontrollers is the next generation of the 68HC12 architecture. Using Motorola's 0.25-micron flash, the HCS12 family provides an upward migration path from Motorola's 68HC08, 68HC11, and 68HC12 architectures for applications that need larger memory, more peripherals, and higher performance.

The 68HC16 family includes the lower cost devices of the 68HC16 Z family, targeting expanded memory applications that require high-performance serial communications and basic analog functions. The 68HC16 Y family comprises highly integrated single-chip devices with flash memory or ROM, a time processor unit, three serial interfaces (two SCI and one SPI), and an ADC. The 68HC16 X and R families focus on lower cost, lower pin count, single-chip devices with flash, serial, and analog capabilities.

With its 68K heritage, Motorola's ColdFire architecture is driving the 68K family into the future. The 32-bit ColdFire devices target applications such as embedded networking, PC peripherals, and electronic motor-control. The 32-bit MPC500 family features a PowerPC core targeting applications from avionics, industrial control, engine management, and global positioning systems to robotics. It offers 1 Mbyte of flash memory for embedded control applications.

Development support: Development support is available from Motorola through Metrowerks as well as leading independent tool developers, providing processor probes, logic analyzers, debuggers, simulation-development environments, C and C++ compilers and emulators, low-cost BDM (background-debugging-mode) emulators, kits for code development and evaluation, and stand-alone programmers. Motorola's Web site offers a large library of microcontroller application notes, a searchable technical microcontroller FAQ, online answers, and downloadable software examples.

National Semiconductor

NATIONAL SEMICONDUCTOR'S GEODE FAMILY of processors targets information appliances, such as thin clients, interactive set-top boxes, personal access devices, and Microsoft Windows-powered smart-display devices. The processor's x86 architecture supports popular software plug-in modules for Internet access. Each Geode family of processors supports power-management features that include support for the Advanced Power Management and Advanced Configuration and Power Interface standards for legacy and Windows power man-

agement. Hardware- and software-controlled modes include active-idle mode, in which only the core stops; standby mode, in which the core and all integrated functions halt; and sleep mode, in which all devices and the external clocks stop.

The Geode GX1 and Single Chip processors are six-stage-pipelined cores that include an integrated FPU with MMX, a 16-kbyte unified L1 cache, and an MMU that adheres to standard paging mechanisms; re-entrant system-management mode enhanced for National Semiconductor's virtual-system-architecture technology; and an SDR (single-data-rate) SDRAM controller. The Geode GX2 family of processors is an eight-stage pipelined core that includes an optimized FPU (MMX and 3Dnow!), 16 kbytes each of instruction and data caches, and an SDR SDRAM or DDR SDRAM controller.

The 8-bit COP8 microcontrollers target high analog applications in industrial, automotive, security, and consumer electronics. They support multiple power-save modes and versatile memory configurations. The CR16 (CompactRISC) microcontroller primarily targets automotive and industrial controller applications. The product portfolio divides into two subgroups—one for general-purpose microcontrollers and one for CANInterface microcontrollers.

Development support: National Semiconductor and third-party suppliers offer low-, medium-, and high-end simulation, emulation, and debugging tools. Programming tools are available from a large selection of approved programming vendors.

Nazomi Communications

NAZOMI'S JA108 UNIVERSAL JAVA accelerator chip is the first device under the KChip product line. The JA108 offloads the microprocessor processor load by taking over the task of executing Java software. It can speed Java execution by 200× and improve multimedia performance by 10× depending on the application. It accomplishes this performance without increasing system-clock frequencies, it requires neither additional memory nor new tools, and it requires no new porting efforts. The chip, which interfaces like a standard SRAM device, is a stand-alone accelerator for Java and multimedia applications that you can integrate into designs on memory buses. The JA108 complies with all Java standards and is available in an 8×8-mm, 132-ball μBGA with a 0.5-mil pitch configuration. The JA108 works with any baseband processor, chip set, or microprocessor and is transparent to designs and legacy operating systems. It allows designers the freedom to choose any RTOS and JVM (Java Virtual Machine), regardless of whether Sun Microsystems authorizes or independently developed them.

Development support: Nazomi offers the JPOP (JRE Porting Options Program) to integrate Nazomi's JA108 Java Multimedia Accelerator chip into mobile wireless platforms. The JPOP includes application-programming-interface references for JVM adaptation for Sun Microsystems' CLDC KVM (Connected Limited Device Configuration K virtual machine), software kernel, and microcode.

NEC Electronics

NEC ELECTRONICS BASES THE K0, K0S, and Kx1 8-bit processor families on a common architecture, with more than 700 variations covering a large selection of integrated peripherals and a variety of memory sizes and types. The memory configurations include ROM, flash, OTP and E². The devices operate at 1.8 to 5.5V with standard temperature operation of -40 to +85°C. Many K0 devices offer an internal expansion-RAM feature in addition to normal on-board SRAM. Users can employ this expansion RAM to load and execute instructions as well as store data. Some devices, such as the 78K0, support low power consumption in a variety of operating modes with as many as eight adjustable energy-saving settings that can reduce power dissipation down to a few microamps.

The Kx1 architecture bridges the gap between 8- and 32-bit performance and comprises two the 8-bit 78K0/KX1 and the 32-bit V850ES/KX1 series of microcontrollers. Both families feature identical peripherals with identical special-function registers using the same software. This configuration allows you to migrate designs across the 8- and 32-bit boundaries as required. The V850/Kx1 series generates less than 100 dB of noise, targeting EMI-sensitive applications. High-end Kx1 devices include hardware 16×16 and 32×32 multiply and 32/16 divide instructions.

The μ PD789881 microcontroller targets battery-operated devices with a typical 18- μ A current consumption when operating at full speed and 2.7V and a typical standby current of 0.9 μ A. This microcontroller includes an integrated (26×4) LCD controller/driver. It can use an internally generated 500-kHz clock for CPU operations and an external 32-kHz clock to operate all the on-chip peripherals. Users can dynamically switch CPU operation between the two clock speeds to accommodate performance and power-consumption requirements. The traditional power-saving modes of Halt and Stop are still available. The μ PD789881 also contains a hardware multiplier, 8- and 16-bit timers, a watchdog timer, a UART, and 512 bytes of SRAM; it is available in 32-kbyte flash-memory and 16-kbyte ROM versions.

The VR4121 is a member of the ultralow-power-consuming devices in the VR41xx series targeting portable devices. The VR4121 has a VR4120 core that incorporates a five-stage pipeline and supports the MIPS III and MIPS 16 instruction sets. This processor integrates peripherals, such as a 16550-compatible serial interface, IrDA interface, keyboard and touch-panel interface, software modem, ADC, and DAC. The VRC4171A is compatible with the VR4121 and includes additional peripherals, such as an LCD controller.

The VR4131 is a member of the highest performance devices in the VR41xx series and supports the MIPS64 and MIPS16 instruction sets. The device integrates a two-way, six-stage pipelined VR4130 core with cache memory, MMU, and peripherals including a DMA interface, serial interface, IrDA interface, and real-time clock. The VR4131 has a 32-bit external memory bus and supports a PCI-bus interface for external devices. It offers four power-saving modes, including standby, suspend, eXsuspend, and hibernate.

The VR4181 is a member of the low-power-consuming devices in the VR41xx series, targeting portable applications that require low power use without using a system controller, such as a Linux PDA. The VR4181's integrated peripherals include an LCD controller, a Compact-Flash interface, a power-management unit, a DMA unit, an interrupt-control unit, timers, a real-time clock, a 16550-compatible serial interface, an IrDA 1.0 interface, a keyboard interface, a touch-panel interface, an ADC, a DAC, and a USB functional interface. The VR4181A is similar to the VR4181 but operates at a higher speed and integrates more peripherals into the chip.

The VR4310 is one of the highest performing devices in the VR4300 series, targeting applications needing 64-bit performance. It uses a five-stage pipeline and is upgradeable to the VR5432. You can pair the VR4310 and the VRC4375 system controller.

The 167-MHz VR5432 microprocessor incorporates a gated clock, minimal switching techniques, and an MMU. Its symmetric dual-issue pipeline, with six independent execution units, executes any combination of ALU, floating-point (with 64-bit barrel shifter unit), or rotate instructions, and the 32-kbyte instruction and data caches perform cache-line locking to keep critical code and data-cached. The pipeline incorporates local bypasses to bypass write-back for immediate data use. Multiple outstanding read transactions allow concurrent filling of both caches that keeps the processor supplied with a steady stream of instructions and data. To enable each pipeline to handle both integer and floating-point operations, the floating-point operations split with the mantissa in the integer portion of the pipe and the exponent in the separate 12-bit ALU. Mapping accesses to virtual memory addresses is optimized with a 48-double-entry joint instruction/data TLB (translation look-aside buffer) and two separate four-

entry micro TLBs for instructions and data.

The VR5000 microprocessor is a 64-bit processor with 64-bit interfaces that is compatible with the VR5500. It includes a dual-issue pipeline and features floating-point and MAC (multiply-accumulate) capabilities. It implements the MIPS IV instruction set and extends the instruction set with integer and other register-based multiply instructions for fast DSP support, integer-rotate instructions for fast 32- and 64-bit string operations, packed data-vector operations, and cache-line-locking instructions. The processor incorporates a standby mode that suspends all instruction execution to complement the low-power draw of the 1.5V core.

The VR5500 extends the performance line of VR Series microprocessors, is the successor to the VR5000 and VR5432 microprocessors, and implements the MIPS64 instruction set. The VR5500's two-way, out-of-order superscalar and super-pipelined microarchitecture supports efficient instruction execution relying on parallelism and higher clock frequency. The pipeline selects, in an out-of-order manner, two of the 16 fetched instructions and dispatches them to the appropriate integer unit (of which there are two), floating-point unit (of which there are two), branch-prediction unit, or load/store unit. The 10-stage pipeline enables the issue of two instructions per cycle and graduation of three instructions per cycle. The VR5500 can interchange between 32- and 64-bit data and integrates with system controllers such as the 32-bit NEC VRC5477, the 64-bit Algorithmics Bonito, and Marvell/Galileo controllers.

The VR7701 incorporates a version of the VR5500 processor as a core and integrates a set of peripherals via a 200-MHz internal 64-bit bus and a new 133-MHz DDR memory controller. This combination optimizes processing of large amounts of true 64-bit I/O on one chip. The VR7701's integration features include Bi-Endian DMA for the various interfaces, a 64-bit PCI/PCI-X interface with master and slave capabilities, two Ethernet MACs, a 32-bit multiplexed local bus, an interrupt control unit, and a clocked serial interface. The VR7701 extends the MIPS64 instruction set with instructions for integer multiply-add, three-operand integer multiply, 32- and 64-bit rotate, leading one/zero count, and wait.

Development support: The development tools for all NEC processor families use the same user interface and include C language support. Available simulators include virtual hardware support and viewing of timing waveforms. For both the K0 and K0S families, the simulator supports interfacing with both peripherals and virtual hardware, such as keypads, LCDs, switches, LEDs, and analog inputs. The user interface for the simulator and emulators are virtually identical, facilitating collaboration between groups. The emulator can also use files that the simulator uses.

To aid rapid code development, the NEC Web site includes downloadable C and assembly programming examples for K0 and K0S 8-bit microcontroller family peripherals. You can download from the Web site evaluation versions of the C compiler, assembler, and simulator, as well as updated device files and software updates. NEC works with a variety of third-party vendors for development support. IAR provides alternative support for both the K0 and K0S devices with C compilers and assemblers. Green Hills, Accelerated Technology, and Red Hat offer C compilers, RTOSs, and other software-development support for the 32-bit processors.

NEC is a member of EEMBC (EDN Embedded Microprocessor Benchmark Consortium, www.eembc.com) and has performed benchmarking for eight devices to support comparison with similar microcontrollers and microprocessors for embedded applications. You can find the scores on the NEC and EEMBC Web sites.

NetSilicon

THE NET+ARM FAMILY OF PROCESSORS from NetSilicon are 32-bit SOC (system-on-chip) ASICs targeting networked applications. The NET+ARM includes a 10/100BaseT Ethernet MAC (media-access controller) with MII (media-independent interface) and independent serial

ports that can run in UART, HDLC, or SPI modes. The onboard processor is an ARM7 32-bit RISC processor core with support peripherals such as memory controllers for five types of RAM, including flash memory and EEPROM, timers, DMA controllers, an external bus-expansion module, and as many as 40 general-purpose I/O pins.

Development support: Developers using the NET+ARM processor family can choose Green Hills Software's Multi IDE or Microcross' Gnu X-Tools for software development. The standard level of customer support includes one year of hardware support, design review, and one year of software support.

Oki Semiconductor

OKI'S ML674X FAMILY, A STANDARD ARM-based processor family, comprises of a variety of general-purpose processors. The application-specific-standard-product series includes products such as Bluetooth baseband controllers and audio controllers for MP3 players. Oki's application-specific custom products use a platform-based SOC (system-on-chip) option with ARM-cores, IP libraries, and an AMBA bus architecture. The ML671000 includes a built-in USB 1.1 device controller.

Development support: Oki's ARM products leverage ARM's third-party development tools. Oki also provides dedicated ARM7TDMI development boards for its ML670100, ML671000, ML674000, ML674001, ML67Q4002, and ML67Q4003 standard products. These development boards are JTAG-interface-based development tools that come bundled with their own sample source code to assist the design-implementation process. Oki's ARM-based development boards support any third-party JTAG-interface boards and ARM-development software packages.

Patriot Scientific

IGNITE PROCESSORS DIFFER FROM CLASSICAL RISC architectures in that they use a stack-based architectural design with a zero operand, 8-bit opcodes instruction set that supports an internal 32-bit structure. The stack architecture couples with a zero-operand instruction set to enable extreme code density. The processors fetch instructions as a group of four from 32-bit memory. The processor does not use a cache, because random memory accesses complete in a single processor cycle. It does not implement pipelining but does perform a prefetch of four instructions while executing a current instruction group.

Development support: The Ignite Virtual Platform allows software designers to run applications on the Ignite with no hardware. This program allows you to tie to the Ignite other emulation models of hardware using well-defined APIs. The Virtual Platform allows users to characterize the behavior of the system and derive precise timing information related to task execution and interrupt latencies. Linux and Windows 98/2K/NT workstations support cross-platform development. Development packages are available with VxWorks Binary, vxPresso Binary (VxWorks and Personal Java), Personal Java Tools, vxPresso Build environment, vxPresso Programmer's guide, and VxWorks Board Support Package.

Philips Semiconductors

PHILIP'S CONTINUING 80C51 DEVELOPMENTS include complete migration to a C51 six-clock core and in-application/system-programmable flash memory. The design features include user-selectable power-management options, a low-power oscillator, and system operation down to 1.8V. The low-power LPC900 3V Flash family uses the C51 architecture and includes data EEPROM. The 80C51MX family is an 80C51-compatible architecture that includes a seamless

memory extension beyond 64 kbytes and introduces a linear code and data address range reaching 8 Mbytes. The device's improved EMC and processor speed rely on a 2× acceleration of the 80C51 core with six clocks per machine cycle.

Development support: Software and hardware development tools for the 80C51, 89LPC900, 80C51MX, and 16-bit XA are available from Philips Semiconductors' Web-site tools section and third-party suppliers, such as Ashling, BP Micro, Ceibo, Data I/O, EE Tools, Hitex, IAR, Keil, Metalink, Nohau, Phytex, Raisonance, Signum, System General, and Tasking. ARM's Realview development environment supports ARM7-based development. Multi-ICE (in-circuit-emulation) and trace systems are supported by Philips' on-chip implementations of E-ICE (JTAG) ETM (Embedded Trace Macrocell) debugging monitor for ARM-core support. Ashling, Hitex, Keil, and Nohau also provide third-party development-tool support for these processors.

PMC-Sierra

THE RM5200 FAMILY PROCESSORS ARE 64-bit microprocessors with 64-bit data paths, 64-bit ALU, and 32- or 64-bit external accesses. The processors include independent 32-kbyte instruction and data caches and support external peripheral and memory access at bus speeds exceeding 100 MHz. Clock speeds are 200 to 400 MHz, and typical power consumption is 1W.

The RM7000 family processors are 64-bit microprocessors that feature an L2 cache for LAN and WAN applications. It can simultaneously execute two integer instructions or one integer with one floating-point instruction. These processors integrate 256 kbytes of L2 cache and 16 kbytes each for independent L1 instruction and data caches. The RM7000A/B/C devices include an L3 cache controller for accessing as much as 8 Mbytes of external cache. Clock speeds are 300 to 600 MHz, with SysAD capability reaching 125 MHz. Typical power dissipation is less than 3.5W at 400 MHz.

The RM9000x2 integrated multiprocessor includes enhancements for networking, offering tightly coupled L1/L2 caches with deterministic access times, a seven-stage pipeline that allows a 1-GHz pipeline frequency, and sophisticated branch prediction. The five-state MOESI (modified-shared/exclusive/shared/invalid) protocol maintains cache coherency, and all cache transfers between CPUs occur at the CPU's pipeline frequency. HyperTransport and SysAD interfaces support hardware-I/O coherency, enabling I/O devices access to coherent memory. The 160-Gbps, shared-memory, multiport switch fabric connects the CPU subsystem with the memory and I/O interfaces and allows simultaneous accesses to all ports. The 200-MHz DDR-SDRAM interface provides 25.6 Gbps of memory bandwidth, and the HyperTransport and SysAD interfaces provide connections to a range of high-speed networking peripherals. A local bus provides connectivity to lower speed devices. The vectored, prioritized interrupt controller supports 256 mappable, external, and interprocessor interrupts to support multiprocessing. The on-chip EJTAG debugging module supports hardware and software debugging.

Development support: Third-party development partners for PMC-Sierra MIPS processors include Momentum Computer and its "Ocelot" family of CompactPCI development platforms. Board-support packages that support the VxWorks and Linux operating systems are available. Applied Microsystems Corporation provides NetROM for debugging and boot-code development. NetROM serves as a virtual communication channel between the host and target system, and as a networked device, can download applications directly into RAM from remote locations at Ethernet speeds.

QuickLogic

QUICKMIPS FAMILY MEMBERS COMBINE a MIPS32 4Kc processor core running at 175 MHz maximum with programmable logic and application-specific functions on a single piece of silicon. The 32-bit AHB (Advanced High-performance Bus) runs at half the CPU clock frequency and supports two 10/100 Ethernet ports; a 33/66-MHz PCI host; a high-bandwidth memory controller for SDRAM, SRAM, and EEPROMS; a master and slave port to the programmable fabric; and a global system configuration and interrupt controller. A 32-bit APB (Advanced Peripheral Bus) running at half the CPU frequency contains three slave ports to the programmable fabric, two serial ports (one with modem-control signals and one with IrDA-compliant signals), and four general-purpose 32-bit timer-counters.

Development support: QuickLogic's system development kit for the QuickMIPS platform includes a QuickMIPS device and a board-support package with an RTOS, timing model, and drivers. Green Hills Software's Multi 2000 and Accelerated Technology's code|lab Embedded Developer Suite support source-level debugging. A system analyzer combines an enhanced MIPS EJTAG FS2 BlackBox debugging probe with a configurable logic-analysis monitor; on-chip logic accesses as many as 128 internal nodes (32 that you can trace simultaneously) in the programmable fabric. The device can capture trace information on-chip with a trace depth reaching 4000 frames.

Rabbit Semiconductor

THE 8-BIT RABBIT 2000 AND RABBIT 3000 microprocessors use a 64180/Z180-style architecture. It eliminates obsolete or little-used 64180/Z180 instructions and adds 1-byte operation codes for 16-bit logical and arithmetic operations, including compact instructions for 16-bit indexed loads and stores. The Rabbit 2000 and 3000 have a low-power "sleepy" mode of operation that reduces current consumption to 2 μ A at 1.8V, by continuing to execute instructions at a slower rate. They support six or 11 programmable-processor-clock modes and several programmable wait states. A separate power pin for the real-time clock can shut down the processor while keeping alive the battery-backable clock. An 8-bit slave port allows the Rabbit to act as an intelligent peripheral device. Other features include glueless interfacing to memory and I/O devices, remote cold boot, and spread-spectrum circuitry for low EMI.

Development support: Z-World's Dynamic C environment includes an interactive compiler, editor, and source-level debugger that support software development for Rabbit microprocessors. Dynamic C can handle applications exceeding 50,000 C statements and takes advantage of Rabbit's instruction set to reduce the need for assembly-language programming. Dynamic C includes a royalty-free TCP/IP (Transmission Control Protocol/Internet Protocol) stack and source code. The Premier edition of Dynamic C includes the royalty- and license-free Jean Labrosse MicroC/OS-II real-time kernel and a PPP (Point-To-Point Protocol) library for TCP/IP communications. Rabbit Semiconductor developers can alternatively use an ANSI-C-compliant software package from Softools.

SandCraft

THE SR71000 FAMILY OF PROCESSORS IS a two-way superscalar MIPS64 architecture with a nine-stage pipeline targeting applications such as networking, image processing, and Internet servers. The architecture can operate to a maximum frequency of 600 MHz and includes dual instruction fetch, up-to-six issue, up-to-six execute, and dual-commit, to sustain an instruction-throughput rate of two instructions per cycle. Sophisticated branch-prediction techniques keep the pipeline in full use.

The SR71000 family of processors includes on-chip 512-kbyte L2 cache, L3 cache controller, and L3 cache tags. The SR71000 family designs are fully static with dynamic power-

saving features. The system interface, which is fully compatible with the R4xxx/5xxx/7xxx SysAD interface, can operate to 133 MHz with split transactions and out-of-order return. The SR71000 family includes a floating-point unit that is fully MIPS64-compliant. The FPU is decoupled from the integer pipeline, allowing autonomous integer and floating-point operations.

Development support: SandCraft offers a development tool kit for the SR71000 family of microprocessors. The \$4999 SR71010tk1 leverages standard third-party software tools and the VxWorks operating system from Wind River. The SR71000 and SR71010 have booted many of the RTOSs used in the networking and imaging industry. A Linux OS by RedHat is available. The SR71010tk1 tool-kit development board provides Ethernet ports and logic-analyzer connection ports for convenient code development and debugging; a full set of compilation tools, including an optimizing C compiler from Red Hat, optimized specifically for this CPU architecture; linkers; loaders; libraries; and a full set of documentation, including the SR71000 user manual and tools manual.

Sharp Microelectronics of the Americas

THE 8-BIT BLUESTREAK PRODUCT LINE uses an enhanced 8051 core that runs at 12 clocks per cycle; the 8051 standard runs at two clocks per cycle. The 40-MHz CPU is software-compatible with a standard 8051 and includes a two-wire debugging interface. The 16-bit BlueStreak product line combines the performance of a 32-bit ARM core with the code density of 16-bit applications. It includes an LCD controller, CAN (controller area network) 2.0b, ADC, and capture/compare hardware. The ARM core allows smooth migration to the 32-bit BlueStreak product line, which provides higher performance and higher integration. The LH7A405 has a hardware JIT (just-in-time) Java Compiler that speeds Java execution by five times and consumes less power than traditional software JIT Java compilers. Direct support of common LCD panels (including Sharp's Advanced TFT) is available on most BlueStreak products.

Development support: Keil and IAR Systems support development for Sharp's BlueStreak line of Enhanced-8051 8-bit microcontrollers. First Silicon Solutions provides a low-cost JTAG-like debugger, providing features such as in-circuit programmability, the ability to set complex breakpoints and view/modify registers and memory, and trace capability. Sharp has partnered with leading companies, such as Embedix/Lineo and bSquare, to provide Linux and WinCE 3.0/.NET options for its 32-bit ARM720T and ARM922T product line. For all BlueStreak products, evaluation boards are available from Sharp or Sharp's distributors.

Silicon Storage Technology

THE DUAL-BANK ARCHITECTURE OF SST'S FlashFlex51 microcontroller family maps the flash memory into two independent blocks. The primary memory block comprises as much as 64 kbytes of SuperFlash EEPROM with a 128-byte sector size. The secondary memory block of 8 kbytes of SuperFlash EEPROM, also with a 128-byte sector size, can act as either electronically erasable nonvolatile data or code storage. The FlashFlex51's dual-memory-block architecture supports in-application programming and allows the processor to run user programs from one flash-memory block while in the background concurrently servicing a flash-programming operation on the other block.

SST's microcontrollers also include the company's proprietary SoftLock security features. SoftLock is a security-protection mode that prevents both accidental overwriting of program memory and software piracy while still enabling in-application programming operation under the secured environment. SST's SoftLock mode contains a four-level security-lock scheme. To support advanced features, SST's FlashFlex51 products also offer 1 kbyte of on-chip SRAM,

which is four times the amount that most industry-standard 8051-compatible microcontrollers offer.

Development support: Recent additions to SST's development tools include the company's second-generation BSL (bootstrap-loader) demo kit with enhanced Windows software, as well as the new FlashFlex51 SoftICE (software in-circuit emulator), a software utility that offers true in-circuit-emulation capabilities through a popular third-party Windows monitor interface without requiring additional on-chip peripheral circuits and external components. The SoftICE tool supports the in-application-programming capability of SST's FlashFlex51 products.

SST's FlashFlex51 BSL Demo Kit includes new BSL features with Windows software. It also includes an improved target board for SST microcontrollers to demonstrate the full in-application-programming capabilities of the FlashFlex51 microcontrollers through the BSL, which is factory-preprogrammed into most of the FlashFlex51 microcontrollers. With the new board, designers can vary the operating frequency; run the device at 2.7 to 5.5V; control the device reset and EA (External Access) pins onboard and offboard; and upload and download microcontroller-unit files from internal or external memory.

STMicroelectronics

THE 8-BIT ST7 CORE USES A VON NEUMANN architecture, which means only one addressing space maps the program, data, and I/O peripherals. The advantages are that accesses to any byte of program, data, or I/O use the same instructions, and no special instructions are necessary to access constant data in program memory or I/O. The accumulator-based core uses six internal registers including a 16-bit program counter. The instruction set has 63 instructions with 17 addressing modes supporting 8×8-bit unsigned multiply, true bit manipulation, various bit/byte transfer modes, and powerful branching logic. The core handles peripheral resources via dedicated interrupts and registers.

The accumulator-based ST6 with only 40 instructions is a low-end Harvard-architecture microcontroller. The core includes two 8-bit index registers; two 8-bit, general-purpose registers; an 8-bit accumulator register; and a 12-bit program counter. All basic arithmetic operations involve the accumulator as one parameter and end by placing a result into the accumulator. At a maximum operating frequency of 8 MHz, most instructions execute in 3.25 to 9.75 msec, and the average instruction time is 6.5 msec. Registers and peripherals are memory-mapped in the chip's address space. To configure, send, or receive data to or from a peripheral, the program writes to or reads from the peripheral's memory registers. The program counter directly addresses as much as 4 kbytes of program memory. A banking scheme that uses a dedicated memory-mapped banking register can expand the program memory. The device can bank the lower 2 kbytes of ROM, providing access to higher 2-kbyte pages in the program memory with ranges as high as 20 kbytes. Program memory can also hold constants or tables that the processor accesses via a 64-byte, memory-mapped window in RAM that maps into ROM.

The 32-bit STPC family of microprocessors uses an x86 core processor for PC compatibility with a range of interchangeable standard functions, such as SDRAM UMA (Unified Memory Architecture) memory controllers, VGA and SVGA graphics controllers, a video-interface port, a TFT controller, a PCI controller, an ISA controller, a PCMCIA controller, a DMA controller, an interrupt controller, and integrated power management.

Development support: Hardware tools for ST6, ST7, and ST9 microcontrollers are available directly from ST and from third-party vendors. ST designs and manufactures hardware emulators, development kits, single-device programming boards, and evaluation boards. Third-party emulators, in-circuit debuggers, and gang programmers are available from an ex-

tensive list of third-party vendors. An assembly-language development environment is available free of charge from ST for the ST6, ST7, and ST9 microcontrollers. An ST6 C-compiler is available from Raisonance. ST7 C-compilers are available from Cosmic Software and Metrowerks. Hardware tools for ST10 microcontrollers are available from Hitex, Lauterbach, Nohau Phytex, Rigel, and FS Forth-Systeme. Software support for ST10 is available from Keil, Tasking, CMX, Wind River, OSEK, Vector, and 3soft.

Sun Microsystems

THE ULTRASPARC IIE MEMBER OF SUN Microsystem's UltraSPARC II RISC-processor family implements the full SPARC Version 9 architecture plus the VIS instruction set to accelerate small integer operations and provide special-purpose instructions. The CPU uses 64-bit address arithmetic and contains an MMU that translates 44-bit virtual addresses to 41-bit physical-memory addresses with 64-bit address pointers. The devices have 64-byte block-load and store instructions that use the 64-bit data paths and registers inside the processor, supporting high-performance memory-to-memory bandwidth. The VIS RISC instruction set extends the SPARC Version 9 architecture and accelerates multimedia, image-processing, and networking applications. Sun's medialib, a multimedia performance library, supports the VIS instructions via assembler, C functions, or macros.

The processor includes an SDRAM controller that supports PC-100-type SDRAM DIMMs and a 32-bit, 66-MHz PCI-bus interface, which is compatible with the PCI-specification version 2.1. The UltraSPARC Iie complies with the Energy Star initiative, supports wake-on-PCI activity, and implements a sleep mode that shuts down external devices and self-refreshes the SDRAM. PLL support and 1/6 modes as well as a stick register (PCI clock/10) for constant clock reference are also available.

Development tools: Forte Developer products deliver an integrated environment that provides a full set of graphical tools to create and maintain C, C++, and Fortran applications.

SuperH

THE SH-4 IS A 32-BIT, RISC-PROCESSOR core, targeting automotive, digital consumer, and residential gateway markets. It features a 16-bit fixed-length instruction set for code efficiency. The 266-MHz SH-4 core features a single- and double-precision IEEE754-compliant floating-point unit. The FPU can make four single-precision vector/matrix calculations for handling floating-point signal-processing algorithms and 3-D graphics in gaming and car-navigation applications.

SuperH bases the ST40 family on the SH-4 CPU core; it uses the SuperHyway internal interconnect bus for optimal bandwidth usage. Devices feature a PCI-bus v2.2 running at 66 MHz, and two memory interfaces—one 64-bit high-speed memory interface supporting DDR at 100 MHz for code and data, and one 32-bit peripheral interface supporting all kinds of flash chips, configurable SRAM, and peripheral access. A five-channel DMA engine serves all these interfaces.

The SH-5 is a 64-bit RISC core with a floating-point unit, SIMD (single-instruction, multiple-data) instructions, and on-chip-debugging capabilities. The SH-5 implements two operating modes. The SHmedia mode is a 32-bit encoded fixed-length instruction set that delivers multimedia performance for integer, packed-arithmetic/SIMD, and floating-point operations. The SHcompact mode is a 16-bit encoded fixed-length instruction set for higher code density for integer and floating-point operations. Users can switch on the fly between the two modes. SIMD core instructions operate on three operands; each may have eight 8-bit, four 16-bit, or two 32-bit values. This configuration addresses requirements for processing visual images or

audio data. The system can sustain a maximum throughput of 9.6 GOPS.

The SuperHyway is a VSI (Virtual Socket Interface)-compliant SOC (system-on-chip) interconnect that provides an on-chip communication option that you can tailor for different cost/performance implementations. In its simplest form, it can be a single 8- to 64-bit wide bus for basic peripherals. For more complex systems, it can support a memory-mapped, packet-based split-transaction protocol that achieves 3.2 Gbytes of bandwidth when operating at 200 MHz. SHdebug link is an on-chip module and associated software tool chain that allows engineers to nonintrusively analyze system behavior inside an SOC design. It allows them to trace execution flow, set watch points, and monitor on-chip CPU core and SuperHyway traffic.

Development support: SuperH partners with about 50 third-party companies to provide SuperH-core licensees with tools and complementary IP (intellectual property), such as libraries, silicon design, modeling verification, and testing. SuperH microprocessor cores are delivered as either soft or hard IP, and Mentor Graphics and Verisity provide support for industry-standard environments. Hitachi, ST Microelectronics, and UMC provide a choice of silicon manufacturers. RTOSs and kernels include WinCE, Linux, and Tornado. Partners also provide compilers, debuggers, development boards, emulators, application software, and middleware. Design services are available. STMicroelectronics offers proprietary hardware and software tools for product evaluation and fast prototyping for the ST40RA family of devices.

Tensilica

TENSILICA'S XTENSA IS A 32-BIT RISC SYNTHESIZABLE processor architecture targeting high-volume, embedded applications. Designers use the Xtensa Processor Generator to configure and extend a family of core processors with special functions developed for their designs, while doing concurrent software development and testing. The Xtensa Processor Generator allows broad freedom in hardware design and provides a choice of two software tool suites—Gnu-based GCC (Gnu C Compiler) or Xtensa XCC (Xtensa C Compiler)—to match each optimally configured processor. Each new processor configuration automatically creates the software-development environment, the instruction-set simulator, the bus functional model, the RTOS OSKit, DSP libraries (for Vectra), EDA tool scripts, and the XTMP (Xtensa Multiprocessor) system-modeling API. Developers create new designer-defined instructions using Xtensa's TIE (Tensilica Instruction Extension) compiler. Optional blocks include configurable Vectra DSP units, floating-point units, MMUs, and multiplier blocks.

Development support: A full standard set of Gnu software-development tools support development for the Xtensa processor and includes the GCC, linker, assembler, profiler, and GDB (Gnu debugger) and DDD (Data Display Debugger). Tensilica automatically supplies a configured instruction-count-accurate instruction-set simulator for each configuration of the Xtensa processor. This Xtensa software-development environment uses the same database as the processor's hardware description. The Processor Generator simultaneously generates the hardware description, software-development tools, and documentation.

Tensilica offers an optional compiler, the Xtensa C/C++ Compiler, as well as Mentor Graphics XRay for Xtensa Debugger, optimized for multiple-processor SOC (system-on-chip) designs. Tensilica offers the Xtensa Modeling Protocol, a multiple-processor simulation API to support multicore SOCs. Third-party integrated-development environments and operating systems are available, such as the Tornado development environment from Wind River, and the Nucleus Plus UDB and EDE (embedded development environment) from the ATI Division of Mentor Graphics.

Texas Instruments

THE MSP430X SERIES OF DEVICES ARE 16-bit RISC microcontrollers. MSP430x1xx derivatives include a range of in-system-programmable devices with 1 to 60 kbytes of flash, a 12-bit ADC, a multiplier, USARTs, and 10 PWM channels. MSP430x3xx derivatives include a range of devices that provide a segment-type LCD driver and offer one-time programmability for low-volume and factory-masked ROM. These devices target high-volume OEMs that ultimately require cost-effective ROM. MSP430x4xx derivatives include a range of in-system-programmable flash devices that integrate a segment-type LCD driver and can operate in a standby mode with a real-time-clock function active at less than 1 μ A. The MSP430x4xx family targets portable battery-powered measurement applications that require an LCD.

These devices include an asynchronous clock system that supports two external crystals and a third independent on-chip digitally controlled oscillator that enables start-up and synchronization in less than 6 μ sec. This approach allows an MSP430 to extensively remain in low-power standby modes and quickly respond to interrupt-driven events. In many applications, a single 32-kHz watch crystal with the on-chip digitally controlled oscillator is sufficient for low-rate operation.

Development support: Texas Instruments' flash-emulation tool supports development and uses an integrated-development environment to access the device's on-chip JTAG port for in-circuit emulation. The tools support peripheral access, programming, single-stepping, breakpoints, and full-speed operation. IAR provides a C compiler, and Hitex provides an in-circuit emulator. Evaluation kits are available for all MSP430x3xx devices.

Toshiba America Electronic Components

THE 8-BIT TLCS-870 FAMILY INCLUDES MORE THAN 80 devices with a variety of peripheral options. It maintains a 500-nsec minimum execution time and includes a register configuration that contains 16 banks of eight, 8-bit registers. The TLCS-870/X family builds on the TLCS-870 with faster execution at 250 nsec and an external memory bus capable of addressing a 1-Mbyte linear address space. Devices in the TLCS-870/X family are available with as much as 96 kbytes of on-chip ROM and 2 kbytes of RAM. Toshiba's newest family, the TLCS-870/C, combines the faster operation of the TLCS-870/X with a register architecture optimized for the use with the C-language.

Toshiba's 16-bit product offerings consist of four TLCS-900 core processors. All families provide dynamic bus sizing from external memory access and can access as much as 16 Mbytes. The register model includes four banks of eight, 16-bit registers for real-time processing, which you can access as 32-bit registers. The TLCS-900 and TLCS-900/L families have a minimum execution time of 200 nsec, and the TLCS-900/H and TLCS-900/L1 offer minimum execution times of 160 nsec for higher performance applications.

The TX19 is a MIPS-based, 32-bit RISC microprocessor core that delivers the compact code associated with a 16-bit instruction set. It is based on the MIPS I/MIPS32 instruction-set architecture and supports the MIPS 16e ASE instructions. It features an 8 \times improvement for interrupt acknowledgement. It employs a five-stage pipeline and implements a single-cycle 32-bit multiply-and-add operation.

The TX39 MIPS-based RISC processor is available as a core for ASIC designs and as an integrated standard product. The TX39 core includes a high-performance instruction and data cache and a one-cycle MAC (multiply accumulate). It features functions and instructions for real-time, on-silicon-debugging support, reduced code size, and improved performance with branch-likely instructions, hardware-interlock functions, and increased real-time capability using a cache-lock function.

The low-power TX49 64-bit, MIPS-based RISC processor is available as a standard product or as a core for ASIC designs. It employs five-stage pipelining; has 32 64-bit general-

purpose registers; and includes a nonblocking load function that allows the processor to execute instructions that follow while refilling the cache.

Development support: Toshiba and leading third-party development-tool vendors offer a range of tools to support designing with the TX System RISC Series of 32- and 64-bit microprocessors. Third-party support includes compilers, operating systems, debugging tools, and simulators. A Toshiba family of compilers, linkers, assemblers, and debuggers and a build manager supports Toshiba's CISC TLCS-870 and TLCS-900 family of processors. Third-party simulator support is also available.

Transmeta

THE X86-COMPATIBLE CRUSOE TM5800 and TM5500 microprocessors target handheld- and mobile-computing applications. Low-power operation relies on Code Morphing, a software process that dynamically translates x86 instructions into VLIW (very-long-instruction-word) instructions for the underlying Crusoe hardware engine. The Code Morphing software resides in flash ROM and is the first application to launch when you power up the Crusoe processor. Upon completion of Code Morphing's initialization, other system software components, such as the BIOS and operating system, load in traditional fashion.

Transmeta's LongRun power-management technology allows Code Morphing software to adjust Crusoe's voltage and clock frequency on the fly, depending on the demands that software places on the Crusoe processor, resulting in reduced power consumption. The Code Morphing software implements LongRun policies, which continuously scale both the frequency and the voltage of the Crusoe processor according to the instantaneous demands of the computer system. It can detect scenarios based on runtime performance information and then, transparently to the user, adapt its power usage accordingly.

Triscend

THE TRISCEND E5 CONFIGURABLE-SOC (system-on-chip) family comprises five accelerated, 8051-based microcontrollers, which vary in their amount of on-chip programmable logic, RAM, and I/Os. The A7 configurable-SOC family is similar to the E5, except that it uses the 32-bit ARM7TDMI processor core. The A7 supports 16-bit instructions in the Thumb state for higher code density. These devices target embedded applications that demand high levels of customization and are compatible with third-party tools that support their respective core architectures—from code development to in-system, real-time debugging. They support programmable power-management modes to control power consumption.

Development support: Designers customize the SOC peripherals with the Triscend FastChip development system using a drag-and-drop method, enabling the creation of 8051 or ARM7 derivatives on demand. Designers select the desired soft peripheral and then "drag" it into place around the processor. FastChip automates the rest of the process so that code development can proceed without you needing to worry about the implementation details of the soft peripheral.

These devices are compatible with third-party tools that support their respective core architectures. Both families have an on-chip JTAG interface and a hardware-breakpoint unit for dedicated in-system debugging. The E5 supports integration with Keil Software's uVision2. The A7 includes advanced debugging support via Wind River's VisionProbe II and VisionClick source-level debuggers, which provide visibility into the ARM7TDMI core and into the on-chip programmable logic. The SRAM can double as a trace buffer during debugging. Triscend offers hardware/software-development boards, low-level drivers, and board-support packages for eCos, Nucleus, and VxWorks.

Ubicom

THE HEART OF THE IP2022 IS A 100-MIPS RISC engine that integrates on-chip high-speed flash memory and SRAM. Two full-duplex serializer/deserializers decode data over a variety of high-speed communication interfaces to support LAN bridging and gateway applications. Implementing traditional hardware functions in software, the device supports in-system programming and reprogramming using prebuilt software modules and configuration tools, including device programming over the network. The IP2022 includes a sleep capability with a watchdog timer and a multi-input wakeup, supports 32-kHz oscillator operation, and can change the clock speed on the fly via a speed instruction. The speed instruction changes the processor execution speed on the fly by dividing down the core clock by factor of one to 128.

Development tools: Ubicom provides a software-development kit that includes a variety of prebuilt ipModule-software functions, including Ethernet MAC (media-access controller)/physical-layer and TCP/IP stack modules, USB, and multichannel UARTs. These software ipModules are typically communications-centric and use on-chip, hardware-assisted peripheral blocks or general-purpose-I/O pins to implement additional peripheral features. Ubicom offers the Unity integrated-development environment, which includes the GnuPro tool chain from Red Hat, a software-development kit with an application-configuration tool, OS support, a development board, and an in-system programming/debugging dongle.

Xemics

THE XE8000 SERIES OF MINIATURE MICROCONTROLLERS offers mixed-signal peripherals, including a 16+10-bit zooming ADC and 16-bit signal DACs. They consume as little as 200 μ A at 1 MIPS and have a flash memory with retention of 100 years at 55°C.

Development support: Xemics SA has launched a new version of the XE8000 ProStart kit that includes hardware- and software-development tools, including an integrated-development environment with C compiler, assembler, in-socket-debugger, linker, and simulator. The ProStart II contains a multipurpose programming board with a serial interface to a PC for program download and for RS-232 communication with the application. It also contains an evaluation board with a zero-insertion-force socket, buttons for signal input, LEDs for signal output, Xtal, and access to all circuit pins.

Xilinx

THE MICROBLAZE IS A 900-LOGIC-CELL, soft 32-bit RISC processor core that you can embed into any of the Virtex-architecture FPGAs from Xilinx, such as Virtex-II, Virtex-E, Spartan-II, and Spartan-IIe. It has a 32-bit data path and uses hard embedded features, such as multipliers, to increase performance. The core is available as part of the embedded-development kit along with a list of peripheral IP (intellectual-property) cores, such as UARTs, general-purpose I/O, SPIs, timers/counters, and watchdog timers. Xilinx's IP interface helps developers integrate standard, custom, and third-party IP into the CoreConnect bus. Developers can parameterize their peripherals with only the features they require for their design using the software available in the embedded development kit.

The IBM PowerPC is a hard 32-bit RISC-processor core available in several members of the Virtex-II PRO family, with as many as four PowerPC cores on the same FPGA. The PowerPC comes with a 32-bit data path and 16 kbytes each of instruction and data cache. It has a five-stage data-path pipeline, an embedded MMU, 32 \times 32-bit general-purpose registers

that support multiplication or division, and dedicated on-chip memory interfaces. Standard peripheral support includes UARTs, general-purpose I/O, SPI, I²C, and high-performance cores, such as a 10/100-Mbps Ethernet MAC. The IBM CoreConnect Bus is the interface between the processor core and the other blocks of the processor subsystem and is capable of a 2.1-Gbps bandwidth on the high-speed-processor local bus.

Development support: The MicroBlaze and PowerPC processors use the IBM CoreConnect technology as the interconnect bus. Xilinx offers the Embedded Development Kit, which includes Gnu tools, the System Generator for either processor, processor IP, simulation, other utilities, and software to aid the design process. This set of tools is available for an introductory price of \$495. The standard set of peripherals operates with either core. Wind River provides a Xilinx version of its development tools and operating system for PowerPC designs that includes the DIAB C/C++ compiler, SingleStep Trace Debugger, and vision-Probe hardware debugger.

Zilog

THE Z8 ENCORE! FAMILY OF MICROCONTROLLERS uses an 8-bit eZ8 CPU and introduces flash memory to Zilog's line of 8-bit microcontrollers. The eZ8 processor is upward-compatible with Z8 instructions. With as much as 64 kbytes of flash memory, the device can change, update, and reprogram software code during development and into production. The processing environment includes a 12-channel, 10-bit ADC, an on-chip debugger, and as many as 24 interrupts. The three-channel DMA controller supports direct peripheral-to-memory swaps with minimal CPU interruption.

The eZ80 family of microprocessors implements a pipeline architecture operating at 50 MHz maximum. Improving on the Z80 architecture by using single-cycle instruction fetch, the eZ80 can operate in Z80-compatible (64-kbyte) mode or in full 24-bit (16-Mbyte) addressing mode.

The latest addition to the eZ80 family is the eZ80 Webserver-I, which includes power-management modes and peripheral power-down controls, IrDA-compatible Infrared Encoder/Decoder, DMA-like eZ80 instructions, a glueless external memory interface with four chip selects, and a JTAG and ZiLOG debugging interface.

Development support: The Z8 Encore! Development Kit, Z8ENCORE000ZCO, contains an evaluation board, PC-to-target interface module, serial cable to on-chip debugger, and power supply. The ZDS II integrated development environment includes a new suite of low-level tools, including a C compiler, a full runtime library, an assembler, a linker, a librarian, a ZDB (Zilog debugger) target-module interface-board communication interface, sample code, and device drivers. The eZ80 Development Platform allows users to experience the eZ80's capability and operation. The eZ80 Webserver-i microprocessor powers the latest development kit, the eZ80 Webserver-i E-NET Module, which includes the ZPAK II debugging interface module, ZDS II integrated-development environment, and 10 BaseT Ethernet hub.