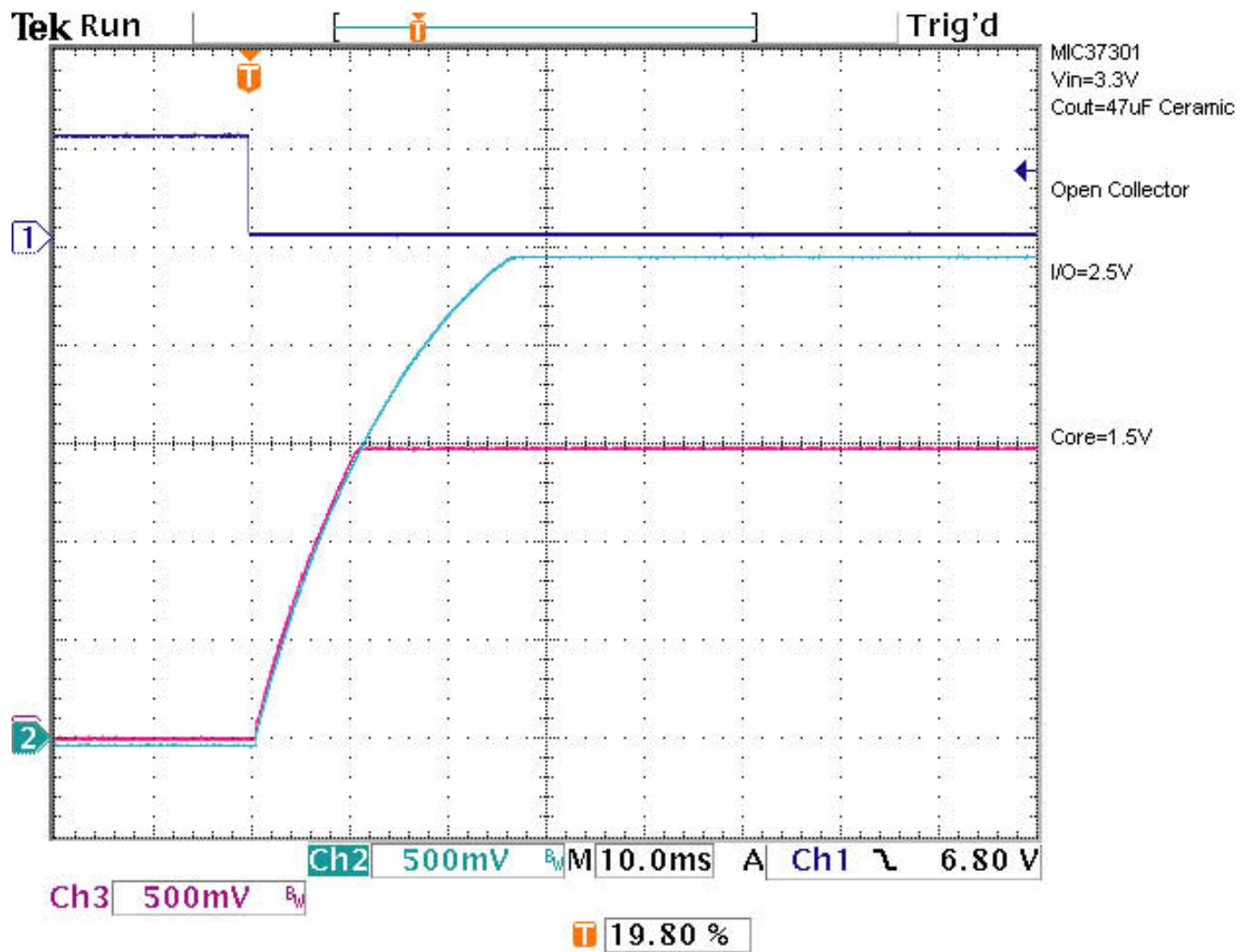


Figure 4



The I/O and core voltages have controlled rise times during the power-on phase.