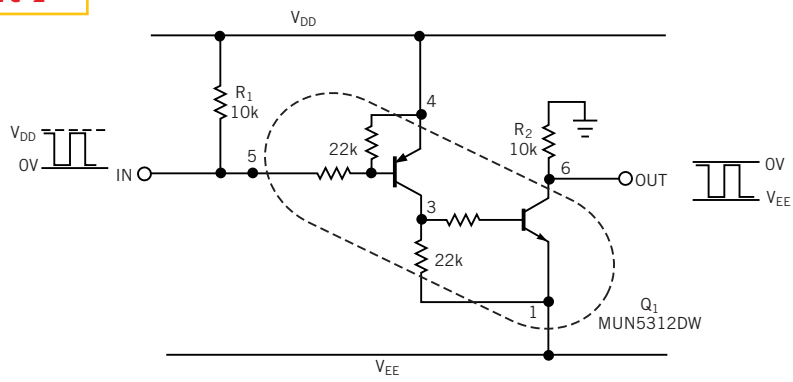


Figure 2



This transistor arrangement level-shifts the data or clock signals from positive to negative levels.