

FEEDING AND READING AN AVALANCHE PHOTODIODE TAKES A HIGH DEGREE OF CIRCUIT SOPHISTICATION.

Bias-voltage and current-sense circuits make avalanche photodiodes work

APDs (avalanche photodiodes) or APDs, are common components in laser-based fiber-optic systems for converting optical data into electrical form. The bias voltage and current measurement requirements constitute a significant design challenge, and common circuit approaches do not meet APD signal-conditioning requirements. More sophisticated techniques are necessary, particularly with any additional performance requirements for high-accuracy, low-noise, and digital outputs.

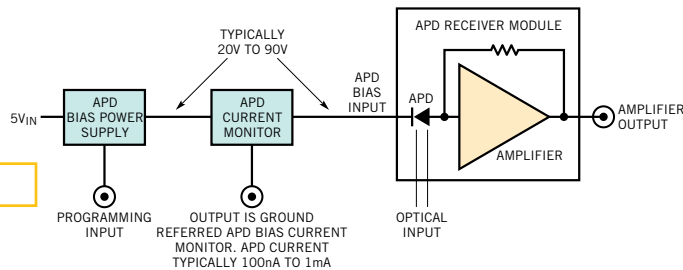
The usual APD package includes a signal-conditioning amplifier in a small module (**Figure 1**). The APD module contains the APD and a transimpedance (current-to-voltage) amplifier. An optical port permits interfacing fiber-optic cable to the APD's photosensitive portion. The module's compact construction facilitates a direct, low-loss connection between the APD and the amplifier, which is necessary because of the extremely high-speed data rates involved.

The receiver module needs support circuitry. The APD requires a relatively high voltage bias—typically, 20 to 90V—to operate. The bias supply's programming port sets this voltage. This programming voltage may also include corrections for the APD's temperature-dependent response. Additionally, it is desirable to monitor the APD's

average current, which indicates optical signal strength. Feedback techniques can combine this information to maintain optical-signal strength at an optimal level. The feedback loop's operating characteristics can also determine whether deleterious degradation of optical components has occurred, permitting the circuit to take corrective measures. APD current is typically 100 nA to 1 mA, a dynamic range of 10,000 to 1. This measurement, which requires accuracy of at least 1%, normally must occur in the APD's "high side," which complicates the circuit design. This restriction applies because the APD's anode is committed to the receiver amplifier's summing point.

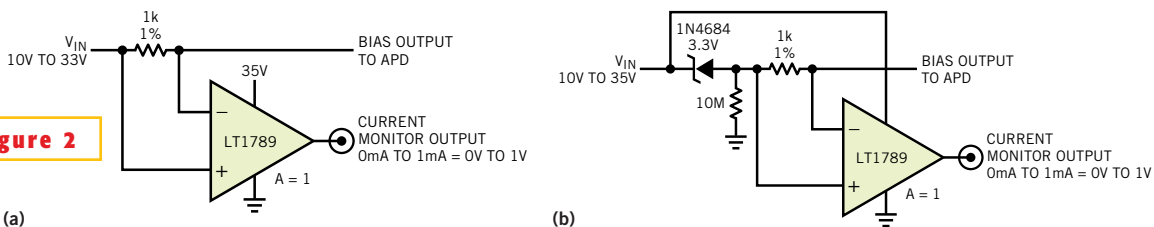
The APD module, an expensive and electrically delicate device, requires protection from damage under all conditions. The support circuitry must never produce spurious outputs, which could destroy the APD module. You must devote particular attention to the bias supply's dynamic

Figure 1



A typical APD module contains an APD, an amplifier, and an optical port. A power supply provides APD bias voltage, and an APD current monitor operates at a high common-mode voltage, complicating signal conditioning.

Figure 2



Instrumentation amplifiers extract current measurements from modest common-mode voltages but have limitations. One approach requires separate amplifier power and bias-supply connections (a); a similar approach derives both connections from a single point (b).

response under programming and power-up and -down conditions. Finally, it is desirable to power the support circuitry from a single 5V rail.

SIMPLE CURRENT MONITORS HAVE PROBLEMS

Straightforward approaches attempt to address the current-monitor problem (Figure 2). An instrumentation amplifier powered by a separate 35V rail measures current across the 1-kΩ shunt resistor (Figure 2a). A similar circuit derives its power supply from the APD bias line (Figure 2b). Although both approaches function, they do not meet APD current-sensing requirements. APD bias voltages can reach 90V, exceeding the amplifier’s supply and common-mode-voltage limits. Additionally, the measurement’s wide dynamic range requires the single-rail-powered amplifier to swing within 100 μV of zero, which is impractical. Finally, it is desirable for the amplifiers to operate from a single, low-voltage rail.

An alternative circuit divides down the high common-mode current-shunt voltage, theoretically permitting the 5V-powered amplifier to extract the current measurement over a 20 to 90V APD bias range (Figure 3). In practice, this arrangement introduces prohibitive errors, primarily because the circuit also divides down the desired signal. The current-measurement information is buried in the divider resistor’s tolerance, even with 0.01% components. The circuit can-

not achieve the desired 1% accuracy over a 100-nA to 1-mA range. Finally, although the amplifier operates from a single 5V supply, it cannot swing all the way to zero.

AC-carrier-modulation techniques help to meet APD current-monitor requirements (Figure 4). This circuit features 0.4% accuracy over the sensed current range, runs from a 5V supply, and has the high-noise-rejection characteristics of carrier-based “lock-in” measurements. Such measurements modulate the desired signal on a carrier, effecting narrowband amplification with extremely high out-of-band rejection.

An internal oscillator clocks the LTC1043 switch array. Oscillator frequency, set by the 0.56-μF capacitor at pin 16, is approximately 150 Hz. S₁ clocking biases Q₁ via level shifter Q₂. Q₁ chops the dc voltage across the 1-kΩ current shunt, modulating it into a differential square wave signal, which feeds instrumentation-amplifier IC₁ through 0.2-μF ac coupling capacitors. IC₁’s single-ended output biases demodulator S₂, which presents a dc output to buffer amplifier IC₂. IC₂’s output is the circuit output.

Switch S₃ clocks a negative-output charge pump that supplies the amplifier’s V – pins, permitting output swing to 0V

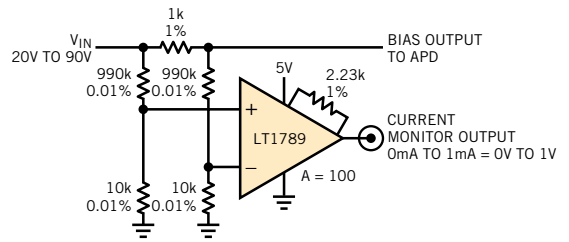


Figure 3 Dividing down the high-common-mode voltage introduces huge errors, even with precision components, making this approach impractical.

and below. The 100-kΩ resistors at Q₁ minimize its on-resistance error contribution and prevent destructive potentials from reaching IC₁ (and the 5V rail) if either 0.2-μF capacitor fails. IC₂’s gain of 1.1 corrects for the slight attenuation introduced by IC₁’s input resistors. In practice, it may be desirable to derive the APD bias voltage regulator’s feedback signal from the indicated point, eliminating the 1-kΩ shunt resistor’s voltage drop (see sidebar “Low-error feedback-signal-derivation techniques”). Verifying accuracy involves loading the APD bias line with 100 nA to 1 mA and noting output agreement. Appropriate high-value load resistors, perhaps augmented with a monitoring current meter, are available from Victoreen (www.ohmite.com/victoreen/) and other suppliers. Tight resistor tolerance, although convenient, is not strictly necessary because the current-meter indication sets the output target value.

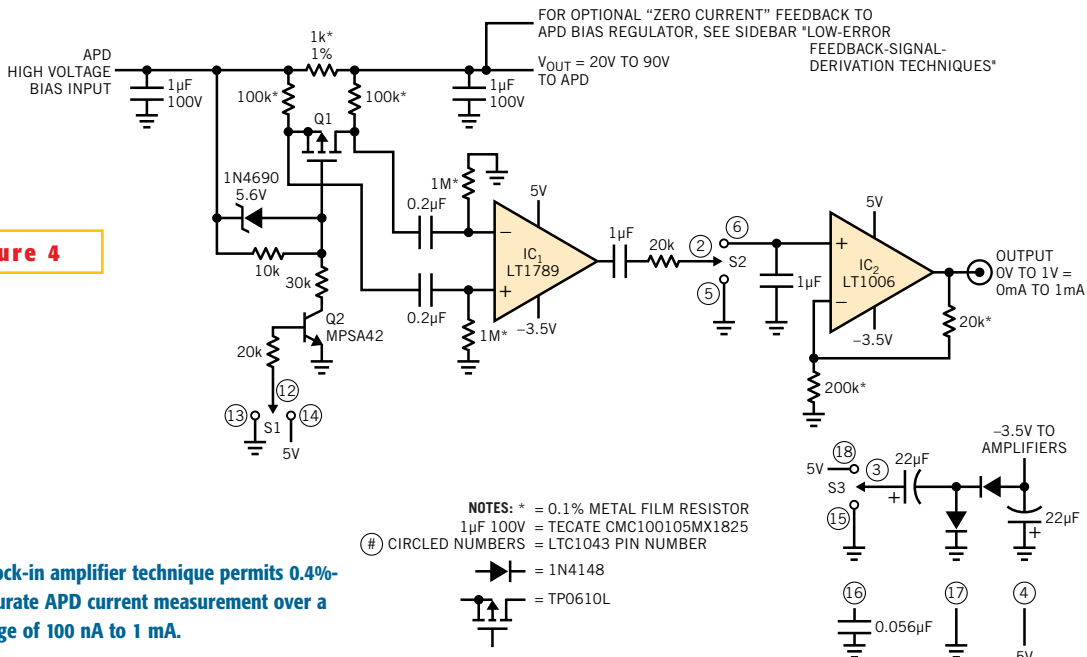


Figure 4

A lock-in amplifier technique permits 0.4%-accurate APD current measurement over a range of 100 nA to 1 mA.

- NOTES: * = 0.1% METAL FILM RESISTOR
 1μF 100V = TECATE CMC100105MX1825
 # CIRCLED NUMBERS = LTC1043 PIN NUMBER
 = 1N4148
 = TP0610L

A dc-coupled current monitor is simple but pulls more current from the APD bias supply (Figure 5). IC₁ floats, powered by the APD bias rail. The 15V zener diode and current source, Q₂, ensure that IC₁ never is exposed to destructive voltages. The 1-kΩ current shunt's voltage drop sets IC₁'s positive input potential. Feedback via Q₁ to the negative input balances the inputs of IC₁. As such, Q₁'s source voltage equals IC₁'s positive input voltage, and its drain current sets the voltage across its source resistor. Q₁'s drain current produces a voltage drop across the ground-referred 1-kΩ resistor identical to the drop across the 1-kΩ current shunt and, hence, the APD current.

This relationship holds across the 20 to 90V APD bias-voltage range. The 5.6V zener diode assures IC₁'s inputs are always within their common-mode operating range, and the 10-MΩ resistor maintains adequate zener current when APD current is at very low levels.

Two output options are possible. IC₂, a chopper-stabilized amplifier, provides an analog output. Its output can swing to zero or lower because its V₋ pin is supplied with a negative voltage. To generate this potential, IC₂'s internal clock activates a charge pump, which in turn biases IC₂'s V₋ pin. (Circuit veterans exercise extreme wariness when they confront this type of bootstrapped biasing

scheme (Reference 1).

A second output option substitutes an A/D converter, providing a serial-format digital output. This option requires no V₋ supply because, the LTC2400 ADC converts inputs to—and slightly lower than 0V.

Resistors at strategic locations prevent destructive failures. The 51-kΩ unit protects IC₁ if the APD bias line shorts to ground. The 10-kΩ resistor limits current to a safe value if Q₁ fails, and the 100-kΩ resistor serves a similar purpose if Q₂ malfunctions. As in Figure 4, the circuit can take APD voltage-regulator feedback at the current shunt's output to maintain optimal regulation (see sidebar “Low-error

LOW-ERROR FEEDBACK-SIGNAL-DERIVATION TECHNIQUES

Various circuits either detail or make reference to counteracting loading effects of the APD (ava-

lanche-photodiode) bias supply's output feedback divider. If the divider location is before the 1-kΩ

current shunt, the current monitor's output does not include its current drain, and the circuit incurs no error. A potential difficulty with this approach is that the 1-kΩ shunt appears in series with the bias supply's output, degrading load regulation. The maximum 1-mA shunt current produces a 1V output-regulation drop. In some cases, this drop is permissible, and no further consideration is necessary. Circumstances dictating tighter load regulation require compensation techniques.

shunt resides in the “high side.” Such arrangements involve high common-mode voltages, seemingly mandating a high-voltage buffer amplifier to isolate the divider's current loading. However, you can alternatively use standard low-voltage amplifiers to process high-voltage signals (Figure B). IC₁, sensing after the 1-kΩ shunt, isolates the feedback divider's loading while permitting the APD bias regulator to include the shunt within its feedback loop.

The bias regulator's high-voltage output directly powers IC₁, but the zener diode clamps the IC's V₋ pin with respect to its V₊ pin. Current sink Q₁ maintains this bias over the range of possible APD-regulator outputs. Although IC₁ processes high-voltage signals, the circuit holds the voltage across it to safe levels. The 5.6V zener diode in the APD bias line ensures that IC₁'s inputs are always inside their common-mode operating range. The 10-MΩ resistor maintains adequate zener-diode bias when APD currents are extremely low. A 51-kΩ resistor protects IC₁ from destructive high voltage if the APD bias output shorts to ground. Similarly, the 100-kΩ resistor prevents high voltage from appearing on the 5V supply if Q₁ fails.

When the shunt is in a transformer's return path (“low-side shunt”), you can cancel divider error by introducing a compensatory term into the APD current-monitor circuitry (Figure A). This scheme prevents the output-voltage divider's current-loading error from appearing in IC₁'s output by feeding forward a compensatory current from the APD bias-programming input. The circuit scales the compensating current, arriving at IC₁ via R_{LARGE} to precisely balance out the portion of shunt output that the voltage divider's loading error contributes.

The situation differs when the

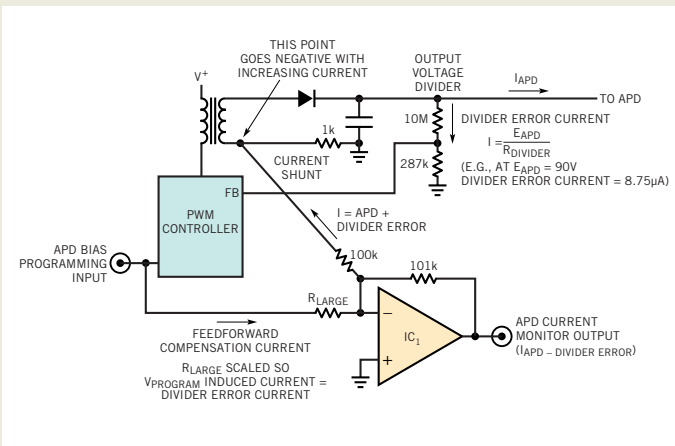


Figure A Feedforward from the programming input compensates for the output voltage divider's current-loading error.

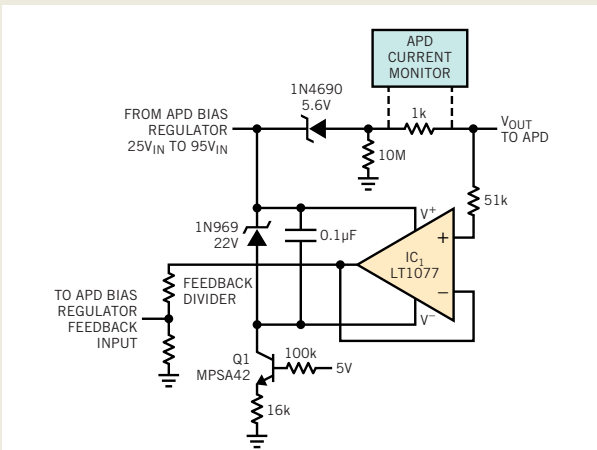


Figure B IC₁'s follower floats from a high-voltage rail and eliminates feedback-divider current-loading error.

feedback-signal-derivation techniques). This circuit requires no trimming and maintains 0.5% accuracy. It does, however, pull current approximately equal to the current delivered to the APD, in addition to Q_2 's collector current. This current can be an issue if the APD bias supply has restricted current capability.

All these examples are current monitors. The circuit in **Figure 6a**, which Linear Technology application engineer Michael Negrete developed is a high-voltage APD bias supply (Reference 2). The LT1930A switching regulator and L_1 form a flyback-based boost stage. The flyback events pump a diode-capacitor network tripler, producing a high-voltage dc output. Feedback from the output via the R_1 - R_2 combination stabilizes the regulator's operating point. D_6 and D_7 protect the switch and feedback pins, respectively, from parasitic negative excursions, and the 10Ω resistors prevent excessive switch current. C_8 and C_9 , series-connected for high-voltage capability, minimize output noise. A 0 to 4.5V programming voltage results in a corresponding 90 to 30V output with 3% accuracy and approximately 2 mA of current capacity.

Circuit output noise is quite low (**Figure 6**). With 500 μ A loading at $V_{OUT} = 50V$, the ripple and harmonic residue in a 10-MHz bandwidth is approximately 200 μ V. This noise level is adequate for most APD receivers.

ADD A CURRENT MONITOR

Figure 7, named the Martin configuration for work by Alan Martin, an application engineer at Linear Technology, combines the previous circuit with **Figure 5**'s current monitor, providing a complete APD signal conditioner. The programmable APD bias supply is as before, except that

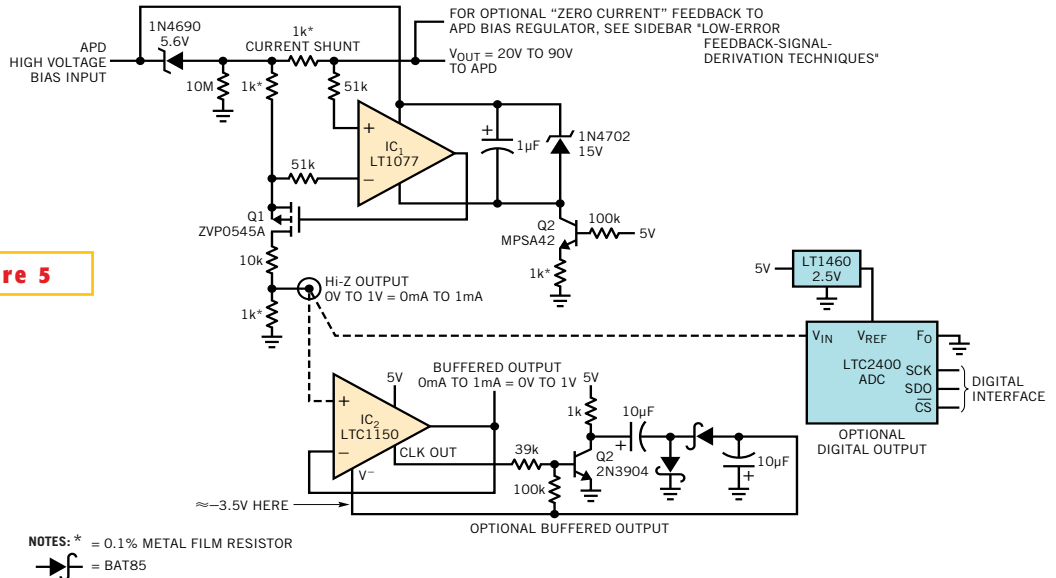


Figure 5

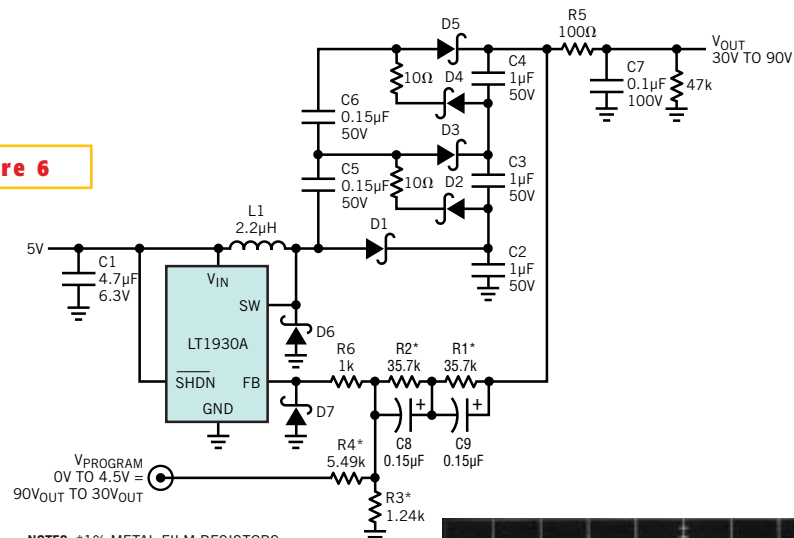
IC_1 and Q_1 float at the high-voltage rail and measure APD current to 0.5% via the 1-k Ω shunt. Q_1 's ground-referred drain current provides a high-impedance output, but you can also choose a buffered-analog or digital-output option.

feedback comes via IC_2 , IC_3 , sensing after the 1-k Ω current shunt, isolates the R_1 - R_2 path loading, preventing loading from influencing the shunt's voltage drop. IC_2 's action also ensures tight output regulation, despite the current shunt's presence (see sidebar "Low-error feedback-signal-derivation techniques").

The current monitor borrowed from **Figure 5** measures across the 1-k Ω current shunt, presenting its output in Q_1 's drain line. The output has an output impedance of approximately 1-k Ω , but you can also use one of **Figure 5**'s output options.

When considering circuit operation, note that the charge pump's high-voltage

Figure 6



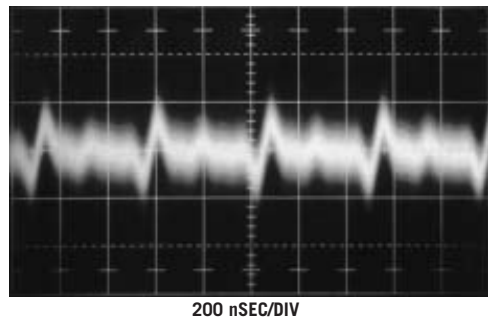
- NOTES: *1% METAL FILM RESISTORS
 C1: TAIYO YUDEN JMK212BJ475MG
 C2 TO C4: MURATA GRM42-2X7R105K050
 C7: TAIYO YUDEN HMK316BJ104ML
 C8, C9: VISHAY 695D154X9050AZ
 D1 TO D7: CENTRAL SEMI CMDSH2-3TR
 L1: MURATA LQH32C2R2M24

(a)

A boost regulator and charge pump supply APD bias of 30 to 90V (a) with only 200 μ V p-p ripple and harmonic residue in a 10-MHz bandwidth (b).

100 μ V/DIV
AC COUPLED

(b)



output powers both amplifiers, and the circuit returns its V^- pins to the “ $2/3 V_{OUT}$ ” point. This biasing permits the amplifiers to process high-voltage signals, although the voltage across them never exceeds 30V.

Another complete APD bias supply and current monitor uses techniques that differ from the previous example’s (Figure 8a). Advantages include 0.25% bias voltage and current-monitoring accuracy, compactness, and fewer high-voltage components for greater reliability. The LT1946 switching regulator and T_1 form a flyback-type boost configuration. T_1 ’s turn ratio provides voltage gain, and the diode and capacitor in T_1 ’s secondary winding rectify and smooth the high-voltage flyback events to dc. The circuit divides down this dc potential and feeds the resultant signal back to IC_1 . IC_1 compares this signal with the APD-bias programming input and sets

the LT1946’s operating point, closing a control loop. A local roll-off at IC_1 and a lead network across the 10-M Ω feedback resistor furnish loop compensation. This loop establishes and maintains the APD bias output in accordance with the programming input’s value. IC_3 , active at $V_{SUPPLY} = 1.2V$, prevents output overshoot at power turn-on by grounding the programming input command while forcing IC_1 ’s output low. This action shuts off the switching regulator, which then stops producing a high voltage. When turn-on power reaches approximately 4V, IC_3 changes state, and IC_1 ’s positive input ramps to the programming voltage. The switching regulator’s output follows this turn-on profile, and no overshoot occurs. The LT1004 clamps spurious programming inputs beyond 2.5V, preventing excessive high-voltage outputs. Optional circuitry allows input clamping at any desired voltage (see sidebar

“APD protection circuits”).

The circuit’s current-monitor portion takes full advantage of T_1 ’s floating secondary. Here, the 1-k Ω current shunt resides in T_1 ’s secondary return path (Pin 3), eliminating the high common-mode voltages that the previous “high-side”-sensed examples encountered. Circuit ground is at the shunt’s uncommitted terminal, meaning that Pin 3 of T_1 undergoes increasing negative excursions with greater APD current. Inverter IC_2 converts the shunt’s negative voltage to a buffered positive output. IC_2 ’s gain, which the circuit scales 1% above unity, compensates for the input resistor’s shunt-loading error. The circuit facilitates a voltage swing to zero by returning IC_2 ’s V^- pin to a small negative potential derived from the LT1946’s V_{SW} pin switching. A compensatory current from the APD bias-programming input prevents the 10-M Ω /287-k Ω divider’s current-loading er-

APD-PROTECTION CIRCUITS

APD (avalanche-photodiode)-receiver modules are electrically delicate and expensive devices. Thus, protection circuits may be of interest. Protection circuits can protect the APD module from bias-programming overvoltage error (Figure Aa), excessive current (Figure Ab), or destructive voltage (Figure Ac). In Figure Aa, Q_1 is normally off, and programming voltage passes to the bias-regulator voltage-programming input. Abnormally high inputs, defined by the potentiometer’s setting, cause IC_1 to swing low, biasing Q_1 and closing IC_1 ’s feedback loop. This situation causes Q_1 ’s emitter to clamp at the potentiometer wiper’s voltage, safely limiting the bias regulator’s programming input.

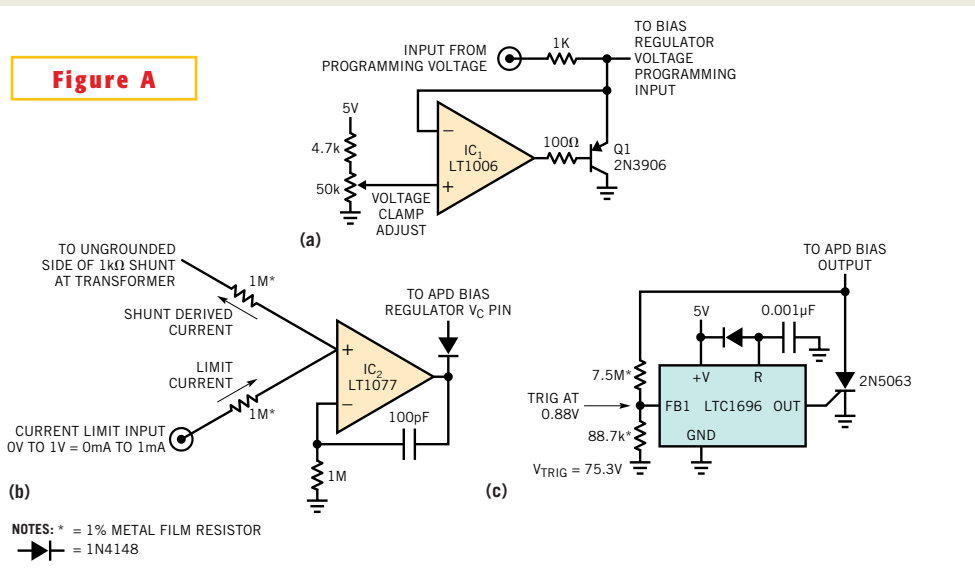
Figure Ab is an APD current limiter. The circuit works with “low-side” shunts in transformer-coupled APD supplies, such as in Figure 8a of the main text, although the technique is generally

applicable. As long as the shunt current’s absolute value is below the current limit point, IC_2 is saturated high, and the associated APD bias regulator functions normally. Shunt overcurrent forces IC_2 ’s output lower, pulling the regulator’s control pin (V_C) lower and limiting current. The 100-pF/1-M Ω combination stabilizes IC_2 , and the bias regulator

assumes the characteristics of a current source.

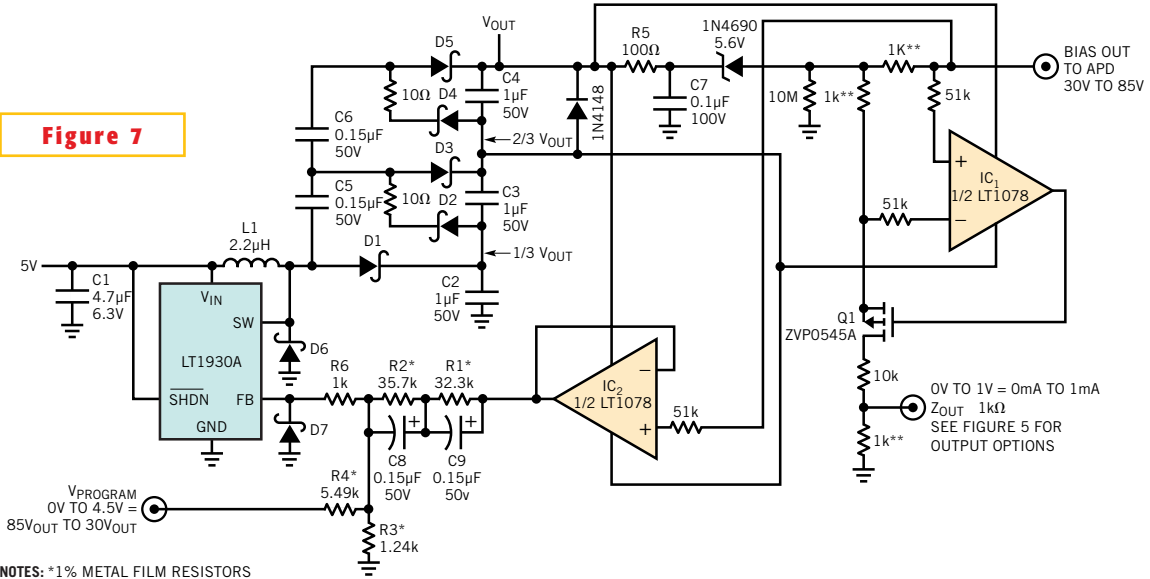
Figure Ac is an overvoltage protection crowbar. This circuit’s purpose is as the last line of defense against uncontrolled APD bias-supply high-voltage outputs. Normally, the LTC1696 crowbar IC is below its 0.88V trigger threshold, and the SCR is off. If the APD bias rises too high, the

LTC1696 triggers, firing the SCR. SCR turn-on “crowbars” the APD bias line, arresting the high voltage and maintaining a short across the line via its latch characteristic. If the APD bias supply has significant output impedance, prolonged SCR loading is not deleterious; if not, you should put a fuse in the bias supply line.



Protection-circuit options include a programming-voltage clamp (a), a current limiter (b), and a bias-voltage crowbar (c).

Figure 7



- NOTES:** *1% METAL FILM RESISTORS
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 C1: TAIYO YUDEN JMK212BJ475MG
 C2 TO C4: MURATA GRM42-2X7R105K050
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 D1 TO D7: CENTRAL SEMI CMDSH2-3TR
 L1: MURATA LQH32C2R2M24

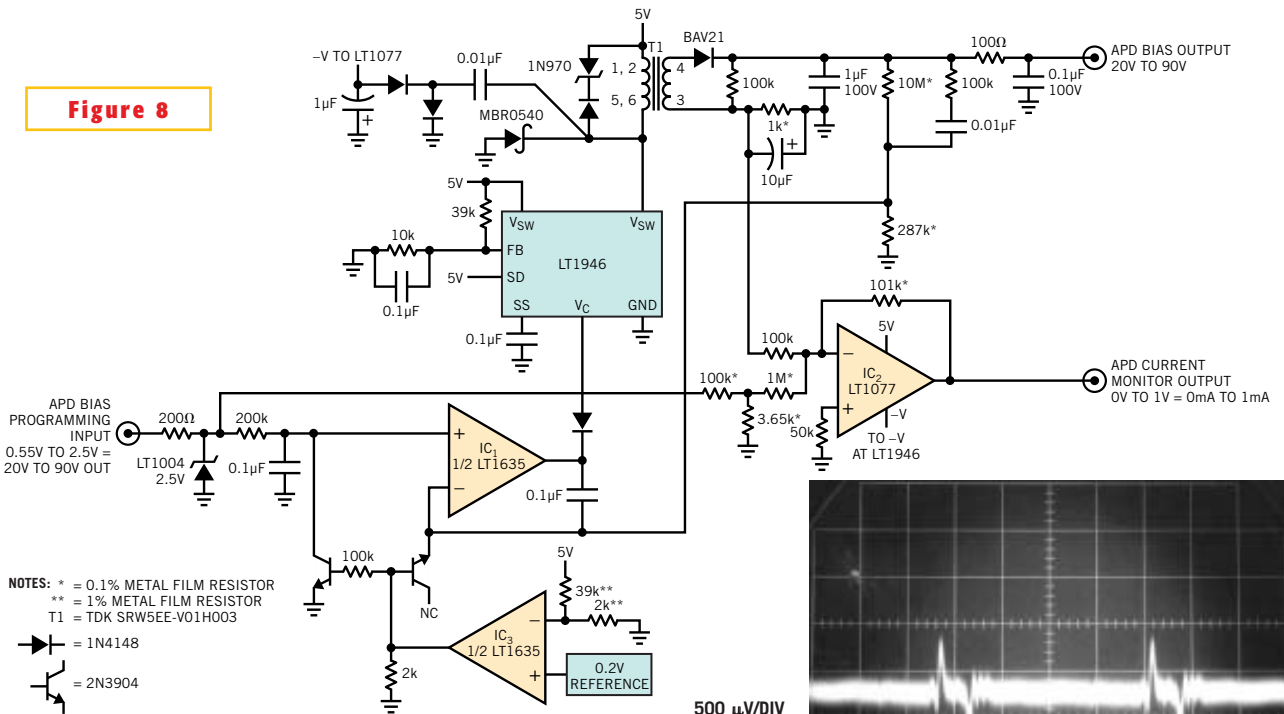
Figure 5's current monitor joins with Figure 6's bias supply to provide APD bias and 0.5% current measurement. IC₂ buffers the LT1930A's feedback-path loading from the bias supply's output, eliminating current error.

ror from appearing in IC₂'s output. The circuit scales this compensating current, arriving at IC₂ via the 100-kΩ/3.65-kΩ/1-MΩ resistor network, to precisely balance

out the shunt's output portion due to the 10-MΩ/287-kΩ path's loading error (see sidebar "Low-error feedback signal derivation techniques").

Output noise for this circuit is approximately 1 mV p-p in a 10-MHz bandwidth (Figure 8b). This noise level is characteristic of flyback regulators and somewhat

Figure 8

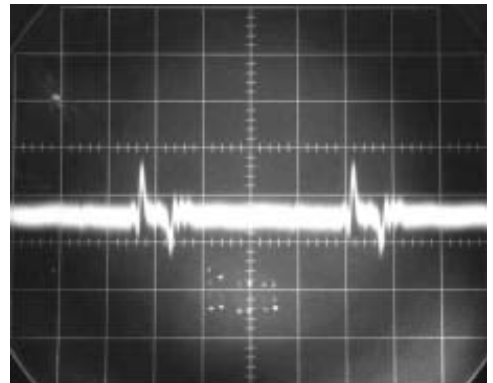


- NOTES:** * = 0.1% METAL FILM RESISTOR
 ** = 1% METAL FILM RESISTOR
 T1 = TDK SRW5EE-V01H003
 D1 = 1N4148
 D2 = 2N3904

(a)

IC₁ controls an LT1946 boost regulator to provide a bias supply of 20 to 90V (a). IC₂ senses APD current to 0.25% across the 1-kΩ shunt in T₁'s output return. Output noise measures 1 mV p-p in a 10-MHz bandwidth (b).

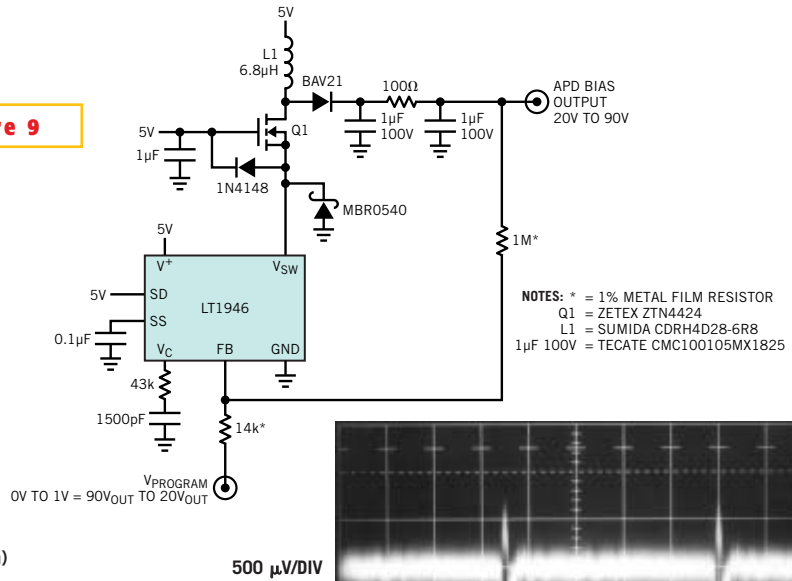
(b)



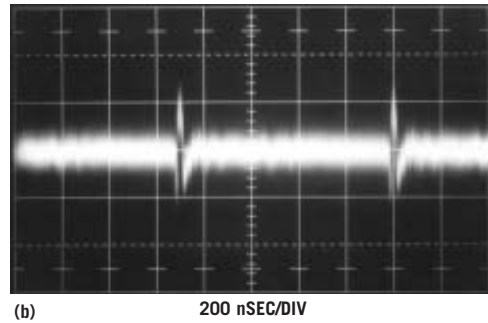
higher than **Figure 7**'s charge-pump-based arrangement. This noise is still acceptable for most APD receivers, although special switching-regulator techniques can considerably reduce this figure.

You can borrow from **Figure 8**'s flyback technique to form a simple, small-area APD bias supply (**Figure 9a**). This circuit provides only the bias supply and deletes **Figure 8a**'s current-monitor function. Additionally, a two-terminal inductor replaces **Figure 8a**'s transformer. The circuit is a basic-inductor flyback boost regulator with a single important deviation. Q_1 , a high-voltage device, sits between the LT1946 switching regulator and the inductor, which permits the regulator to control Q_1 's high-voltage switching without undergoing high-voltage stress. Q_1 , operating as a cascode with the LT1946's internal switch, withstands L_1 's high-voltage flyback events (**Reference 3**). The diodes associated with the source terminal of Q_1 clamp L_1 -originated spikes arriving via Q_1 's junction capacitance. The circuit rectifies and filters the high voltage to dc, forming the circuit's output. Feedback to the regulator stabilizes the output, which you can vary by appropriate biasing at the $V_{PROGRAM}$ input. Components at the LT1946's V_C pin compensate the loop. Over a 20 to 90V-output range, the circuit remains within 2% of the $V_{PROGRAM}$ input's dictated output voltage. Switching-related output noise is approximately 1.3 mV p-p in a

Figure 9



(a) Q_1 , in a cascode configuration with LT1946, controls L_1 switching to provide an APD bias output of 20 to 90V (a). Bias-supply noise in a 10-MHz bandwidth is approximately 1.3 mV p-p (b).

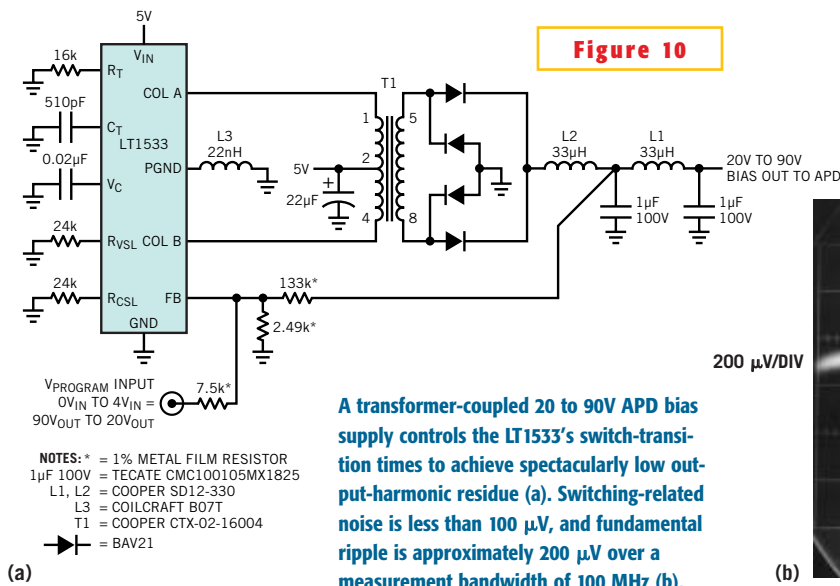


10-MHz bandwidth (**Figure 9b**).

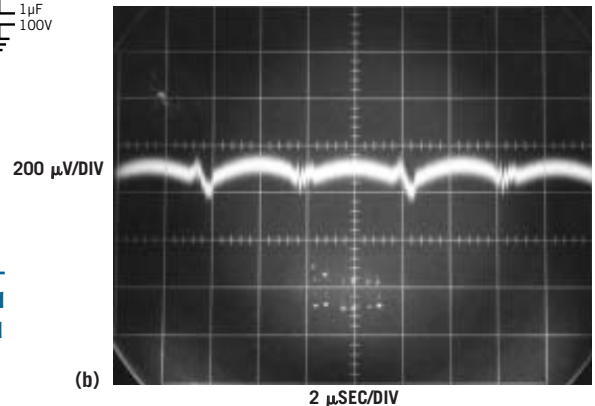
Some APD-receiver applications require extremely low noise in an extended bandwidth. An APD bias supply can use special switching regulator techniques to achieve 200- μ V noise in a 100-MHz bandwidth (**Figure 10a**). The LT1533 is a “push-pull” output-switching regulator with controllable switch-transition times. Slower switch transitions notably reduce output harmonic

content, or “noise.” Noise contains no regularly occurring or coherent components. As such, switching-regulator output noise is a misnomer. Unfortunately, undesired switching-related components in the regulated output are almost always called noise. Accordingly, although technically incorrect, this article refers to all undesired output signals as “noise” (**Reference 4**).

Resistors at the R_{CSL} and R_{VSL} pins con-



(a) A transformer-coupled 20 to 90V APD bias supply controls the LT1533's switch-transition times to achieve spectacularly low output-harmonic residue (a). Switching-related noise is less than 100 μ V, and fundamental ripple is approximately 200 μ V over a measurement bandwidth of 100 MHz (b).



control the switch current and voltage-transition times, respectively. In all other respects, the circuit behaves as a classical push-pull, transformer-based, step-up converter. The $V_{PROGRAM}$ input biases a feedback loop, setting the output at 20 to 90V.

The controlled transition times result in a dramatic decrease in output noise (Figure 10b). The ripple and switching-related residue of 200 μ V in a 100-MHz bandwidth is much less than that of conventional regulators, meeting the most stringent noise requirements.

You can build on the previous circuit's performance to form a complete, high-performance APD-signal conditioner (Figure 11). The bias supply is identical to Figure 10a's low-noise example, with the addition of the IC₁-based feedback buffer. This stage, similar to the one in Figure 7, isolates the regulator's feed-

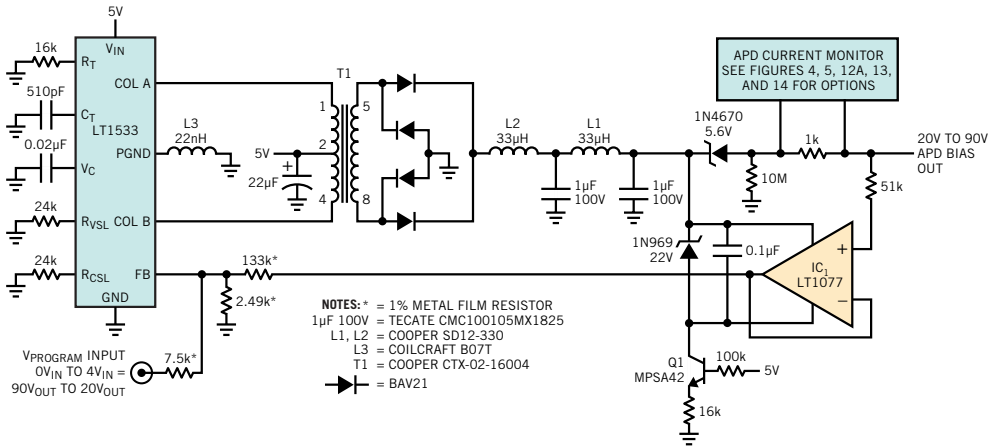


Figure 11 Augmenting Figure 10a with a feedback-divider buffer and a current monitor provides a complete APD signal conditioner with 100 μ V of noise.

back-path current from the 1-k Ω shunt, preserving current-monitor accuracy. IC₁'s zener-current source-power biasing scheme permits this amplifier to process high-voltage signals even though it is a low-voltage device (see sidebar "Low-error feedback-signal-derivation techniques"). You can select the current monitor for this circuit, which the schematic shows in block form, from many circuits, depending on requirements.

Some APD current-monitor applications call for high accuracy and stability. An unusual optical-switching-based approach achieves 0.02% accuracy over a sensed range of 100 nA to 1 mA (Figure 12a). This scheme measures shunt current by switching a capacitor using switches S_{1A} and S_{1B} across the shunt ("ACQUIRE"). After a time, the capacitor charges to the voltage across the shunt. S_{1A} and S_{1B} open, and S_{2A} and S_{2B}

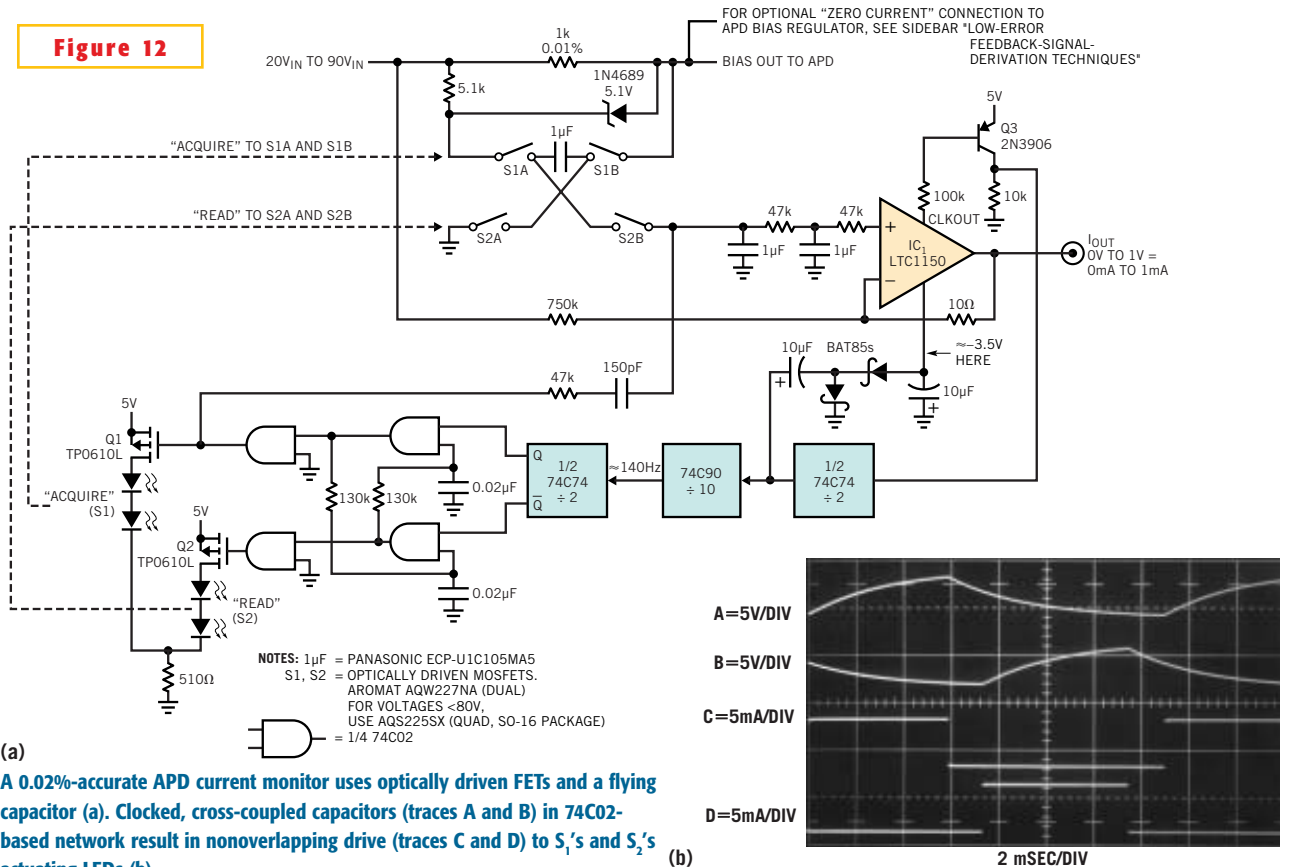


Figure 12 A 0.02%-accurate APD current monitor uses optically driven FETs and a flying capacitor (a). Clocked, cross-coupled capacitors (traces A and B) in 74C02-based network result in nonoverlapping drive (traces C and D) to S₁'s and S₂'s actuating LEDs (b).

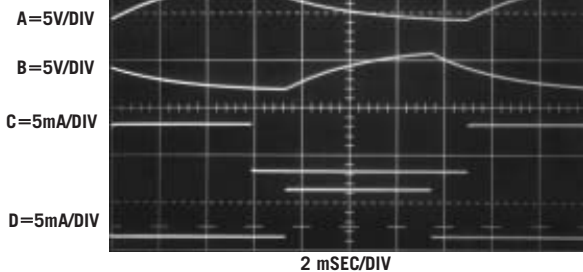
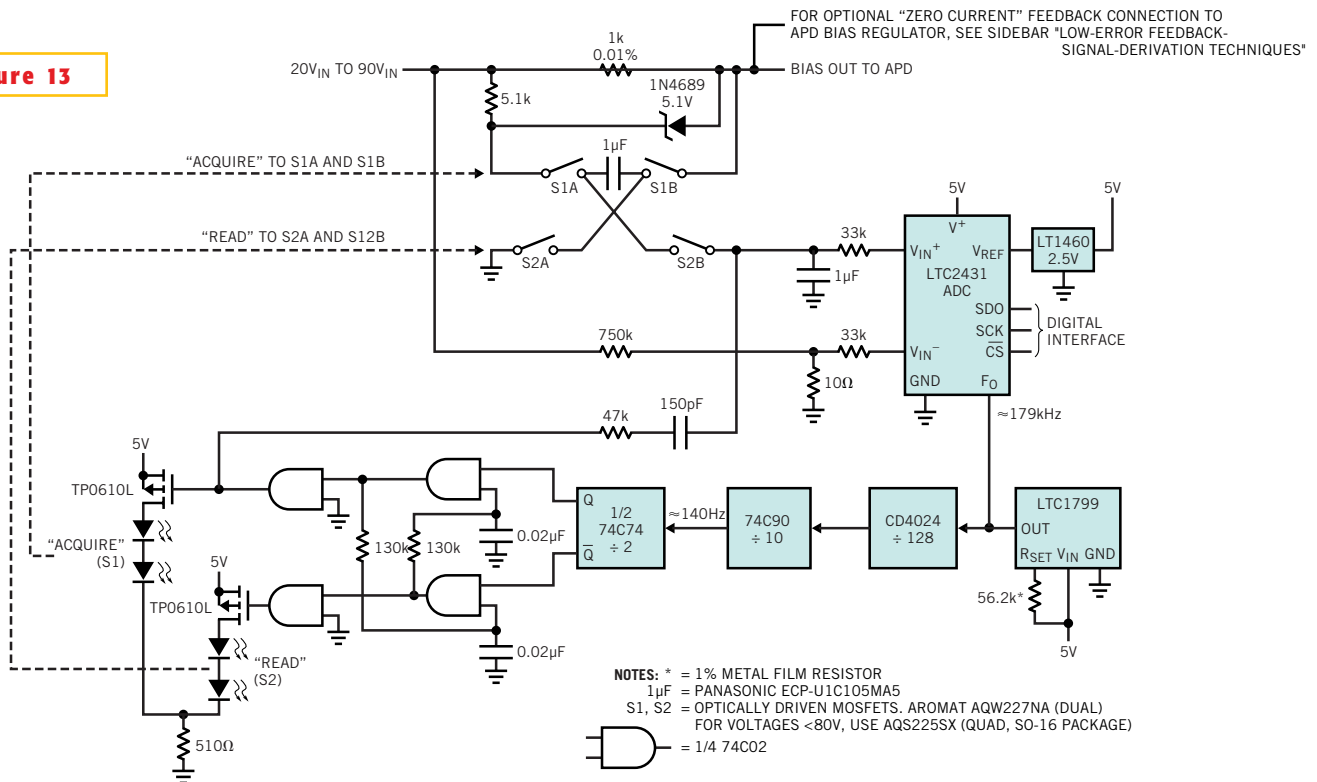


Figure 13



Adding an A/D converter to Figure 12a's optically driven FET-based current monitor provides for a digital output with 0.09% accuracy.

close ("READ"). This action grounds one capacitor plate, and the capacitor discharges into the grounded 1-μF unit at S_{2B}. This switching cycle continuously repeats, resulting in IC₁'s ground-referred positive input, assuming that the same voltage that is across the floating 1-kΩ shunt. The specified LED-driven MOSFET switches have no junction potentials, and the optical drive contributes no charge-injection error. A nonoverlapping clock prevents simultaneous conduction in S₁ and S₂, which would result in charge loss, causing errors and possible circuit damage. The 5.1V zener diode prevents switched-capacitor failure if the bias output shorts to ground.

IC₁, a chopper-stabilized amplifier, has a clock output. After level-shifting and buffering by Q₃, this clock drives a logic-divider chain. The first flip-flop activates a charge pump, pulling IC₁'s V⁻ pin negative, which permits amplifier swing to and below 0V. This scheme is a variant of the one in Figure 5. The divider chain terminates into a logic network. This network provides phase-opposed charging of the 0.02-μF capacitors (traces A and B in Figure 12b). The cir-

cuit arranges the gating associated with these capacitors, so the logic provides nonoverlapping, complementary biasing to Q₁ and Q₂. These transistors supply this nonoverlapping drive to the S₁ and S₂ actuating LEDs (traces C and D).

The extremely small parasitic-error terms in the LED-driven MOSFET switches result in nearly theoretical circuit performance. However, S_{1A}'s high-voltage switching, which pumps S_{2B}'s 3- to 4-pF junction capacitance, causes residual error of approximately 0.1%. This error results in the transfer of a slight quantity of unwanted charge to the 1-μF capacitor at S_{2B}. The amount of transferred charge varies with the APD bias voltage (20 to 90V) and, to a lesser extent, the varactorlike response of S_{2B}'s off-state capacitance. The feedforward of dc components to IC₁'s negative input and ac feedforward from Q₁'s gate to S_{2B} partially cancels these terms. The corrections compensate error by a factor of five, resulting in 0.02% accuracy.

Optical-switch failure could expose IC₁ to high voltage, destroying it and possibly presenting destructive voltages to the 5V rail. The 47-kΩ resistors in IC₁'s pos-

itive input prevent this unwelcome state of affairs.

ADD DIGITAL OUTPUTS

You can modify many of these circuit types to have digital outputs. An optically based current monitor with a digital output (Figure 13) is essentially identical to Figure 12a with two significant differences. In this case, the LTC2431 A/D converter supplies a digital output. The converter's differential inputs allow the same feedforward-based error correction as in the previous example. The divider-chain countdown ratio is different to accommodate a higher speed clock, which the LTC1799 oscillator supplies. This higher speed clock, which times the converter's operation, centers the ADC's internal notch filter at the optical switches' commutation frequencies to maximize rejection. The LTC2431's internal digital filter's first null occurs at 1/2560 of the frequency at the F₀ pin. (See the data sheet for more details.)

This circuit's 0.09% accuracy does not equal the previous analog output's version because of the LT1460 reference's 0.075% tolerance, which you cannot

higher accuracy of 0.05% (see data sheet).

Figure 15 also floats an A/D converter across the shunt and includes an APD bias supply. The LT1946 switching regulator and Q_1 , operating in nearly identical fashion to **Figure 9a**'s circuit, generate the bias supply. The primary difference is that a transformer replaces **Figure 9a**'s inductor. The transformer's primary winding furnishes high-voltage step-up, similar to the one in **Figure 9a**. The floating secondary drives an isolated LT1120-based 3.75V regulator. This floating regulator's output, stacked on top of the APD bias line, powers the LTC2400 ADC. The isolated 3.75V supply permits the A/D converter to measure across the 1-k Ω shunt without pulling operating power from the APD supply. Resistive current limiting and the 5.1V zener diode protect the converter from high voltage if the APD bias output shorts to ground. Low-power optoisolators provide ground-referred digital output and eliminate floating-supply "starve-out" due to cross-regulation interaction with the

APD-regulation loop. Specifically, low-power APD bias outputs could result in insufficient transformer flux to furnish the floating supply's loading requirements. Common optoisolators require significant current, mandating the specified low-power types. The previous circuit's discrete level-shift stage would draw even less power, but the optoisolators are simple and adequate.

The LT1120 2.5V reference and 1-k Ω shunt tolerances dictate 2% circuit accuracy. If you use the tighter tolerance components noted in the schematic, 0.1% accuracy is practical.

A table in the Web version of this article summarizes all of the previous circuits (www.ednmag.com). The chart reviews salient features, but such brevity breeds oversimplification. No substitute exists for a thorough investigation of any application's requirements. \square

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