

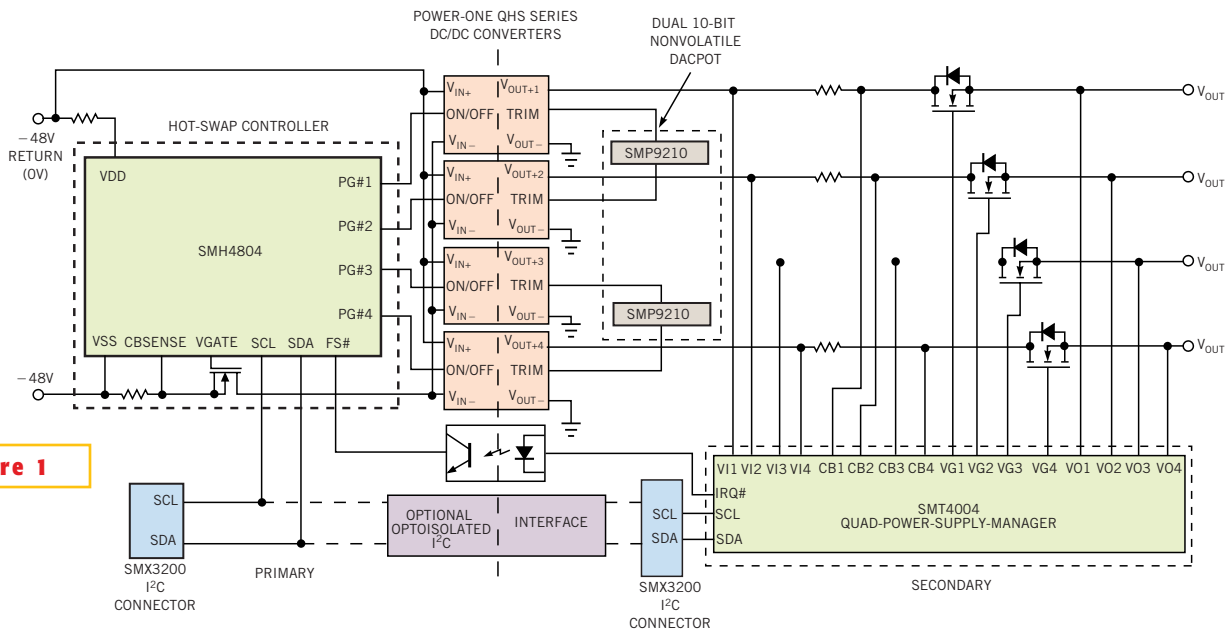
**A COMPLETE POWER SYSTEM GUARANTEES THE PROBLEM-FREE OPERATION OF TELECOMMUNICATIONS EQUIPMENT AND THAT EQUIPMENT'S COMPLIANCE WITH APPLICABLE STANDARDS. DESIGNING THE COMPLETE POWER SYSTEM REQUIRES EXPERTISE IN AREAS BEYOND POWER CONVERSION.**

# Designing a NEBS-compliant power system

DEVELOPING A POWER SYSTEM for modern communications equipment no longer involves simply converting the input voltage into a number of output voltages. The processors and ASICs the system uses determine the fashion in which power is delivered to loads. The power system also must not disrupt communication-system components' normal operation by generating excessive conducted and radiated noise. Finally, the power system must be immune to EMI (electromagnetic in-

terference), ESD (electrostatic discharge), power faults, and damage from power bursts and surges. NEBS (Network Equipment Building System) standards govern the emission and immunity criteria for communications equipment.

Therefore, the task of a power-system designer goes well beyond generating the output voltages. Besides power converters, a comprehensive system includes a variety of components for managing power, reducing EMI, and protecting systems from



**Figure 1**

**A complete telecommunications power system outputs four separate voltages.**

external noise sources. Only a complete power system can guarantee the reliable long-term operation of communications equipment and compliance with industry standards, such as NEBS.

**POWER MANAGEMENT**

The need for power management derives from the constantly increasing complexity of the semiconductor devices that telecommunication and networking equipment use. Data-processing ASICs running at gigahertz speeds, the use of deep-submicron fabri-

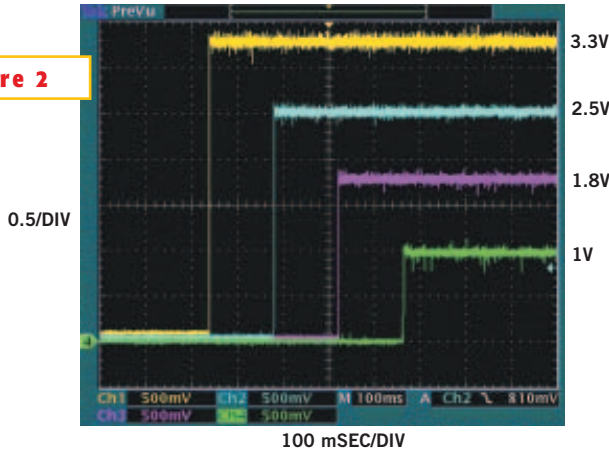
cation processes, and the requirements for multiple voltage rails make semiconductor devices susceptible to power quality and the mode of power delivery.

For example, if you subject a CMOS device to voltage spikes or transients exceeding its maximum voltage rating, the device may exhibit latch-up. Turning on a parasitic structure causes latch-up, which is characterized by the formation of a low-impedance path between power rails. If you do not remove power, the excessive current flowing through the silicon structure can cause system failures or even permanent device damage. Other factors that can trigger latch-up are excessive voltage differentials between power rails, input/output pin voltages exceeding a supply voltage by more than a diode drop, and improper voltage sequencing (Reference 1).

Incorrect voltage sequencing can also cause bus contention. If a DSP's I/O supply receives power before the DSP's core supply receives power, the I/O pins of the DSP and a peripheral device can simultaneously configure as outputs. Depending on the data on the opposing pins, excessive current can flow through the output drivers of either the processor or the peripheral device (Reference 2).

It seems prudent, then, to simply power up the core before the I/O buffers. However, some networking processors require that the core voltage does not exceed the I/O voltage by, typically, a few hundred millivolts. Moreover, they require the core and I/O voltages to track each other in both positive and negative directions (Reference 3). Even

**Figure 2**



**A quad hot-swap controller manages the turn-on sequencing event.**

voltage tracking may be insufficient to address all the chip needs. For example, some FPGAs specify the core voltage's minimum and maximum ramp rates (references 4 and 5). Failure to comply with the requirements for powering semiconductor devices may cause numerous problems, ranging from a bit error to latent defects and, in extreme cases, to immediate and catastrophic device failure.

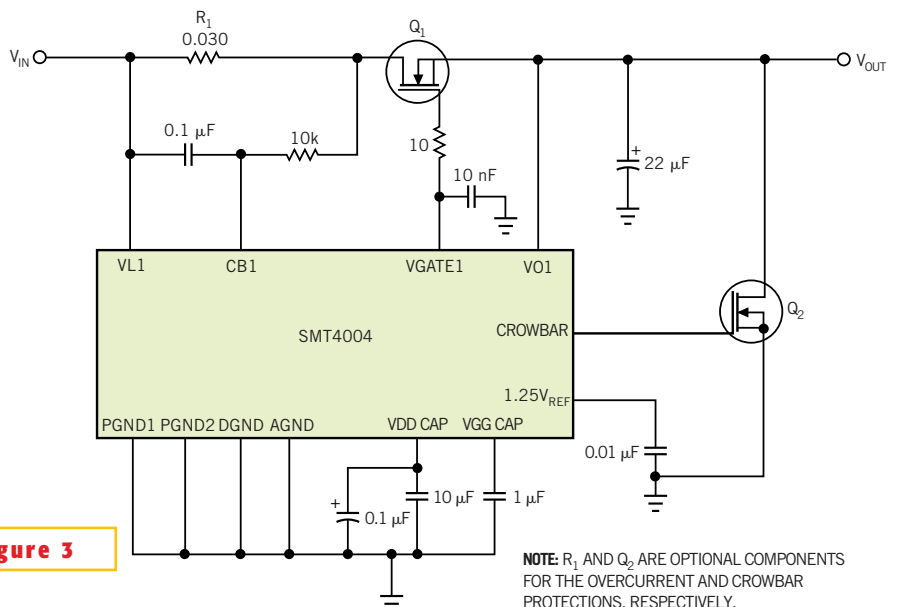
**BASICS OF NEBS COMPLIANCE**

The term NEBS commonly finds use in a family of documents containing in-

dustrywide generic requirements related to telecommunications equipment. GR-1089-CORE, the "Electromagnetic Compatibility and Electrical Safety-Generic Criteria for Network Telecommunications Equipment" is a key document that establishes emission, immunity, and safety criteria for network equipment, systems, and services. NEBS had its genesis in the 1970s when Bell Labs began producing guidelines for equipment designers to help them focus on physical protection, electromagnetic compatibility and safety, and over-

all reliability. Telcordia, the direct corporate descendent of Bell Labs and Bellcore (Bell Communications Research), now administers NEBS.

In most cases, companies do not deploy network equipment unless NEBS has certified it. Compliance with NEBS demonstrates that the equipment vendor has thoroughly tested it for safety and functional criteria for use in telecommunications networks. In addition, communication companies may place extra emphasis on certain aspects of NEBS, such as earthquake resistance in the western United States, humidity in the South,

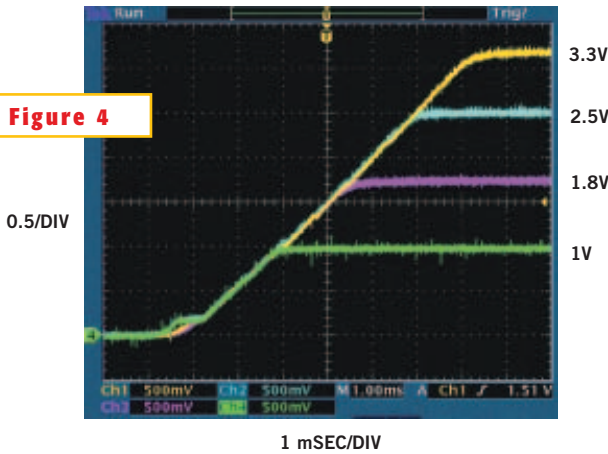


**Figure 3**

**A power-supply manager enables voltage tracking.**

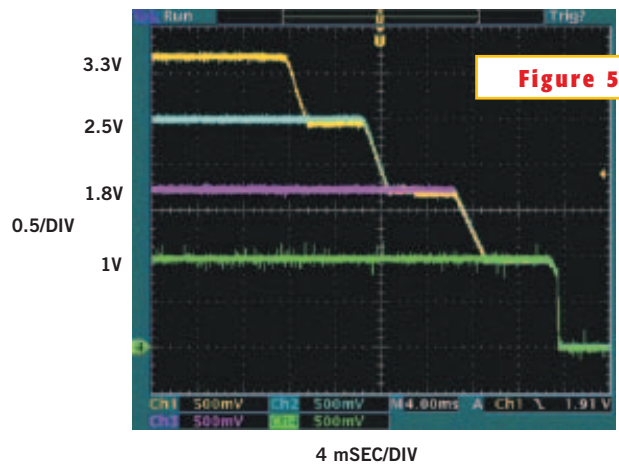
**NOTE:** R<sub>1</sub> AND Q<sub>2</sub> ARE OPTIONAL COMPONENTS FOR THE OVERCURRENT AND CROWBAR PROTECTIONS, RESPECTIVELY.

**Figure 4**



All four voltages synchronously and monotonically ramp up.

**Figure 5**



Staggering outputs and controlling the turn-off slew rate are two means of managing the voltage turn-off.

and airborne contaminants in the Midwest. Some telephone companies are even basing their requirements on the NEBS criteria.

A reference-system design containing dc/dc converters, EMI filters, and power-management controllers has undergone NEBS-compliance testing (Figure 1). These test results are for reference only, because NEBS compliance requires submission to an approved testing facility. The electrically isolated quarter-brick converters generate 3.3, 2.5, 1.8, and 1V output voltages. The quad hot-swap controller and quad tracking power-supply manager handle power-management functions. The dual 10-bit, nonvolatile DAC finds use in trimming the output voltages of the dc/dc converters. The complete system schematic includes an integrated EMI filter model for reducing input noise (Reference 6).

**POWER-MANAGEMENT FUNCTIONS**

All power-management controllers that the system uses include an I<sup>2</sup>C interface. This interface enables a user to program system parameters, such as turn-on and turn-off delays, positive and negative slew rates, overvoltage- and undervoltage-protection thresholds, and other characteristics. A user can adjust the parameters without changing hardware, effectively redesigning the system without swapping a single component. The ability to tweak the power-system parameters during testing and

troubleshooting increases system performance.

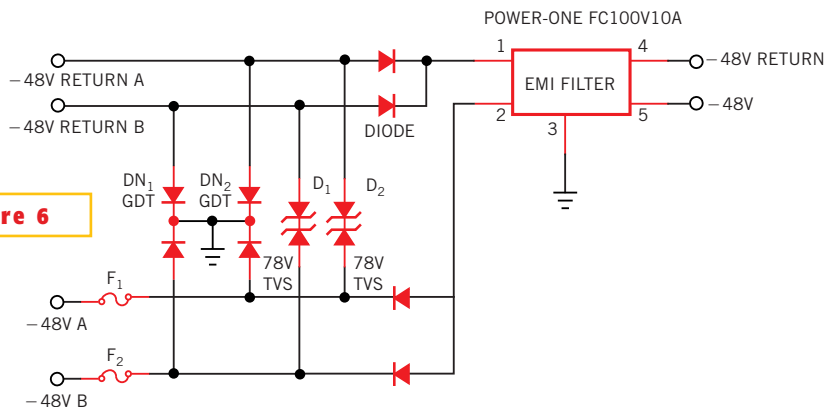
The hot-swap controller permits full control of both the power-on and the power-off sequencing of as many as four dc/dc converters (Figure 2). Users can program delay times of 50 to 160 msec. In addition, the controller reduces the inrush current that users cause by inserting and removing system boards that connect to the voltage source. On/off pins control the dc/dc converters. This sequence is for demonstration purposes only; you can accomplish any required sequence by programming the quad hot-swap controller via the I<sup>2</sup>C interface.

If sequencing is insufficient for system needs, you can add a power-supply man-

ager to enable voltage tracking. This device can control four independent voltage rails, and it also performs a variety of supervisory functions, such as voltage monitoring and undervoltage, overvoltage, and overcurrent protection (Figure 3). The series-pass MOSFET, Q<sub>1</sub>, lies between the output of a dc/dc converter and its load. The power-supply manager controls the turn-on and turn-off behavior of Q<sub>1</sub>, enabling a user to manage the mode of power delivery.

Analyzing the turn-on behavior of the four dc/dc converters with the voltage-tracking feature enabled, all four voltages are synchronously and monotonically ramping (Figure 4). No voltage differential exists between the supply rails during

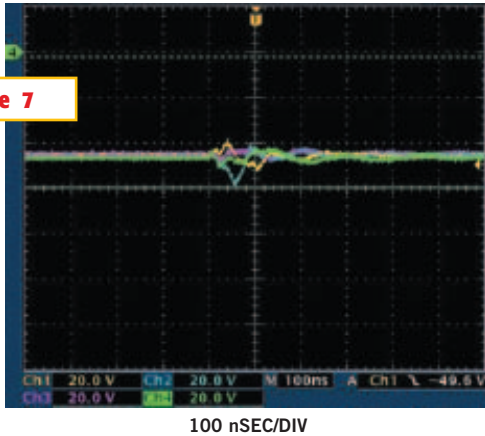
**Figure 6**



The input section of the power system, bolstered for NEBS compliance, adds the components shown in red.

**Figure 7**

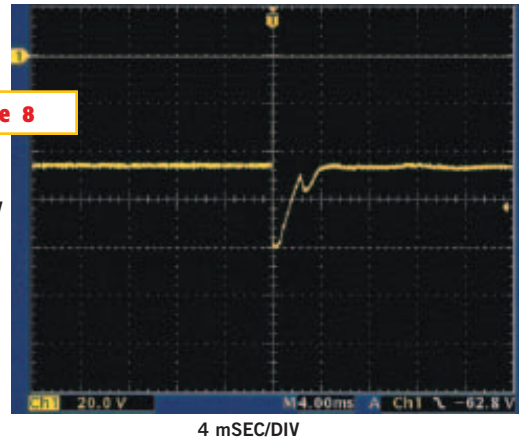
20V/DIV



Results of the 500V burst test at various points in the power system indicate the degree of attenuation that each section contributes to suppressing the burst-waveform disturbance. Channel 2 placement is after the protection circuit and before the EMI filter (blue trace). Channel 4 placement is after the EMI filter on the input of the dc/dc converters (green trace).

**Figure 8**

20V/DIV



Results of the 1000V surge test indicate that the protection circuit is clamping the surge to approximately -80V.

turn-on, thus eliminating the need for clamping diodes. You can adjust the slew rate from 0.1V/msec to 1V/msec to meet specific device requirements. The turn-off process demonstrates how you can manage the turn-off by staggering outputs and controlling the turn-off slew rate (Figure 5). Additional functions, enhanced flexibility, and a greater degree of user control all justify the increased system complexity. All of these factors enable users to meet the power-managing requirements of the most demanding semiconductor devices.

exceed certain specified field strengths. A similar test occurs with the doors open. Conducted emissions, including ac and dc power and signal leads, from the power system into public-utility power lines similarly undergo control and testing to demonstrate compliance.

Although ESD and EMI represent the commonplace, everyday side of electromagnetic compatibility, power faults and lightning surges represent arbitrary events. These occurrences dictate two levels of criteria. First-level compliance holds that the equipment be undamaged

and able to continue operations after the fault or strike. Second-level criteria state that the unit “may sustain damage, but shall not become a fire, fragmentation, or electrical safety hazard.” Tests typically include short-circuit and surge testing (Reference 8).

### COMPONENT SELECTION

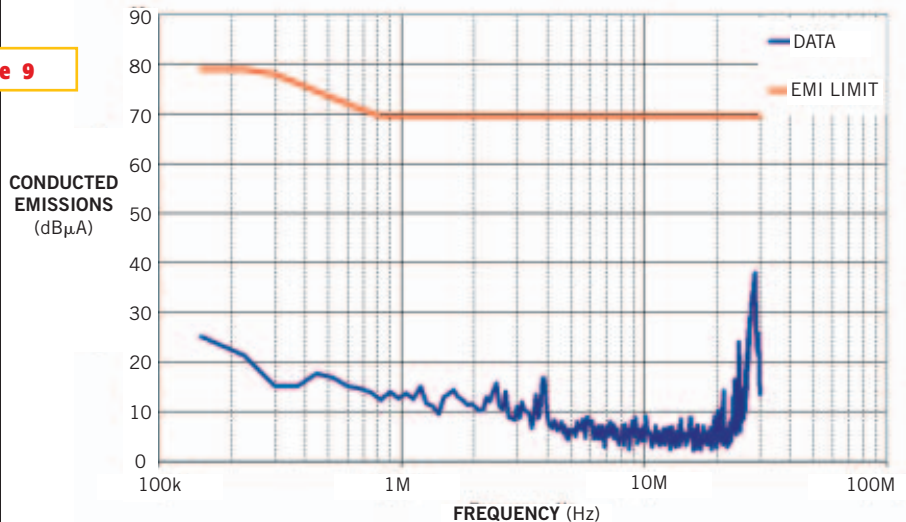
Though the NEBS EMI/EMC (electromagnetic compatibility) standards are exhaustive, most of the testing and hardening efforts focus on immunizing the system from external noise sources such

### NEBS REQUIREMENTS

Noting that electrostatic discharges can cause device damage, alter software and firmware, and affect data, NEBS outlines criteria for ESD immunity during normal operation, installation, and repair. Testing for ESD immunity involves using either contact- or air-discharge methods. For example, during normal operation, a unit must show that its test points can withstand 40 15-kV air discharges or 20 8-kV contact discharges. During this test, according to GR-1089, “a service-affecting response, unless within system operating limits, shall not occur” (Reference 7).

NEBS also describes the equipment testing necessary to see how well it avoids interfering with other nearby equipment. For example, radiated electronic emissions from a closed-door unit must not

**Figure 9**



Conducted common-mode emissions of the power system indicate its response to ESD tests.

as ESD, voltage surges, and lightning strikes. The same circuitry—the EMI filters—that prevents the system itself from becoming a noise source renders harmless additional noise sources, such as EMI that originates from other cards operating on the  $-48\text{V}$  bus.

Within the input section of a NEBS-compliant power system, the transient-voltage suppressors, diodes  $D_1$  and  $D_2$ ; the gas-discharge tubes,  $DN_1$  and  $DN_2$ ; the fuses,  $F_1$  and  $F_2$ ; and the conducted-EMI-suppression filter comply with GR-1089 requirements (**Figure 6**).  $DN_1$  and  $DN_2$  protect the equipment from lightning strikes. Exceeding these devices' breakdown voltage causes them to act as a short circuit. The rugged devices are available in a number of breakdown voltages.  $D_1$  and  $D_2$  handle high-voltage, short surges, such as ESD, and are also available in many breakdown voltages and power-handling capabilities.

$F_1$  and  $F_2$  protect against the catastrophic failure of a component of the input section or the input circuitry of a dc/dc converter. The EMI filters attenuate noise coming from the  $48\text{V}$  bus, as well as noise reflected by the dc/dc converters back into the  $-48\text{V}$  source. These filters are often necessary for meeting conducted- and radiated-emissions criteria. The integrated EMI filter includes low- and high-frequency common-mode inductors and X and Y capacitors, and it eliminates the need for external EMI-reduction components.

#### TESTING FOR NEBS COMPLIANCE

**Figure 7** shows the effect of the NEBS 500V amplitude-burst pattern on the  $-48\text{V}$  supply following the input-protection circuitry. The protection circuitry clamps the burst voltages to approximately 60V. The varying amplitudes of the waveforms indicate the degree of attenuation that each section contributes to squelching the burst-waveform disturbance. Level 1 ( $\pm 500\text{V}$ ) bursts damaged none of the components. This system passes the Level 4 requirements of  $\pm 4000\text{V}$ .

Despite applying Level 1 ( $\pm 500\text{V}$ ) and Level 2 ( $\pm 1000\text{V}$ ) surges to the system, the protection circuit is clamping the surge to approximately  $-80\text{V}$  (**Figure 8**). It also shows that the dc/dc converters in the system must be able to withstand the input-voltage surge exceeding the maximum input-voltage rating of 75V. Con-

verters with an input-surge rating of 100V/100 msec guarantee reliable operation during NEBS testing.

Beginning at the lowest level of protection according to NEBS, the Level 1 ESD test comprises five positive and five negative 2000V applications to the system at 1-sec intervals. Level 2 is similar to Level 1 except that Level 2 employs 4000V. Levels 3 and 4 voltages are 6000V and 8000V, respectively. Any attempt to take scope photos would potentially damage the scope and its probes if the protection circuit failed. However, a current probe can measure the conducted common-mode emissions from the power system into the  $48\text{V}$  source, as the GR-1089 requires (**Figure 9**). □

#### REFERENCES

1. Redmond, Catherine, "Winning the battle against latch-up in CMOS analog switches," *Analog Dialogue*, Volume 35, 2001.
2. Texas Instruments, "Power Supply Sequencing Solutions for Dual Supply Voltage DSPs," *Application Report SLVA073A*, 2000.
3. Motorola, "MPC8280 hardware specifications," Revision 0.1, October 2002.
4. Goldblatt, Kim, "Power-On Requirements for the Spartan-II and Spartan-IIe Families," Xilinx Application Note XAPP189, 2001.
5. Lesea, Austin and Mark Alexander, "Powering Xilinx FPGAs," Xilinx Application Note XAPP158, 2002.
6. "SMH4804 and SMT4004 Telecom Reference Design," Application Note 25, Summit Microelectronics, 2002.
7. Telcordia, "GR-1089-CORE: Electromagnetic Compatibility and Electrical Safety-Generic Criteria for Network Telecommunications Equipment," Issue 2, December 1997 with Revision 1, February 1999.
8. "The FaultZone Recipe for Reliability: NEBS Testing and CompactPCI-based Equipment Design," Force Computers, June 2001.

#### AUTHORS' BIOGRAPHIES

*Thomas J DeLurio is the director of application engineering at Summit Microelectronics (Campbell, CA). John Ng is a staff applications engineer with Summit Microelectronics. Mikhail Guz is a senior field applications engineer with Power-One.*