

leading edge

What's hot
in the
design
community

Edited by
Fran Granville

It's getting hot in here

"My wife and I own a ranch in Montana, and four years ago we built a house on it. I love taking guests there and showing them my media center. Three racks of gear, each seven feet tall. Sounds good, looks good ... and heats the entire house. We just leave the closet door open. In Montana in the middle of winter, that's really handy."

—Intel Chief Executive Officer
Craig Barrett

Tricolor LEDs slim front panels

By Bill Schweber

A NEW SURFACE-MOUNT RGB LED from BivarOpto, the optoelectronics division of Bivar, measures just 0.6 mm (0.024 in.) thick, making it a good fit with thin enclosures, such as hand-



Color your panel and display world with the SMTC0606 ultraslim RGB LED with three LEDs in a 1.5×1.6-mm footprint that is just 0.6 mm high.

held devices, screen backlights, and games. The SMTC-0606, in a standard 1.5×1.6-mm package, is encapsulated in epoxy with a lens that appears "water clear" when off. Each of the three LED dice (one comprised of AlGaInP and two of InGaN/SiC) is individually addressable, so your system can fully control the color mixing and appearance. Maximum forward drive current is 125 mA. Color output is 635, 520, and 465 nm for red, green, and blue, respectively. The lead-free device sells for \$1.45 (OEM quantities).

►Bivar Inc, www.bivar.com.

Microcontroller offerings go public

TEXAS INSTRUMENTS has for years been using and delivering ARM-based cores but only to a few customers. The TMS470 platform of ARM7TDMI-based general-purpose processors comprises the first devices from Texas Instruments that are publicly available. The range of devices includes 64 to 1024 kbytes of single-cycle-access flash memory at 60 MHz in pipeline mode. The on-chip analog-to-digital converter sports a 1.5- μ sec conversion time, and the device family includes standard and high-end CAN (controller-area-network) controllers. The programmable high-end timer supports pulse-width modulation and capture and compare functions, or it can act as 32 programmable I/O channels.

The TMS470R1A64, A128, and A256 operate at 48 MHz

and are available now with prices beginning at \$4.95 (1000). The TMS470R1A288, A512, A768, and A1024 will operate as fast as 60 MHz and will be available by midyear with prices beginning at \$8.95 (1000). In addition to the ARM7 third-party development environments, Texas Instruments offers an integrated development environment for the TMS470 devices. The TMX-SK470R1A256 development kit is available for \$395 and includes a development board with the TMS470 device, a JTAG debugger with a USB connector, a power supply, a C compiler, a simulator, and the Kickstart version of IAR's Embedded Workbench for ARM.—by Robert Cravotta

►Texas Instruments, 1-800-336-5236, www.ti.com/tms470pr.

Graphics core slims down for cellular

GRAPHICS CHIPS THAT IMPLEMENT a traditional polygons-to-pixels pipeline offer full compatibility with years' old APIs, but they also require huge transistor budgets and gobble up lots of memory density and bandwidth. This trade-off is acceptable for PCs, perhaps, but it's intolerable for embedded cores within SOCs (systems on chips)

in high-volume and cost-sensitive consumer-electronics applications (see "Getting glitzy with graphics for embedded systems," *EDN*, April 1, 1999, pg 79). Tile-based alternatives from companies such as Bitboys Oy (www.bitboys.fi) and Imagination Technologies (www.imgtec.com) may have had underwhelming success at past PC experiments, but they're leading the charge into multime-

dia-rich cell phones, PDAs, and similar systems.

Add Falanx Microsystems to the list, with a unique twist: the ability to share the functions of a single set of transistors across both graphics and video tasks. According to President and Chief Executive Officer Borgar Ljosland, "Falanx can implement, in silicon budgets ranging from 190,000 to 400,000 gates, the same functions that require 600,000

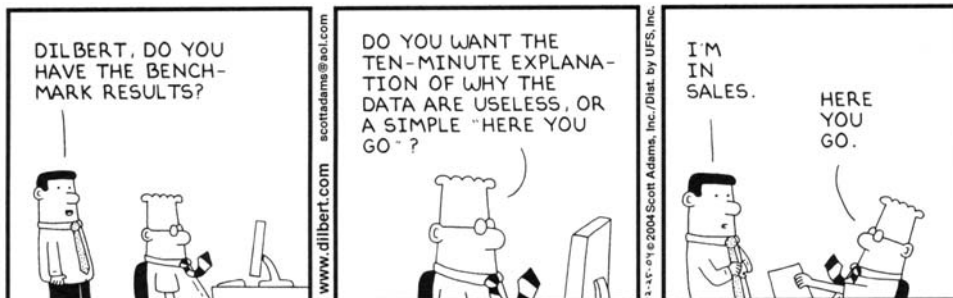
to 1 million gates with competing solutions." The company's second-generation Mali-55 (back-end-triangle setup) and Mali110 (setup plus front-end transform and lighting) cores, binary-compatible with their predecessors, accomplish this objective with a power-consumption budget of 0.2 to 0.5 mW/MHz on a 90-nm process with a 1.2V core voltage (Table 1). They can implement 4× FSAA (full-scene antialiasing) with no performance or power-consumption penalty, and they can support as much as 16× FSAA. Further hardware acceleration is possible using the separate Mali Geometry core. Compatible APIs and video codecs include OpenGL ES, OpenVG, and OpenMAX, which the Khronos Group (www.khronos.org) developed; SVG (scalable vector graphics); Java M3G; Microsoft's D3D Mobile; and various MPEG-4 profile proliferations.

—by Brian Dipert
►Falanx Microsystems, 1-603-264-3438, www.falanx.no.

TABLE 1—GRAPHICS CORES AND THEIR SPECS

	Mali Geometry	Mali110	Mali55
Logic-gate count (NAND, full scan)	150,000	230,000	190,000
SRAM (kbytes)	10	7	4
Die area (130 nm, mm ²)	1.5	3	2
Maximum clock rate (MHz)	150	200	200
Millions of pixels/sec (4×FSAA, bilinear)	NA	300	100
Millions of triangles/sec (transform)	5	5	0.5

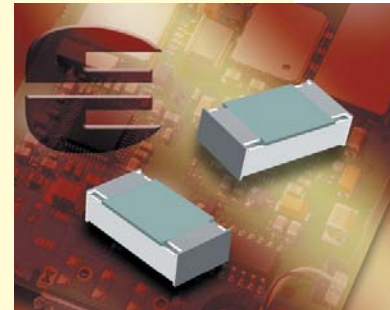
DILBERT *By Scott Adams*



►A recent survey of InStat/MDR's Technology Adoption Panel of US consumers indicates that half of the survey's respondents had heard of digital-satellite radio.

CHIP RESISTOR SHRINKS TCR AND SIZE

The Vishay Beyschlag MCS-0402 family of chip resistors features tight tolerance and low TCR (temperature coefficient of resistance), suitable for precision measurements and other analog-signal paths. The 0402-size devices, in values of 100 to 221 kΩ, are available with tolerance values



With the 0402 thin-film chip resistors of the Beyschlag family, designers can choose resistance of 100 and 221 kΩ, TCR as low as 10 ppm/K, an initial tolerance of better than 0.1%.

of 0.1% and 0.25%. TCR, often more critical than absolute resistor tolerance, is ±25 to ±10 ppm/K, depending on grade. These thin-film, flat resistors have a maximum voltage rating of 50V and can operate at temperatures as high as 125°C with maximum dissipation of 0.63W.

—by Bill Schweber
►Vishay Intertechnology, www.vishay.com.

Class D amplifiers target space-constrained apps

ANALOG DEVICES RECENTLY rolled out a line of amplifiers for the automotive and flat-panel-TV markets, which, it claims, combine space- and

heat-savings benefits of Class D amplification with Analog's audio-signal-processing technology. The company expects the audio technology to im-

prove sound quality and audio fidelity and to decrease EMI.

According to Bill Slattery, Analog's product-line manager for its digital-audio-pro-

duct group, linear amplifiers are still leading the way when it comes to quality and performance. Class D amplifiers have their own inherent strengths, however, according to Slattery. "In a linear world, Class D lets you receive a linearlike performance in a smaller space," he says, adding that Class D amps' perform-

ance is challenging linear for sleek, small systems lacking the room for bulky amps. "These amps have a more compact design [than linear amplifiers], and ... Class D is back to the audiophile performance [that] linear amps have," he says.

The new amplifiers, AD-

(continued on pg 18)

Now there are three: MSOs gain features—and a competitor

FOR THE PAST FEW YEARS, only two companies—Agilent and Yokogawa (www.yca.com)—have manufactured benchtop MSOs (mixed-signal oscilloscopes). These popularly priced instruments have typically combined eight to 16 logic-timing-analysis channels with two or four analog-input channels, whose bandwidth rarely exceeded 1 GHz. MSOs have proved useful in such areas as embedded-system development. Now, LeCroy Corp has joined the MSO fray with 32-logic-channel units, and Agilent has announced a new MSO line, the 6000 series, which offers an even greater number of attractive features than did its highly successful predecessor, the 54600 series.

All three MSO suppliers manufacture moderately priced deep-memory digital scopes. The importance to MSO users of megasample memories in both the analog and the digital channels might explain why Tektronix (www.tektronix.com), the industry's leading scope supplier, has yet to offer a moderately priced MSO. Although Tek supplies deep-memory scopes in its high-performance lines and nearly 10 years ago offered an early, high-performance MSO, the FISO (fast-in/slow-out) architecture of the company's top-selling, popularly priced TDS3000 series doesn't readily accommodate long memories.

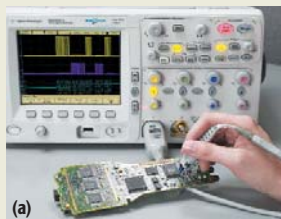
Agilent's 6000 series of 12 portable DSOs (digital storage oscilloscopes) and MSOs includes units that have two and four analog-input channels with bandwidths of 300 MHz, 500 MHz, and 1 GHz. Maximum sampling rates are 2G and 4G samples/sec. Agilent claims that the real-time display-update rate exceeds that of competitive units by as much as 30 times. Memory depths extend to 8M samples/channel using the company's patented MegaZoom III technology. Prices range from \$5595 (300 MHz on two analog channels) to \$16,995 (1 GHz on four analog channels and 16 logic channels). Prices for factory-installed memory upgrades start at \$500, and prices for user-installable DSO-to-MSO upgrade kits start at \$1800.

LeCroy's \$3990 MS-32 32-channel logic-timing-analysis option is unusual in that you can use it to upgrade any model of LeCroy scope that you own with which the factory is now shipping the option. The upgradable scopes include most of the company's four-channel, 350-to-500-MHz WaveSurfer 400 and 500-MHz to 2-GHz WaveRunner 6000A lines. Before upgrading a scope, you must ensure that it contains firmware and software that support the MS-32 option, but LeCroy says that registered LeCroy-scope owners can download firmware and software updates for their scopes from LeCroy's Web site.

The MS-32 can capture records 1M points long at clock rates to 125 MHz. The option package includes a 32-channel logic pod to which you connect all logic probes, an oscilloscope-interface module, a 10.5-in. digital-lead set, a power supply, a USB 2.0 cable, a foam-lined accessory case, and a 5× magnifying glass. Prices for WaveSurfer 400-based configurations with the MS-32 option start at \$10,980; prices for WaveRunner 6000A configurations start at \$12,980.—by Dan Strassberg

▶ Agilent Technologies, 1-800-829-4444, www.agilent.com.

▶ LeCroy Corp, 1-800-553-2769, www.lecroy.com.



The Agilent 6000 series MSOs are compact and present a friendly user interface (a). LeCroy's MS-32 option adds 32 channels of logic-timing analysis at clock rates to 125 MHz and memory depth to 1M sample to two families of the supplier's four-channel DSOs (b).

▶ According to figures from the Consumer Electronics Association, December 2004 factory-to-dealer sales of DTV products hit 927,000 units, marking a 45% increase over December 2003. Total DTV sales for 2004 reached 7.2 million units, an increase of 75% compared with year-end 2003.

(continued from pg 16)

1990, AD1992, AD1994, and AD1996, deliver audiophile sound quality with less than 0.0005% total harmonic distortion plus noise, as much as 40W of output power per channel with at least a 30% heat reduction, and a dynamic range greater than 101 dB.

The amps comprise power-stage-design capability, an advanced sigma-delta modulator, a closed-loop-feedback topology, and advanced mixed-signal and power and digital-CMOS processes. "Using sigma in a closed loop gives the best performance, and closed loop is important

because it gives nonlinearity in output," says Slattery. "In the past, many Class D's have used an open loop, which is self-limiting after a certain point." These amplifiers are instrumental in fixing design issues in HDTV and home-theater systems with lower EMI, resulting in lowered in-

terference with other electronic equipment. The amplifiers are currently available for sampling, and full production quantities will be available in April. Sample prices range from \$2.90 to \$6.72 (1000).

—by Jeff Berman

► **Analog Devices Inc.**, www.analog.com.

System validates wireless-product performance across myriad protocols and applications

AEROFLEX'S NEW DEVELOPMENT- and conformance-verification system tests applications that run on all major cellular-phone types, including GSM (Global System for Mobile Communications), EGPRS (Enhanced General Packet-Radio Service), and W-CDMA (wideband code-division multiple access). According to the manufacturer, the AIME/AT (Air Interface Monitor and Emulator/Applications Test) is the first tester of any kind to use a single platform for testing applications on GSM, W-CDMA, and CDMA handsets. For deterministic lab testing, the system performs live network tests alone or with any Aeroflex GSM, W-CDMA, or CDMA protocol-test system.

"Application developers can no longer think of themselves as part of either the CDMA or GSM world. Instead, they must now market their applications globally. Our new multistandard application-test platform will enable them and their customers to ensure that their products work around the world without interoperability problems," says Peter Connell, general manager of Aeroflex's Burnham, UK, location.

According to Aeroflex, the system's protocol-agnostic approach to application testing is air-interface-independent and meets handset manufacturers' current and future testing needs. Capabilities include testing applications, such as MMS (multimedia-messaging services). The GSM Certification Forum in December 2004 made it mandatory to run such test cases. In addition to measuring data performance, throughput, and application performance and ensuring that the system under test recovers from network failures, the tester also verifies that cellular handsets pass all applicable minimum and application-enabled conformance tests and operator-specific test plans.

Network operators are pressuring handset manufacturers to deliver a plethora of applications during 2005 and early 2006. Although protocol-standards bodies are still working on the exact timetables, the sheer volume of test cases to deliver and test will be challenging. After MMS, the next

two applications requiring certification are video telephony, including two-way image transmission in real time, and digital-rights management to prevent data forwarding. Video streaming for downloading images, instant messaging, push-to-talk technology over cellular, and browsing will follow. As handset- and network-equipment manufacturers and network operators define test cases, they can download and run them on the AIME/AT system.

Because of the myriad applications and wireless-product configurations they can test, AIME/AT system configurations vary widely. The price for a software-only configuration begins at approximately \$170,000. Test cases cost approximately \$1000 each. When you add wireless-network-emulation hardware, system prices extend upward to at least \$700,000.—by Dan Strassberg

► **Aeroflex Inc.**, 1-516-694-6700, www.aeroflex.com.



The AIME/AT system tests the performance and verifies specification conformance of countless wireless products, including phones and applications. The system is available in software-only configurations, as well as in configurations that combine test hardware and software.

► **Since the first DTV products hit the market in late 1998, manufacturers have shipped 16.1 million DTVs, bringing more than \$25 billion in factory revenues, according to the Consumer Electronics Association. Some of the biggest drivers of DTV are flat-panel displays, which accounted for 38% of the year-end DTV-unit totals and reached 2.7 million units shipped in 2004.**

Structured ASICs widen market reach

WITH THE DISPARATE range of products on offer, it is not entirely clear that the “structured ASIC” market sector is indeed a

single sector. LSI Logic and Altera mark two very different members of that grouping, and both have added new and more complex devices to their product ranges.

Altera has introduced the latest version of its HardCopy (called HardCopy II, which is confusingly the third generation of the product). It marks a departure from its predecessors in that earlier devices essentially followed the architecture of Altera’s FPGA devices, but with the programmability stripped off. Relieved of the overhead of programming circuitry, a mask-programmed part could be built with equivalent logic in considerably less silicon area, at correspondingly lower cost. HardCopy II leaves behind the FPGA architecture - it looks a lot like an “old-fashioned” gate array - to achieve a further step up in density. However, Altera’s promise of a turn-key conversion from an FPGA-based design is retained. A series of parts ranges up to 2.2 million “ASIC” gates, 8.8 Mbits of

RAM, and over 350 MHz performance. There is no longer a 1:1 equivalence with the FPGA range. Depending on the mix of DSP with other logic, a given FPGA might map to more than one HardCopy part. The reverse is also true; in addition to viewing the parts as a cost-reduction path for a design executed in a programmable device, designs can target the HardCopy part from the outset. In this scenario, the FPGA becomes a prototyping vehicle and in this case, a selection of FPGAs might serve to prototype a given HardCopy chip. At the level of complexity that will be achievable in 2 million gates, physical synthesis will be required to achieve an efficient placement in the design. Altera notes that the design process will allow combinations such as specifying the HardCopy device as the target (maximising efficiency and performance) while also generating an FPGA configuration file for prototyping. This will not yield an FPGA layout of optimum efficiency, but Altera says it

will be functionally equivalent. Features include memory interfaces for 233 MHz SDRAM, 1 Gbit/sec differential I/O and a range of high-speed serial interfaces. Used in volumes of 100,000, prices will be from \$15 per chip, with an NRE charge starting at \$225,000 for a conversion from an FPGA-based design.

LSI’s RapidChip Integrator 2 series is also a family progression from earlier parts. Rapidchip is LSI’s structured ASIC product, and the company says that it is finding applications in consolidating multiple chips (possibly FPGAs) into a single integrated design. It is also being used for designs that “could have been ASICs” in earlier generation technology but which are economically marginal in today’s advanced high-density processes. The new family comprises eight base “slices” - pre-diffused wafers that are customised to a specific design by metallisation, in four layers. They feature separate areas of memory and logic; “matrix-RAM” memory is organised in blocks that can be combined in width and depth to any required configuration. Further memory can also be configured out of the logic array to provide small, local

blocks. Designers can implement very wide or deep memory and still achieve 300 MHz speeds, LSI says. The highest density slice offers 7.9 Mbits of memory in 344 blocks of varying size; the corresponding peak level of logic density is 5.6 million gates. 250 MHz is quoted as the achieved system clock figure at 25 levels of logic. The devices’ I/O features the usual range of high-speed serial interfaces, although LSI has not implemented SERDES on this series - that comes on a later release. There is also support for high-bandwidth interfaces to external memory, such as DDR2, QDR2, RLDRAM2, and FCRAM2, with controlled impedance and slew rates.

Three of the eight devices are in wire-bond packages, allowing the range to start from a per-chip price of around \$40 (at 30,000 per year and upwards). The five most complex devices are flip-chip packaged, and the most expensive will be priced around \$200 per device. Implementing a design would typically take from three to six months, LSI says.

-by Graham Prophet

► **Altera**, +44 1494 602000, www.altera.com

► **LSI Logic**, +44 1344 413200, www.lsil.com

Differential op-amp improves data acquisition resolution

Using a complementary silicon-germanium and CMOS technology, Texas Instruments has built a fully-differential op-amp that is optimised for driving high-speed analogue-to-digital converters at up to 100 MHz. Its (small-signal) bandwidth is 1900 MHz with a slew rate of 6.6 kV/ μ sec and noise of under 2 nV/ $\sqrt{\text{Hz}}$. As it has differential input and output, it can replace multi-amplifier circuit configurations that were previously needed to complete a differential signal chain. TI says it also delivers significant improvements in second- and third-order harmonic distortion figures, and

reduces settling time, compared to previous amplifiers, to under 2 nsec (to 1%). Users in wireless base-station design will appreciate the distortion figures; in imaging, the low noise; and in measurement, the dc precision, with common-mode output of 5 mV. Gain, common-mode voltage and output impedance are essentially independent of each other and can be controlled separately. The THS4509 is packaged in a 16-pin QFN outline, and will be priced at \$3.75 (1000). An evaluation module is available. - by Graham Prophet

► **Texas Instruments**, +49 8161 803311, www.ti.com

Digital amplifier topology aims high in audio

AUDIO AMPLIFIERS THAT USE switching (pulse-width-modulated) waveforms have progressed very rapidly. Usually designated Class D, they have been used chiefly for their high efficiency, allowing audio to be produced

at reasonable levels from portable or battery-powered equipment. They have also allowed high audio power levels to be generated from compact amplifiers with reduced thermal losses (and, therefore, heatsinking). However, although audio quality has steadily improved, they have not been regarded as being capable of competing with high-quality "conventional" audio amplifier designs for the "hi-fi" market.

Zetex has developed a configuration that it believes is sufficiently different to warrant a new classification, and has created the name "Class Z". In demonstrating the amplifier in prototype form at the recent Consumer Electronics Show in Las Vegas, Audio Marketing Manager Craig Bell says the company had a positive response. Listeners used to identifying the failings of audio amplifiers acknowledged that, as Bell puts it, "if they had not been told it was a digital amplifier, they would not have known."

The design sets out to identify the specific shortcomings of a digital amplifier signal chain, and to correct them. Although Class D handles a nominally perfect square wave through a signal chain that comprises PWM generator, output driver and output power switches, the square

wave in practice becomes less and less perfect at each stage. Distortion can take the form of ringing, changes to edge speeds and other degradations. At the amplifier output there is a reconstruction (low-pass) L-C filter followed by the variable load of the loudspeaker. The speaker load is not precisely known to the amplifier designer and can



Evaluation versions of the Class-Z amplifier are built in discrete form - an integrated controller chip will follow.

vary dramatically, both between loads and across the audio frequency range for any given speaker. In Class Z, one of the techniques Zetex applies is to measure the error present in the output waveform and use that data to generate a feedback signal to correct the error. The error measurement is made in the analogue domain, and the result is digitised and fed back

into a noise-shaping stage at the output of the PWM controller. Pulse-width errors are compensated by interpolating on a time-average-basis; and other errors are compensated by measuring and adjusting the total energy in each pulse. Conventional negative feedback around the complete amplifier loop cannot be used in a Class-D design, Bell says, because of the (typically 2 msec) group delay through the signal path. Hence, most digital amplifiers are open-loop designs. This direct-digital-feedback technique overcomes that problem, and allows very low figures for total harmonic distortion (THD) to be achieved. The technique allows the output stage to run with low shoot-through current, for high efficiency; and gives a low effective output impedance for a high damping factor, (in the thousands at low frequencies, Bell says) to handle "awkward" speaker loads. It also removes the need for a very high-quality power supply, as psu imperfections no longer couple directly into the output. THD is not, Bell asserts, the most effective measure of performance. Zetex uses an intemodulation test with 20Hz and 1 kHz tones; the Class-Z design produces some sidebands around the 1-kHz frequency in the output, but at very low level, and almost no other modulation or noise products.

Zetex will produce an integrated amplifier control IC incorporating the digital feedback mechanisms, scheduled for production late in 2005. - by Graham Prophet
 ▶Zetex, +44 161 622 4444, www.zetex.com