

PART 1 OF THIS SERIES PRESENTED A VARIETY OF CIRCUITS THAT USE A MONOLITHIC OSCILLATOR IN VARIOUS APPLICATIONS. PART 2 CONTINUES WITH MORE EXAMPLES: CHOPPED AMPLIFIERS, SINE-WAVE GENERATORS, AN INTERVAL GENERATOR, AND AN ADC.

A clock for all reasons, part 2: Monolithic oscillator invigorates instrumentation applications

ALTHOUGH THE MOST OBVIOUS APPLICATION for an oscillator is as a clock source in digital systems, a second application area is instrumentation. A variety of circuits, continued here from part 1 of this series, which appeared in *EDN's* June 26 issue, attests to the usefulness of a simple and accurate monolithic oscillator.

CHOPPED BIPOLAR AMPLIFIER

An adaptation of a previous circuit (Reference 1) combines a low-noise op amp with a chopper-based carrier-modulation scheme to achieve an extraordinarily low-noise, low-drift dc amplifier (Figure 1a). The dc drift and noise performance exceed any currently available monolithic amplifier. Offset is in-

side 1 μV with drift less than 0.05 $\mu\text{V}/^\circ\text{C}$. Noise in a 10-Hz bandwidth is less than 40 nV, far below monolithic chopper-stabilized amplifiers. Bias current, set by the bipolar LT1028 op amp's input, is approximately 25 nA. One 5V supply powers the circuit, although its output swings $\pm 2.5\text{V}$. Additionally, a carefully selected chopping frequency prevents deleterious interaction with 60-Hz related components at the amplifier's input. These specifications suit demanding transducer-signal-conditioning sit-

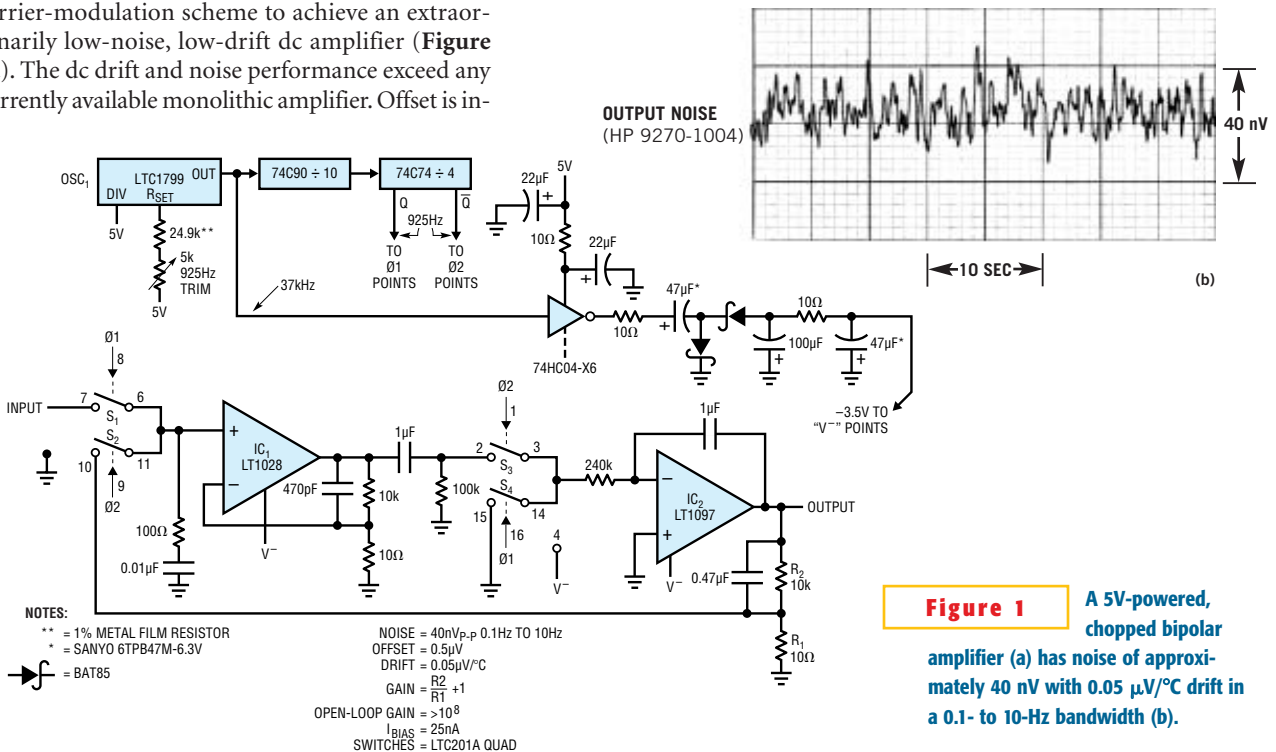
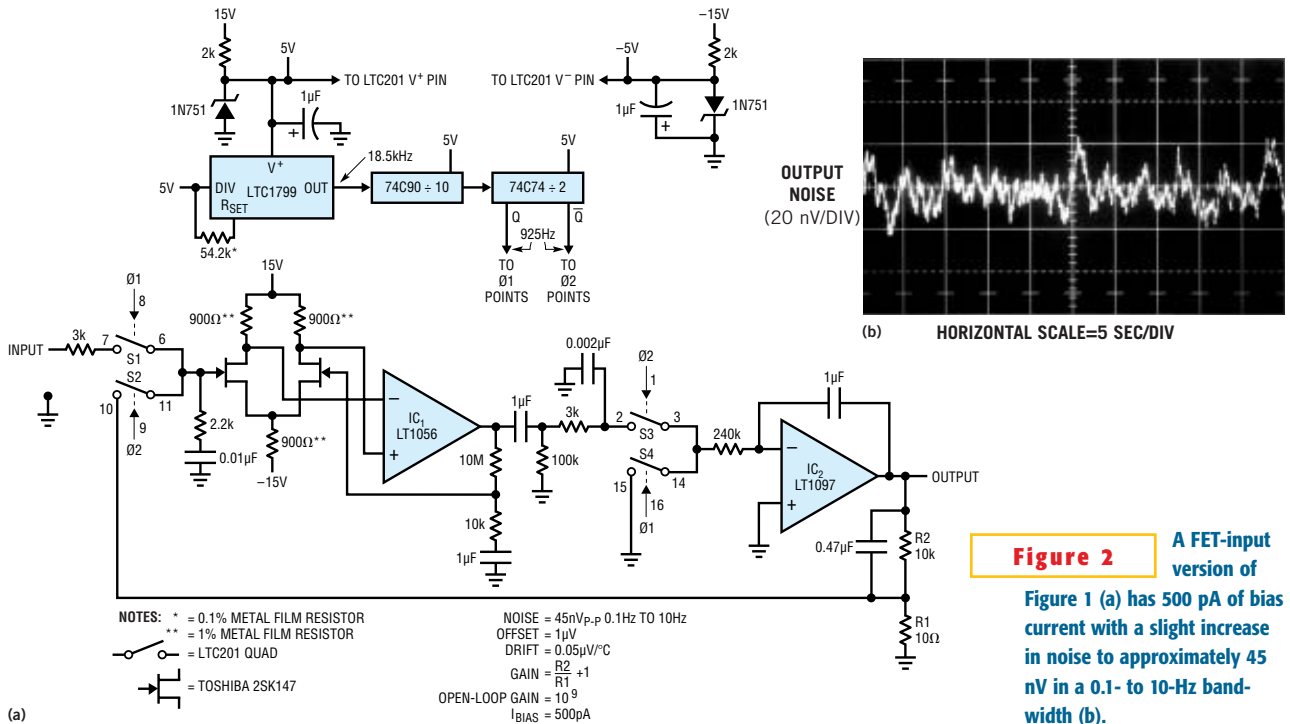


Figure 1 A 5V-powered, chopped bipolar amplifier (a) has noise of approximately 40 nV with 0.05 $\mu\text{V}/^\circ\text{C}$ drift in a 0.1- to 10-Hz bandwidth (b).



uations, such as high-resolution scales and magnetic search coils.

The circuit divides OSC₁'s 37-kHz output to form a two-phase, 925-Hz square-wave clock. This frequency, harmonically unrelated to 60 Hz, provides excellent immunity to harmonic beating or mixing effects, which could cause instabilities. S₁ and S₂ receive complementary drive, causing IC₁ to see a chopped version of the input voltage. IC₁ amplifies

this ac signal. S₃ and S₄ synchronously demodulate IC₁'s square-wave output. Because the input chopper synchronously drives these switches, the circuit presents the proper amplitude and polarity information to IC₂, the dc output amplifier. This stage integrates the square wave into a dc voltage, providing the output. The circuit divides down the output via R₂ and R₁ and feeds back the result to the input chopper where the feedback signal

serves as a zero-signal reference. The R₁-to-R₂ ratio sets the gain, which is 1000 in this case. Because IC₁ is ac-coupled, its dc offset and drift do not affect overall circuit offset, resulting in the extremely low offset and drift performance. IC₁'s input damper minimizes offset-voltage contribution due to nonideal switch behavior.

Normally, this single-supply amplifier's output would be unable to swing to ground. However, powering the circuit's negative rail from a charge pump eliminates this restriction. OSC₁'s 37-kHz output excites the charge pump, which comprises paralleled logic inverters and discrete components. Deliberate 10Ω loss terms combine with the specified 47-μF capacitors to form a very-low-noise power source. These precautions eliminate charge-pump noise that might otherwise de-

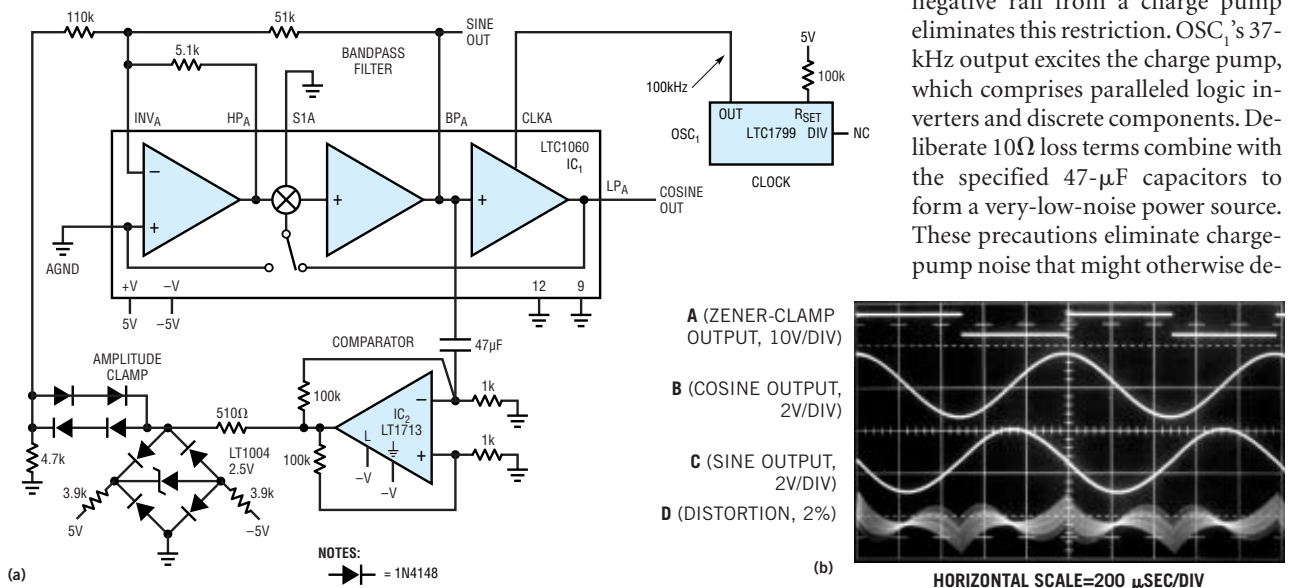


Figure 3 A bandpass filter, driven by IC₁'s oscillation loop (a), continuously rings at resonance to produce cosine and sine outputs (b, traces B and C, respectively). A zener clamp (Trace A) sets the sine and cosine outputs' amplitude.

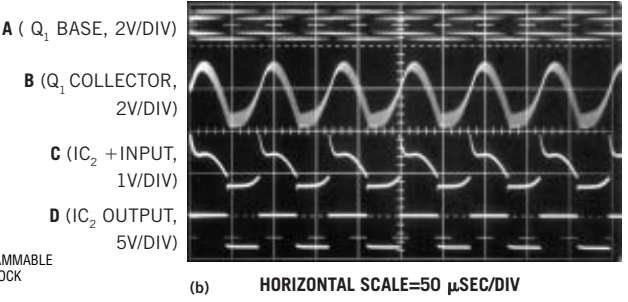
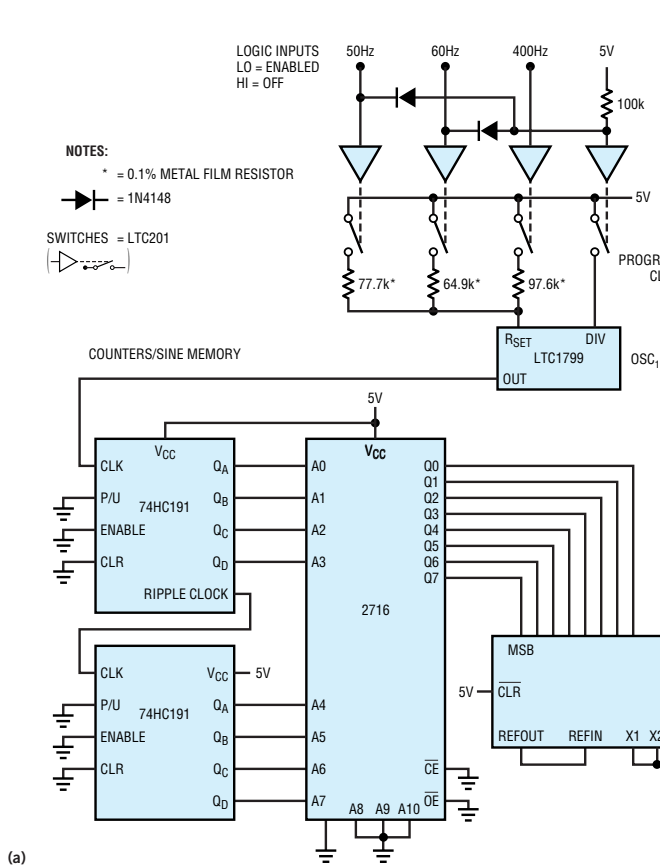


Figure 4 A counter-driven, sine-encoded memory produces a 0.75%-distortion sine wave via a DAC. The LTC1799 oscillator's frequency sets the output frequency.

Clock-related products are evident in the distortion presentation of Figure 4's sine output (a). Fast oscillator-frequency shifting permits crisp changes in the output sine wave's frequency (b). The sine wave's amplitude

Figure 5 instantaneously and faithfully responds to the DAC-reference input step (c).

grade amplifier-noise performance. A noise plot of the amplifier in a 0.1- to 10-Hz bandwidth shows approximately 40 nV of peak-to-peak noise (Figure 1b). IC₁ and the 60Ω resistance of the S₁-S₂ pair contribute approximately equally to form this noise. When using this amplifier, it is important to realize that IC₁'s bias current flowing through the input source impedance causes additional noise. In general, to maintain low-noise performance, the design should keep the source resistance at less than 500Ω. Fortunately, the output resistances of transducers, such as strain-gauge bridges, RTDs, and magnetic detectors, are well below this resistance figure.

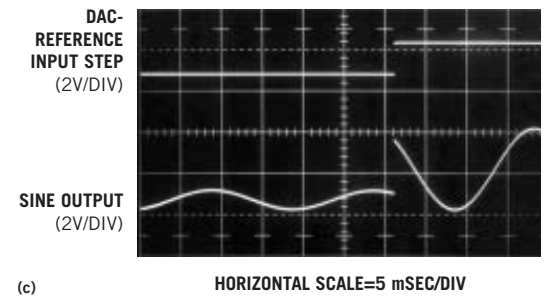
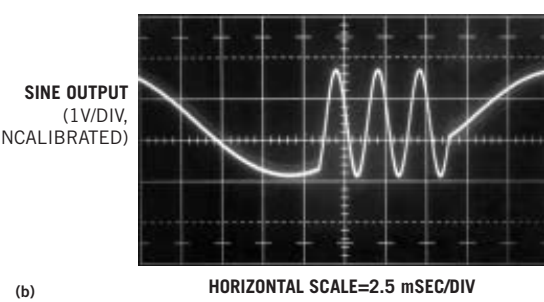
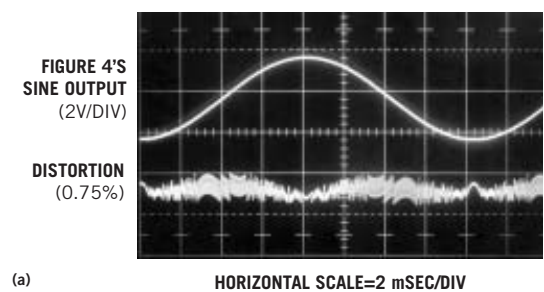
CHOPPED FET AMPLIFIER

You can replace the previous circuit's input stage with a pair of extremely low-noise J-FETs to achieve noteworthy noise performance for a FET-input amplifier (Figure 2a). In most other respects, circuit operation is similar to that of the circuit in Figure 1a. Noise increases slightly to approximately 45 nV, but bias current decreases to 500 pA, which is 50 times lower than the previous circuit. The noise performance is noteworthy because it is almost 17 times better than

currently available monolithic chopper-stabilized amplifiers and nearly equals the best bipolar designs. Other performance specifications, appearing in Figure 2a, are similar to those in Figure 1a.

This circuit retains the 925-Hz clock, although this ±15V-powered design uses zener diodes to derive internal ±5V points. The clock and logic run from 5V, and the LTC201 switches use ±5V. The switches' low-voltage rails reduce charge injection, minimizing its effect on offset voltage. RC damper networks further attenuate parasitic switch-behavior effects, resulting in the 1-μV offset specification.

Noise measured over a 50-sec interval is approximately 45 nV in a 0.1- to 10-Hz bandwidth (Figure 2b). This noise is spectacularly low for a J-FET based design and is directly attributable to the input pairs' die size and current density (references 2 and 3).



R	CLOCK FREQUENCY	NOTCH CENTER FREQUENCY
210k	4.75kHz	60Hz
249k	3.96kHz	50Hz
31.5k	31.72kHz	400Hz

$$\frac{R1}{R2} = 1.234, \frac{f_{CLOCK}}{f_{NOTCH}} = \frac{79.3}{1}$$

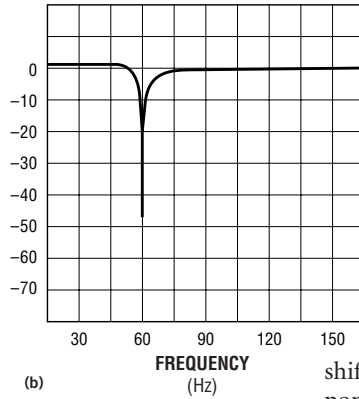
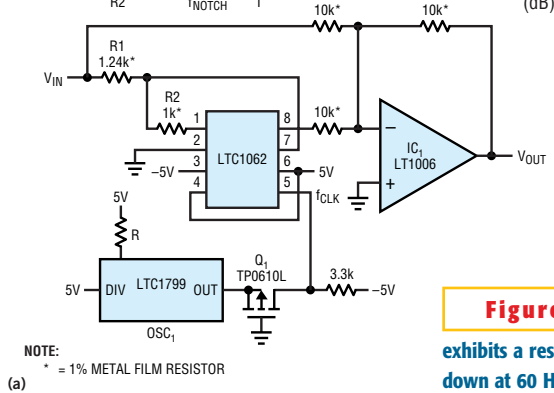


Figure 6 A clock-tuned, highly selective notch filter (a) exhibits a response that is more than 45 dB down at 60 Hz (b).

A sine-wave generator takes advantage of the fact that you can purposely design a feedback-loop-enclosed resonator that oscillates (Figure 3a). This circuit eliminates the need for an amplitude-control loop. This circuit, a mildly modified form of the Regan resonant-bandpass loop, is clock-tunable and produces sine and cosine outputs (Reference 4).

The circuit sets up IC₁'s switched-capacitor filter as a clock-tunable bandpass filter with a Q of 10. OSC₁ clocks the filter at 100 kHz, resulting in a 1-kHz bandpass. The sine output switches IC₂, which supplies square-wave drive to the filter input in regenerative fashion. The loop is self-sustaining, resulting in continuous sine-wave outputs at the indicated points. Zener-bridge clamping of IC₂'s output stabilizes the square-wave amplitude that the circuit applies to the filter and, hence, stabilizes the sine-wave outputs. This form of amplitude control eliminates AGC loop-settling times and potential in-

stabilities. Changes in OSC₁'s clock frequency permit bandpass tuning with no amplitude shifts during or after tuning.

The bandpass filter, responding to IC₂'s clamped output (Trace A, Figure 3b), produces sine (Trace C) and cosine (Trace B) outputs (Figure 3b). Distortion (Trace D), which filter-clock residue dominates, is 2%.

The continuous clocking of a sine-coded look-up-table memory generates a variable-frequency sine wave (Figure 4). A DAC converts the memory's state to an analog output. The strength of this technique is its rapid, high-fidelity response to frequency- and amplitude-change commands. OSC₁'s output, which digital-control inputs set to one of three output frequencies, clocks the 74HC191 counters. These counters parallel load a 2716 EPROM programmed to produce an 8-bit (256 states) digitally coded sine wave (For a copy of the sine-wave-generation code, see the Web version of this

article at www.edn.com.)

The circuit in Figure 4 tunes the sine-wave output in this case to 60 Hz (Trace A, Figure 5a). Distortion mostly comprises clock residue and measures approximately 0.75% (Trace B). The digital inputs abruptly change the output frequency to 400 Hz and then promptly return it to 60 Hz (Figure 5b). These frequency shifts occur crisply, with no alien components or untoward behavior. Amplitude shifts, accomplished by driving the DAC's reference input (see LTC1450 data sheet), are similarly well-behaved. The amplitude faithfully responds to the DAC-reference input step (Figure 5c, traces B and A, respectively). As before, the lack of control-loop time constants promotes the uncorrupted response.

A quick, clean way to tune a notch filter's center frequency is by varying a single, switchable resistor (Figure 6a). The LTC1062 switched-capacitor filter and LT1006 amplifier form a clock-tunable notch. OSC₁, running from the 5V supply, furnishes the clock, which Q₁ level-shifts to drive the ±5V-powered LTC1062. The table in the figure shows three common notch frequencies; you can select others by tuning OSC₁ using the equations in the figure.

The filter's performance at a 60-Hz center frequency shows that the response is down more than 45 dB, with steep slopes on either side of the notch (Figure 6b). The circuit maintains this characteristic over broad ranges of the clock-tuned center frequency.

An accurate interval generator, or "one shot," with a large dynamic range includes a clock, a counter, and a dual flip-

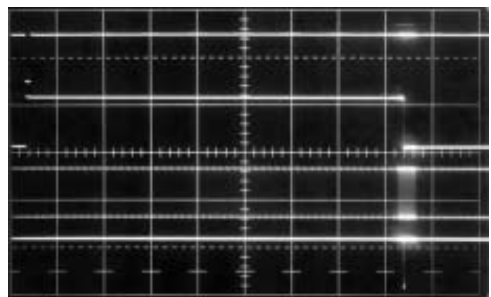
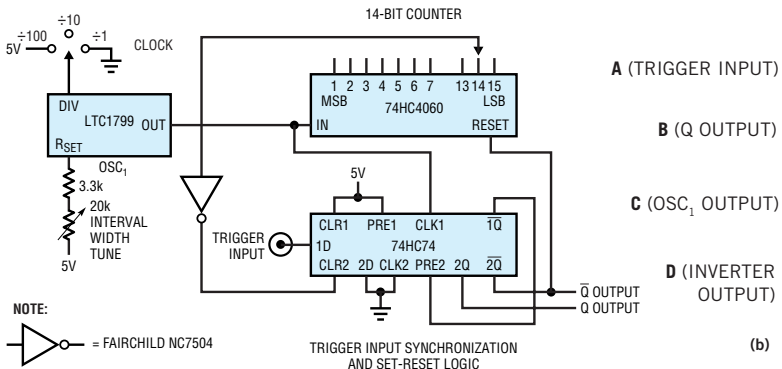


Figure 7 A 1%-accurate interval generator has a dynamic range of 20×10^6 to 1 (a). The trigger-input pulse (b, Trace A) sets the circuit's Q output high (Trace B), and the LTC1799 oscillator (Trace C) clocks the counter until the counter output-biases the inverter low to reset the circuit output (Trace D).

flop (Figure 7a). The clock frequency and counter modulo are programmable. A trigger input passes to the flip-flop IC's $\overline{1Q}$ output (Trace A, Figure 7b) synchronously with OSC_1 's clock (Trace C). This output going low sets the 2Q output—the same as the circuit's Q output—high (Trace B). Simultaneously, the $\overline{2Q}$ output resets the 4060 counter, allowing it to accumulate clock pulses (Trace C, Figure 7b). When enough clock pulses occur to set the selected 4060 output high, the flip-flop IC's CLR2 clear input (Trace D) goes low, ending the circuit's output width. OSC_1 's frequency and the counter's modulo, which are both variable over many decades, set the output width. In Figure 7a's circuit, the interval is programmable from 800 nsec to 16 sec, although other counters can extend this range. Interval accuracy and stability almost entirely depend on OSC_1 's programming resistor.

8-BIT, 80- μ SEC, PASSIVE-INPUT ADC

In general, monolithic ADCs have replaced discrete types. Occasionally, specific desirable circuit characteristics dictate a discrete design. Examples of such special cases include the need for a passive analog input, a particular output data format or control protocol, and economic constraints. An 8-bit design has 90-ppm/ $^{\circ}C$ drift (less than 1 LSB at 0 to 70 $^{\circ}C$) and converts in 80 μ sec (Figure 8a). The circuit, a modern incarnation of an early electronic ADC, consists of a current source, an integrating capacitor, a comparator, logic, and a clock (Reference 5).

Applying a pulse to the convert-command input causes the flip-flop's 1Q output to go high (Trace A) when OSC_1

clocks the CLK_1 input (Figure 8b). This action turns on Q_3 , resetting the 0.01- μ F capacitor (Trace B). Simultaneously, the flip-flop's $\overline{1Q}$ output goes low, pulling the CLK_2 and CLR_2 inputs down. IC_1 's Q output, which is the circuit's status output (Trace C), also goes low, and IC_1 's \overline{Q} output rises high. This logic state prevents any of OSC_1 's clock pulses from transmitting to the circuit's data output (Trace D). When the convert command falls, the flip-flop's 1Q output goes low, Q_3 turns off, and the 0.01- μ F capacitor's voltage begins to ramp. Concurrently, $\overline{1Q}$ goes high, allowing clock pulses to appear at the data output. When the ramp crosses the voltage at E_{IN} , IC_1 's outputs exchange state, pulling the CLK_2 and CLR_2 lines low, and data-output pulses cease. Thus, the OSC_1 -originated clock burst appearing at the data output is directly and solely proportional to E_{IN} . For the arrangement in Figure 8a, 256 pulses appear for a 2V full-scale input. Conversion time decreases with the time required for the ramp to cross E_{IN} . A full-scale conversion requires 80 μ sec, linearly descending to 8 μ sec at 0.1 scale.

The circuit connects the second flip-flop in the 74HC74 as a logic buffer that duplicates the high-impedance diode and 2-k Ω resistor node's logic state. Thus, you should minimize this node's trace capacitance, which this design accomplishes by locating the diodes and 2-k Ω resistor adjacent to the CLK_2 and CLR_2 inputs. You can trim the circuit by applying a 2V input and

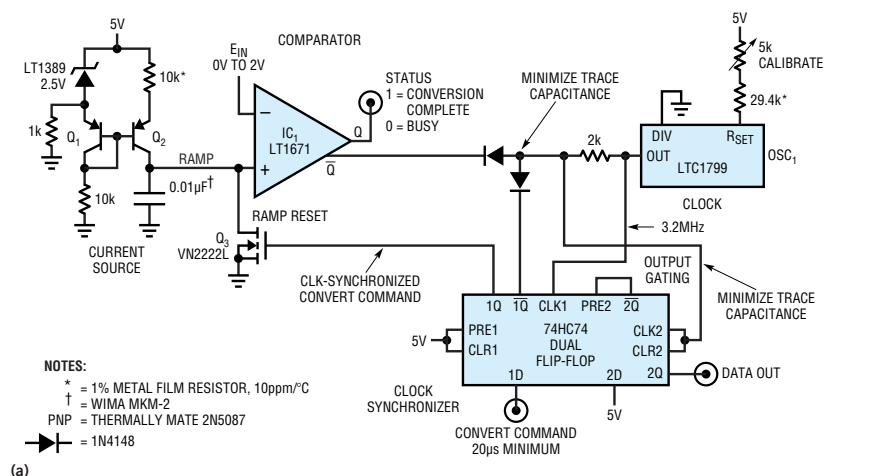
adjusting OSC_1 's frequency output using the 5-k Ω calibrating potentiometer for 256 data-output pulses per conversion. □

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AUTHOR'S BIOGRAPHY

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge).



A (SYNCHRONIZED CONVERT COMMAND, 5V/DIV)
 B (RAMP, 2V/DIV)
 C (STATUS, 5V/DIV)
 D (DATA OUT, 5V/DIV)

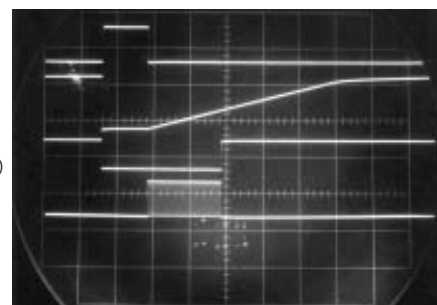


Figure 8 A simple 8-bit ADC has a passive, high-impedance input and an 80- μ sec conversion time (a). A synchronized convert command (b, Trace A) begins a reference ramp and forces the circuit status output low (Trace C). When the ramp crosses E_{IN} 's voltage, the circuit output's clock burst ceases (Trace D).