

TABLE 2—HANDSHAKING TECHNIQUES

Handshake type	Circuits	Signaling type	Sequence length	Synchronizer	Restrictions
Full	Circuit A (request)	Level	Five clocks	Level	Sequence is long. Request must be invalid for at least two of the Circuit B clock periods.
	Circuit B (acknowledge)	Level	Six clocks	Level	Acknowledgment must be invalid for at least two of the Circuit A clock periods.
Partial I	Circuit A (request)	Level	Three clocks	Pulse or edge-detect	Must control rate of acknowledgment pulses.
	Circuit B (acknowledge)	Pulse	Five clocks	Level	Request must be invalid for at least two of the Circuit B clock periods.
Partial II	Circuit A (request)	Pulse	Two clocks	Pulse or edge-detect	Must save pending request information.
	Circuit B (acknowledge)	Pulse	Three clocks	Pulse or edge-detect	Must register request and acknowledgment signals.