



# 2003 Microprocessor directory

32-BIT MICROPROCESSORS (by instruction set)

Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Motorola <a href="http://www.motorola.com/semiconductors">www.motorola.com/semiconductors</a>	68300 family	68K	16 to 33	8 to 32	32	3.3 to 5	1 W	Low-power			
ARC International <a href="http://www.arc.com">www.arc.com</a>	ARCTangent-A4	ARC 32-bit	156 to 183 (0.18) 179 to 247 (0.13)	32	32	1 to 5	0.4 mW/MHz (0.18 micron), 0.1 mW/MHz (0.13 micron)	Standby, sleep	16/24 and dual 16 MAC, XY memory, modulo, bit-reverse, pre/post-increment, two 32x32 options	Can be added	2- to 128-kbyte instruction/data writeback with LRU, locking, configurable from direct mapped to four-way
	ARCTangent-A5	ARCCompact	114 to 164 (0.18) 155 to 230 (0.13)	32	16, 32	1 to 5	0.5 mW/MHz (0.18 micron), 0.2 mW/MHz (0.13 micron)	Standby, sleep	Dual 16-bit MAC/MSUB, 24-bit MAC/MSUB, Viterbi, FFT, CRC, partial complex multiply, saturation	Can be added	2- to 32-kbyte instruction/data writeback with LRU, locking, configurable from direct mapped to four-way
MediaQ <a href="http://www.mediaq.com">www.mediaq.com</a>	MQ9000	ARM	144	24/32	8, 16, 32	1.5/2.5 and 3.3	184 mW	Standby: 2mW	JPEG decode, 64-bit 2-D graphics engine, Java accelerator, MPEG4 post processing		8-kbyte instruction/data
	MQ9150	ARM	144	24/32	8, 16, 32	1.5/2.5 and 3.3			JPEG decode, 64-bit 2-D graphics engine, Java accelerator, MPEG4 post processing		8-kbyte instruction/data
Sharp Microelectronics of the Americas <a href="http://www.sharpsma.com">www.sharpsma.com</a>	LH79520	ARM	77.4	26/32	16, 32	1.8/1.8 or 3.3, 5 tolerant	55 mA	Standby: 35 mA stop1: 500 mA stop2: 18 mA	Yes		8-kbyte unified
	LH7A400	ARM	200	26/32	16, 32	1.8/1.8 or 3.3, 5 tolerant	180 to 200 mA	Halt: 6 to 7 mA standby: 20 to 35 mA	Yes		8-kbyte instruction/data
	LH7A404	ARM	200	26/32	16, 32	1.8/1.8 or 3.3, 5 tolerant	180 to 200 mA	Halt: 6 to 7 mA standby: 20 to 35 mA	Yes		8-kbyte instruction/data
Triscend <a href="http://www.triscend.com">www.triscend.com</a>	A7 CSoC	ARM	Up to 60	32, external: 20 to 32/8 to 32	16, 32	2.5/2.5 to 3.3	1.65 W	Powerdown, selective disable	32x32+64 MAC/32x8, options available		8-kbyte unified, four-way set associative
Altera <a href="http://www.altera.com">www.altera.com</a>	Excalibur: EPXA1 EPXA4 EPXA10	ARM V4T	133, 166, 200	32/32	16, 32	1.8/2.5/3.3	2W, FPGA dependent	Low power (EPXA1)	32x8 user-definable	Can be added in FPGA	8-kbyte instruction/data

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
2- to 10-kbyte RAM, 256-byte Flash	DRAM, SRAM, Flash		132 LQFP, 144 QFP	Two to 16	SCP, TDM, UART, SCI, QSPI, DUART, TouCAN, CTM9	Seven levels	16 channel, 8-bit	-40 to +125		\$9.83 to \$12.46
2- to 512-kbyte ROM, 1- to 128-kbyte XY memory	SRAM			Two 32-bit	Up to eight UART, up to eight Ethernet MAC, USB-FS OTG, USB-FS device	Up to 32		N/A - Core	Add-on AMBA bridge, JTAG to Ethernet debug	License
2- to 512-kbyte ROM, 1- to 128-kbyte XY memory	SRAM, SDR-SDRAM, DDR-SDRAM			Two 32-bit	Up to eight UART, up to eight Ethernet MAC, USB-HS OTG, USB-HS device	Up to 32		N/A - Core	Add-on AMBA bridge, JTAG to Ethernet debug	License
320-kbyte SRAM	SDRAM, SRAM, embedded SRAM, NAND and NOR Flash; DMA	Yes	288 BGA 13x13 mm (0.5-mm pitch) 15x15 mm (0.8-mm pitch)	Two 32-bit, PWM, real-time, watchdog	4-bit SDIO, 115-kbps UART, two 4-Mbps UART, SPI, I <sup>2</sup> C, IrDA, GPIO, 32-bit peripheral bus	Three, up to 71 via GPIO		-30 to +85 0 to +70	CCIR656 interface to support CIF camera, LCD timing chip, hardware rotation, Symbian, Linux, PocketPC, uTRON.	\$14
480-kbyte SRAM	SDRAM, SRAM, embedded SRAM, NAND and NOR Flash; DMA	Yes	336 BGA 16x16 mm (0.8-mm pitch)	Two 32-bit, PWM, real-time, watchdog	4-bit SDIO, 115-kbps UART, two 4-Mbps UART, SPI, I <sup>2</sup> C, IrDA, GPIO, 32-bit peripheral bus	Three, up to 71 via GPIO		-30 to +85 0 to +70	Supports two LCD panels, 1.3M-pixel camera support with hardware JPEG encoder, LCD timing chip, hardware rotation	\$15
32-kbyte SRAM	SRAM/ROM/Flash/SDRAM, four DMA channels	WinCE enabled	176 LQFP	Four 16-bit, two PWM, real-time, watchdog	Three 16550 UART, SPI, Microwire, TI's SSL, 64 PIO	Six external		0 to +70	Color LCDC, advanced TFT support	\$8.27
80-kbyte dual-port SRAM (CPU/LCDC)	SRAM/ROM/Flash/SROM/SDRAM/SFlash, 10 DMA channels	WinCE enabled	256 PBGA or CABGA	Three 16-bit, real-time, up to two PWM, watchdog	Three UART, SPI, MicroWire, SSI, AC'97, 60 PIO	Eight external, vectored	10 channel, 10-bit, touchscreen controller	0 to +70 -40 to +85	Color LCDC, TFT support, MMC/SD, smart-card interface, dc interface, device/host USB 1.1	\$12.28
80-kbyte dual-port SRAM (CPU/LCDC)	SRAM/ROM/Flash/SROM/SDRAM/SFlash, 12 DMA channels	WinCE enabled	324 CABGA	Three 16-bit, real-time, up to two PWM, watchdog	Three UART, SPI, MicroWire, SSI, AC'97, device/host USB 1.1, 60 PIO	Eight external, vectored	10 channel, 10-bit, touchscreen controller	0 to +70 -40 to +85	Color LCDC, TFT support, MMC/SD, smart-card interface, dc interface	\$16.66
4092- or 8192-x32-bit (2048 as optional trace buffer)	8-, 16-, or 32-bit SRAM, Flash, SDRAM, serial Flash, eight-channel DMA	Eight protected, cacheable, resizable memory regions	208 PQFP, 324 BGA	Two 16-bit, 32-bit watchdog, four 32-bit multifunction, can add timers	Two 16C550, can add (HDLC, SPI, I <sup>2</sup> C), SPI, I <sup>2</sup> C, USB, 83 to 189 PIO, two Ethernet	15, special fast, can add more	Eight channel, 10 bit, 1M sample/sec with sequencer		Up to 40,000 on-chip programmable logic gates, up to 120 user-definable I/O pins	\$9.95 to \$18
32- to 256-kbyte SRAM, 16- to 128-kbyte dual-port SRAM	SDRAM, Flash	Dual 64-entry TLB	484/672/1020 FBGA	32-bit, watchdog	Configurable number of UART, up to 170 GPIO, SPI, IDE, PCI, 10/100-Mbps Ethernet	Three configurable modes, six sources, 31 or 63 levels		0 to +70 -40 to +85	4/16/38K FPGA logic elements; two AMBA AHB bus bridges, JTAG debug, ETM9 trace	\$40 to \$500

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Philips Semiconductors <a href="http://www.philips.semiconductors.com/microcontrollers">www.philips.semiconductors.com/microcontrollers</a>	LPC210x	ARM7	60	0/32	8	3 to 4		Idle, powerdown			
Cirrus Logic <a href="http://www.cirrus.com">www.cirrus.com</a>	CS89712	ARM720T	74	32	16, 32	2.5/3.3	90 mW	Standby: less than 0.03 mW, power management			8-kbyte unified
	EP7309	ARM720T	74	32	16, 32	2.5/3.3	90 mW	Standby: less than 0.03 mW, power management			8-kbyte unified
	EP7311	ARM720T	74, 90	32	16, 32	2.5/3.3	108 mW	Standby: less than 0.03 mW, power management			8-kbyte unified
	EP7312	ARM720T	74, 90	32	16, 32	2.5/3.3	108 mW	Standby: less than 0.03 mW, power management			8-kbyte unified
Oki Semiconductor <a href="http://www.okisemi.com/us">www.okisemi.com/us</a>	ML671000	ARM7TDMI	24	23/16	16, 32	2.5/3.3	60 mA	Halt, stop	MAC		
	ML674000 ML674001 ML67Q4002 ML67Q4003	ARM7TDMI	33	24/16	16, 32	2.5/3.3	70 mA	Halt, stop	MAC		
	ML675001 ML67Q5002 ML67Q5003	ARM7TDMI	60	24/16	16, 32	2.5/3.3	70 mA	Halt, stop	MAC		Yes
Cirrus Logic <a href="http://www.cirrus.com">www.cirrus.com</a>	EP9312	ARM920T	200	32	16, 32	1.8/3.3	550 mW	Standby: less than 1 mW, power management	200-MHz MaverickCrunch	200-MHz Maverick-Crunch	16-kbyte instruction/data
ARM <a href="http://www.arm.com">www.arm.com</a>	ARM720T	ARMv4T	Up to 100 (worst case)	AHB 32	16, 32	1.2 (0.13)	0.06 to 0.2 mW/MHz (0.13)	Yes	Yes	Co-processor option	8-kbyte unified
	ARM7TDMI	ARMv4T	Up to 133 (worst case)	AHB 32 (with wrapper)	16, 32	1.2 (0.13)	0.06 mW/MHz (0.13)	Yes	Yes	Co-processor option	Can add external
	ARM7TDMI-S	ARMv4T	Up to 133 (worst case)	AHB 32 (with wrapper)	16, 32	1.2 (0.13)	0.11 mW/MHz (0.13)	Yes	Yes	Co-processor option	Can add external
	ARM920T	ARMv4T	Up to 250 (worst case)	AHB 32 (with wrapper)	16, 32	1.2 (0.13)	0.25 mW/MHz (0.13)	Yes	Yes	Co-processor option	16-kbyte instruction/data
	ARM922T	ARMv4T	Up to 250 (worst case)	AHB 32 (with wrapper)	16, 32	1.2 (0.13)	0.25 mW/MHz (0.13 cache)	Yes	Yes	Co-processor option	8-kbyte instruction/data

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
16- to 535-byte RAM, 72- to 131-byte Flash/EEPROM			HVQFN, LQFP	Three, watchdog	I <sup>2</sup> C, two UART, 32 GPIO	Three external, 16 levels		0 to +70	48 pin, zero wait state	\$4.95 to \$7.95
48-kbyte SRAM	8-, 16-, 32-bit SRAM/Flash/ROM, 32-bit SDRAM	64-entry TLB	256 PBGA	Two 16-bit	10-Mbit Ethernet with integrated PHY, two SSI, IrDA, two UART, two PWM, 27 GPIO	22		0 to +70	LCD controller, 32-bit/128-bit unique MaverickKey ID, touchscreen interface, Glueless digital audio, CODEC interface, JTAG	\$20.37
48-kbyte SRAM	8-, 16-, 32-bit SRAM/Flash/ROM	64-entry TLB	208 LQFP, 256 PBGA, 204 TFBGA	Two 16-bit	Two SSI, IrDA, two UART, two PWM, 27 GPIO	22		-40 to +85	LCD controller, 32-bit/128-bit unique MaverickKey ID, Glueless digital audio, CODEC interface, touchscreen interface, JTAG	\$5.89
48-kbyte SRAM	8-, 16-, 32-bit SRAM/Flash/ROM, 32-bit SDRAM	64-entry TLB	208 LQFP, 256 PBGA, 204 TFBGA	Two 16-bit	Two SSI, IrDA, two UART, two PWM, 27 GPIO	22		-40 to +85	LCD controller, 32-bit/128-bit unique MaverickKey ID, touchscreen interface, JTAG	\$6.51
48-kbyte SRAM	8-, 16-, 32-bit SRAM/Flash/ROM, 32-bit SDRAM	64-entry TLB	208 LQFP, 256 PBGA, 204 TFBGA	Two 16-bit	Two SSI, IrDA, two UART, two PWM, 27 GPIO	22		-40 to +85	LCD controller, 32-bit/128-bit unique MaverickKey ID, touchscreen interface, Glueless digital audio, CODEC interface, JTAG	\$7.13
4-kbyte SRAM	SRAM, DRAM, MASK ROM, Flash		128 QFP	Multifunction, PWM, watchdog	Two UART, USB 1.1, 64-bit GPIO	13, nine external		-40 to +85		\$6.50
8- to 32-kbyte SRAM, up to 4-kbyte of boot ROM, up to 512-kbyte of Flash	SRAM, DRAM, SDRAM, EDO-RAM, MASK ROM, Flash		128 TQFP, 144 LQFP, 144 LFBGA	Multifunction, PWM, watchdog	One or two UART, SSIO, 32- or 40-bit GPIO	18 or 20, five or nine external	Four or eight channel 10-bit	-40 to +85	Selectable clock gears, PLL	From \$4
32-kbyte SRAM, up to 4-kbyte of boot ROM, up to 512-kbyte of Flash	SRAM, DRAM, SDRAM, EDO-RAM, MASK ROM, Flash		144 LFBGA, 144 LQFP	Multifunction, PWM, watchdog	Two UART, I <sup>2</sup> C, SSIO, 42-bit GPIO	20, nine external	Four channel 10-bit	-40 to +85	Selectable clock gears, PLL	From \$5
	8-, 16-, 32-bit SRAM/Flash/ROM, 32-bit SDRAM, EPROM, 12-channel DMA	64-entry TLB	352 PBGA	Two 16-bit, 32-bit, 40-bit, watchdog	Two SSI, IrDA, six I <sup>2</sup> S, SPI, three UART with HDLC, two PWM, three USB 2.0 Host, AC'97, two IDE, 10/100 Ethernet MAC, 8x8 Keypad, 65 GPIO	64	12-bit	-40 to +85	Display controller to CRT/LCD/NTSC/PAL, touchscreen interface, 32-bit/128-bit unique MaverickKey ID, Glueless digital audio, CODEC interface	\$21.53
Licensee option	Licensee option	MMU	Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	Real-time Trace	License
Licensee option	Licensee option		Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	Real-time Trace	License
Licensee option	Licensee option		Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	Real-time Trace	License
Licensee option	Licensee option	MMU	Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	Real-time Trace	License
Licensee option	Licensee option	MMU	Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	Real-time Trace	License

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
	ARM940T	ARMv4T	Up to 180 (worst case)	AHB 32 (with wrapper)	16, 32	1.8 (0.18)	0.8 mW/MHz (0.18 cache)	Yes	Yes	Co-processor option	4-kbyte instruction/data
	SC100	ARMv4T	80 (worst case)	32	16, 32	1.8 (0.18)	0.21 mW/MHz (0.18 no cache)	Yes	Yes		
	SC110	ARMv4T	80 (worst case)	32	16, 32	1.8 (0.18)	0.32 mW/MHz (0.18 cache)	Yes	Cryptography		
	ARM1020E	ARMv5TE	Up to 325 (worst case)	Dual AHB 32 or 64	16, 32	1.0 (0.13)	0.6 mW/MHz (0.13 cache)	Yes	DSP	VFP10 Co-processor	32-kbyte instruction/data
	ARM1022E	ARMv5TE	Up to 325 (worst case)	Dual AHB 32 or 64	16, 32	1.0 (0.13)	0.6 mW/MHz (0.13 cache)	Yes	DSP	VFP10 Co-processor	16-kbyte instruction/data
	ARM946E-S	ARMv5TE	Up to 215 (worst case)	AHB 32	16, 32	1.2 (0.13)	~0.5 mW/MHz (0.13 cache)	Yes	DSP	VFP9 Co-processor	Configurable 4-kbyte to 1-Mbyte instruction/data
	ARM966E-S	ARMv5TE	Up to 250 (worst case)	Dual AHB 32	16, 32	1.2 (0.13)	0.3 mW/MHz (0.13 TCM)	Yes	DSP	VFP9 Co-processor	
	ARM1026EJ-S	ARMv5TEJ	266 to 325 (worst case)	Dual AHB 32 or 64	16, 32	1.0 to 1.2 (0.13)	0.6 mW/MHz (0.13 cache)	Yes	DSP	VFP10 Co-processor	Configurable 4- to 128-kbyte instruction/data
	ARM7EJ-S	ARMv5TEJ	Up to 133 (worst case)	AHB 32 (with wrapper)	16, 32	1.2 (0.13)	0.16 mW/MHz (0.13)	Yes	DSP	Co-processor option	Can add external
	ARM926EJ-S	ARMv5TEJ	Up to 250 (worst case)	AHB 32	16, 32	1.2 (0.13)	~0.6 mW/MHz (0.13 cache)	Yes	DSP	VFP9 Co-processor	Configurable 4- to 128-kbyte instruction/data
	SC200	ARMv5TEJ	110 (worst case)	32	16, 32	1.8 (0.18)	0.30 mW/MHz (0.18 cache)	Yes	DSP		Optional
	SC210	ARMv5TEJ	110 (worst case)	32	16, 32	1.8 (0.18)	0.35 mW/MHz (0.18 no cache)	Yes	DSP, Cryptography		Optional
	ARM1136JF-S	ARMv6	333 to 400 (worst case)	Dual AHB 32 or 64	16, 32	1.0 to 1.2 (0.13)	0.4 mW/MHz (0.13 no cache)	Yes	DSP, SIMD	Yes	Configurable 4- to 64-kbyte instruction/data
	ARM1136J-S	ARMv6	333 to 400 (worst case)	Dual AHB 32 or 64	16, 32	1.0 to 1.2 (0.13)	0.4 mW/MHz (0.13 no cache)	Yes	DSP, SIMD	Option	Configurable 4- to 64-kbyte instruction/data
Motorola <a href="http://www.motorola.com/semiconductors">www.motorola.com/semiconductors</a>	ColdFire family MCF52xx	ColdFire	25 to 140	32/32 or 16	16, 32, 48	1.8/3.3/5	183 mW	Yes	MAC/EMAC, hardware divide		Up to 4-kbyte instruction, or 8-kbyte configurable
	ColdFire family MCF53xx	ColdFire	66, 90	32/32	16, 32, 48	3.3	950 mW		MAC, hardware divide		8-kbyte unified
	ColdFire family MCF54xx	ColdFire	162, 220	32/32	16, 32, 48	1.8/3.3	670 mW		MAC, hardware divide		16-/8-kbyte instruction/data
Fujitsu Micro-electronics America <a href="http://www.fma.fujitsu.com">www.fma.fujitsu.com</a>	FR30	FR	25 to 50, 32.768 kHz	32/32, external: 24/16	16	2.3 to 5.5	230 mW	Sleep, stop, sub clock mode, timer	32x32 DSP macro with barrel shifter and bit search		Up to 4-kbyte instruction
	FR50	FR	32 to 64 32.768 kHz	32/32, external: 24/16	16	2.3 to 5.5	230 mW	Sleep, stop, sub clock mode, timer	32x32 DSP macro with barrel shifter and bit search		Up to 4-kbyte instruction

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Licensee option	Licensee option	MPU	Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core		License
Licensee option	Licensee option	Secure MPU	Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	SecurCore security features	License
Licensee option	Licensee option	Secure MPU	Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	SecurCore security features	License
	Licensee option	MMU	Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	Real-time Trace	License
	Licensee option	MMU	Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	Real-time Trace	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option	MPU	Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	Real-time Trace	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option		Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	Real-time Trace	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option	MMU and MPU	Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	Jazelle (Java), Real-time Trace	License
Licensee option	Licensee option		Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	Jazelle (Java), Real-time Trace	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option	MMU	Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	Jazelle (Java), Real-time Trace	License
Licensee option	Licensee option	Secure MPU	Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	SecurCore security features	License
Licensee option	Licensee option	Secure MPU	Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	SecurCore security features	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option	MMU	Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	Jazelle (Java), Multimedia, Trustzone	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option	MMU	Licensee option	Licensee option	Licensee option	Yes	Licensee option	N/A - Core	Jazelle (Java), Multimedia, Trustzone	License
Up to 96-kbyte of SRAM	EDO, FPM, SDRAM		QFP, BGA	Two to eight 16-bit, four 32-bit, four programmable interval	FlexCAN, 10/100 Fast Ethernet Controller, I <sup>2</sup> C, UART, QSPI, USB, I <sup>2</sup> S, SPDIF, TDM	Interrupt controller	Eight to 10 channel, 10 to 12-bit	0 to +70 -40 to +85	Background debug, IDE interface	\$6.99 to \$17.99
4-kbyte SRAM	EDO, FPM, SDRAM		QFP	Two 16-bit	I <sup>2</sup> C, UART	Interrupt controller		0 to +70 -40 to +85	Background debug	\$11.35 to \$14.95
4-kbyte SRAM	EDO, FPM, SDRAM		QFP	Two 16-bit	I <sup>2</sup> C, UART, USART	Interrupt controller		0 to +70 -40 to +85	Background debug	\$18.95 to \$22.95
Up to 512-kbyte of Flash, up to 160-kbyte of SRAM	DRAM, DMA		100 SQFP, 144 FBGA, 100/160 QFP, 100/120/144 LQFP,	UART, SIO, 16-bit reload, free running, PWC, timebase, PPG, PWM	SIO, CAN, UART, I <sup>2</sup> C, up to 120 PIO	Up to 24 external	16-channel, 8/10 bit ADC; three-channel, 8-bit DAC	0 to +70	Comparator, input capture, output compare	From \$5
Up to 512-kbyte of Flash, up to 160-kbyte of SRAM	DRAM, DMA		100 SQFP, 144 FBGA 100/160 QFP, 100/120/144 LQFP	UART, SIO, 16-bit reload, free running, PWC, timebase, PPG, PWM	SIO, CAN, UART, I <sup>2</sup> C, up to 120 PIO	Up to 24 external	16-channel, 8/10 bit ADC; three-channel, 8-bit DAC	-40 to +85	Input capture, output compare, sound generator, Stepper motor, comparator	From \$5

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	FR65E	FR	50 to 66, 32.768 kHz	32/32, external: 24/16	16	2.3 to 5.5	230 mW	Sleep, stop, sub clock mode, timer	32x32 DSP macro with barrel shifter and bit search		Up to 4-kbyte instruction
Intel <a href="http://www.intel.com">www.intel.com</a>	80960 Cx	i960	16 to 40	32/32	32	5/5	1034 mA	Wait	Yes		1- to 4-kbyte instruction, 1-kbyte data
	80960 HX	i960	25 to 80	32/32	32	3.3/5	1578 mA	Halt, wait	Yes		8- or 16-kbyte instruction/data
	80960Jx 80960VH	i960	16 to 100	32/up to 32	32	3.3/5 tolerant	480 to 690 mA	Halt	Yes		2- to 16-kbyte instruction, 1- to 4-kbyte data, stack frame
	80960Sx 80960Kx	i960	10 to 25	32/16 or 32	32	5/5	340 to 420 mA		Yes	SB/KB only	512-byte instruction
Ubicom <a href="http://www.ubicom.com">www.ubicom.com</a>	IP3023	MASI V2	250	22/8, SDRAM: 15/16	32	1.2/2.5 to 3.3, 5 tolerant	Application dependent	Runtime clock control, separate control of I/O and core PLLs	One-cycle 16x16+48-bit MAC		None, single-cycle program/data memory on-chip
Xilinx <a href="http://www.xilinx.com">www.xilinx.com</a>	MicroBlaze (soft CPU)	MicroBlaze	150	64/32 (Core-Connect)	32	1.0 to 3.3 (FPGA usage)		Yes	556 multipliers		Fast simplex link
IDT <a href="http://www.idt.com">www.idt.com</a>	RC32332 RC32333 RC32334	MIPS	100, 133, 150	23 or 26/32	32	3.3/3.3	1.5 to 1.8 W	Wait	Four		8/2-kbyte instruction/data two-way set associative
	RC32336	MIPS	180	26/32	32	2.5/3.3	2 W	Wait	Four		8/2-kbyte instruction/data two-way set associative
	RC32351 RC32355	MIPS	100, 133, 150	26/32	32	2.5/3.3	1.5 W	Wait	Four		8/2-kbyte instruction/data two-way set associative
	RC32365	MIPS	150	26/32	32	2.5/3.3	2.5 W	Wait	Four		8/2-kbyte instruction/data two-way set associative

# 2003 Microprocessor directory

(by instruction set) 32-BIT MICROPROCESSORS

Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
Up to 512-kbyte of Flash, up to 160-kbyte of SRAM	DRAM, DMA		100 SQFP, 144 FBGA, 100/160 QFP, 100/120/144 LQFP	UART, SIO, 16-bit reload, free running, PWC, timebase, PPG, PWM	SIO, CAN, UART, I2C, up to 120 PIO	Up to 24 external	16-channel, 8/10-bit ADC; three-channel, 8-bit DAC	0 to +70	Comparator, input capture, output compare	From \$5
	Yes		168 PGA, 196 PQFP			Eight, NMI			Supervisor protection	\$27.09 to \$67.56
2-kbyte RAM	GMU		168 PGA, 208 PQFP	Two 32-bit		Eight, NMI			Supervisor protection	\$34.60 to \$106.17
1-kbyte RAM	SRAM, Flash		132 PGA/PQFP, 196/324 PBGA	Two 32-bit	I2C	Program-mable, high-speed controller			16/16 global/local 32-bit registers, high-bandwidth burst bus, JTAG	\$9.98 to \$68.17 \$44.20 to \$68
	Yes		84 PLCC, 80 QFP, 132 PGA/PQFP			Four, direct, handshake				\$7.98 to \$16.66 \$10.64 to \$39.03
256-kbyte SRAM (program or data), 64-kbyte data SRAM	Flash, SDRAM		208 PQFP	Two 32-bit timers, 32-bit watchdog, can add timers	Four MII, two Serdes units, Ethernet MAC/PHY, USB, GPSI, SPI, UART. Software I/O (PCMCIA, CF, IDE, mini-PCI for 802.11a/g)		Analog squelch for 10base-T Ethernet PHY	0 to +70	32-bit random-number generator, software I/O supports interfaces via GPIO, eight-way multithreading, zero-cycle context switching	\$12
72- to 3456-kbyte	SDRAM, DDR, SRAM, Flash, ZBT, SDARM (soft IP)		Virtex/E, SpartanII, SpartanIIE, Spartan3, VirtexII, VirtexII PRO	Watchdog, counters attached via CoreConnect bus	CoreConnect-enabled UART, I <sup>2</sup> C, GPIO, SPI, 16450/550, EMAC10/100, UART lite, 1-Gigabit Ethernet	Soft IP		0 to +70 -40 to +85 -40 to +125	1200 I/O and 125,126 logic cells, chip scope for FPGA debugging	From \$10
	32-bit SDRAM, 8-, 16-, 32-bit ROM/Flash/SRAM/ dual-port/peripheral	32-entry TLB	208 QFP, 256 PBGA	Four 32-bit	One or two 16550-compatible, v2.1 PCI bridge, 12 to 16 PIO	Four, more via PIO		0 to +70 -40 to +85	EJTAG debug	\$13.50 to \$19.25
	32-bit SDRAM, 8-, 16-, 32-bit ROM/Flash/SRAM/ dual-port/peripheral, six-channel DMA	16-entry TLB	256 CABGA	Three 24-bit	One 16550-compatible, SPI, 16 GPIO, v2.2 PCI, v2.1 PCMCIA, 10/100 Ethernet MAC			0 to +70 -40 to +85	ICE, EJTAG	\$15
	32-bit SDRAM, 8-, 16-, 32-bit ROM/Flash/SRAM/ dual-port/peripheral	32-entry TLB	208 QFP	Three 32-bit	Two 16550-compatible, USB 1.1, I2C, 10/100Mbps Ethernet, 36 PIO	Four, more via PIO		0 to +70 -40 to +85	25-Mbps SAR, 8-Mbps TDM, EJTAG debug	\$15 to \$22
	32-bit SDRAM, 8-, 16-, 32-bit ROM/Flash/SRAM/ dual-port/peripheral, six-channel DMA	16-entry TLB	256 CABGA	Three 32-bit	One 16550-compatible, SPI, two 10/100 Ethernet MAC, v2.2 PCI, v2.1 PCMCIA, 16 GPIO			0 to +70 -40 to +85	On-chip security (DES/3DES/AES) encryption, random number generator, ICE, EJTAG	\$17

# 2003 Microprocessor directory

32-BIT MICROPROCESSORS (by instruction set)

Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
	RC32438	MIPS	200, 233, 266	26/16	32	1.2/3.3	2.4 W	Wait	Four		16-kbyte instruction/data four-way set associative
QuickLogic <a href="http://www.quicklogic.com">www.quicklogic.com</a>	QL901M	MIPS	100, 133	32/32	32	1.8/3.3	Based on programmable logic usage	Nap, doze	18 MAC blocks (8x8 multiply, 16-bit carry add)	Software floating-point arithmetic	16-kbyte instruction/data
	QL902M	MIPS	175, 200, 233	32/32	32	1.8/3.3	Based on programmable logic usage	Nap, doze	18 MAC blocks (8x8 multiply, 16-bit carry add)	Software floating-point arithmetic	16-kbyte instruction/data
	QL903M	MIPS	175, 200, 233	32/32	32	1.8/3.3	Based on programmable logic usage	Nap, doze	18 MAC blocks (8x8 multiply, 16-bit carry add)	Software floating-point arithmetic	16-kbyte instruction/data
	QL904M	MIPS	175, 200, 233	32/32	32	1.8/3.3	Based on programmable logic usage	Nap, doze	18 MAC blocks (8x8 multiply, 16-bit carry add)	Software floating-point arithmetic	16-kbyte instruction/data
Toshiba America Electronic Components <a href="http://www.toshiba.com">www.toshiba.com</a>	TX19 family	MIPS16	Up to 40	24/32, external: 8 or 16	16, 32	2.0 to 3.6	165 mW (ROM)	Stop, sleep, slow	One-cycle MAC		
AMD <a href="http://www.amd.com">www.amd.com</a>	Au1000 Au1100 Au1500	MIPS32	266, 333, 400, 500	32/32	32	1.0 to 1.2/ 2.5 or 3.3	200 mW to 1.2W	Idle, sleep	MAC		16-kbyte instruction/data
MIPS Technologies <a href="http://www.mips.com">www.mips.com</a>	4Kc 4Km 4Kp	MIPS32	230 to 260	32/32	32	Process dependent	0.1 to 0.3 mW (0.13)	Wait	One-cycle 16x16, 32x16, two-cycle 32x32		0- to 16-kbyte instruction/data
	4KEc (Pro) 4KEm (Pro) 4KEp (Pro)	MIPS32	230 to 260	32/32	32	Process dependent	0.1 to 0.3 mW (0.13)	Wait	One-cycle 16x16, 32x16, two-cycle 32x32		0- to 64-kbyte instruction/data
	4KS family	MIPS32	200 to 240	32/32	32	Process dependent	0.1 to 0.3 mW (0.13)	Wait	One-cycle 16x16, 32x16, two-cycle 32x32		0- to 64-kbyte instruction/data
	M4K M4K Pro	MIPS32	200 to 240	32/32, SRAM	32	Process dependent	0.1 to 0.3 mW (0.13)	Wait	One-cycle 16x16, 32x16, two-cycle 32x32		

# 2003 Microprocessor directory

(by instruction set) 32-BIT MICROPROCESSORS

Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
	16-, 32-bit SDRAM, 8-, 16-, 32-bit ROM/Flash/SRAM/dual-port/peripheral, 10-channel DMA	16-dual-entry TLB	416 BGA	Three 32-bit	Two 16550-compatible UART, I2C, SPI, two 10/100 Ethernet MAC, v2.2 PCI, GPIO			0 to +70 -40 to +85	Enhanced JTAG and ICE interfaces, on-chip bus-monitor logic	\$25 to \$35
16-kbyte SRAM, 82.9-kbit dual-port SRAM (128x18, 256x9, 512x4, 1024x2)	SDRAM, Flash, SRAM, EPROM	32-bit-entry TLB	680 PBGA, 1.27-mm pitch	Four 32-bit	Two serial (hardware flow control, IrDA), PCI	Seven		0 to +70 -40 to +85	2016 programmable logic cells (equivalent to 75,000 ASIC gates)	\$70
16-kbyte SRAM, 82.9-kbit dual-port SRAM (128x18, 256x9, 512x4, 1024x2)	SDRAM, Flash, SRAM, EPROM	32-bit-entry TLB	544 PBGA, 1.27-mm pitch	Four 32-bit	Two serial (hardware flow control, IrDA), PCI	Seven		0 to +70 -40 to +85	2016 programmable logic cells (equivalent to 75,000 ASIC gates)	\$50
16-kbyte SRAM, 82.9-kbit dual-port SRAM (128x18, 256x9, 512x4, 1024x2)	SDRAM, Flash, SRAM, EPROM	32-bit-entry TLB	544 PBGA, 1.27-mm pitch	Four 32-bit	Two serial (hardware flow control, IrDA), PCI	Seven		0 to +70 -40 to +85	2016 programmable logic cells (equivalent to 43,000 ASIC gates)	\$40
16-kbyte SRAM, 82.9-kbit dual-port SRAM (128x18, 256x9, 512x4, 1024x2)	SDRAM, Flash, SRAM, EPROM	32-bit-entry TLB	544 PBGA, 1.27-mm pitch	Four 32-bit	Two serial (hardware flow control, IrDA)	Seven		0 to +70 -40 to +85	1152 programmable logic cells (equivalent to 43,000 ASIC gates)	\$35
Up to 1 Mbyte of mask ROM or Flash, 40-kbyte SRAM	Eight-channel DMA		100 LQFP, 281FBGA	Four 16-bit, up to 12 8-bit, eight 32-bit input capture, real-time, watchdog	Up to eight UART, I2C, 77 PIO	Up to 29 external, NMI	Up to 24 channel, 10-bit			\$8 to \$15
See cache	SRAM, SSRAM, SDRAM, Flash, EPROM	32-entry TLB, Four-entry instruction TLB	324/399/424 PBGA	Programmable interval, real-time	Two to four UART, 32 to 48 GPIO, USB host/device, AC97, I2S, up to two SSI, IrDA, PCI, one or two Ethernet	Yes		0 to +70 -40 to +85	LCD controller, two secure-digital controllers	\$14.45 to \$31.89
Configurable	Optional	16 dual-entry jTLB with variable page size or FMT mechanism		Optional				N/A - Core	Synthesizable core	License
Configurable	Optional	16 dual-entry jTLB with variable page size or FMT mechanism		Optional				N/A - Core	Synthesizable core, CorExtend user-instructions	License
Configurable	Optional	16 dual-entry jTLB with variable page size or FMT mechanism		Optional				N/A - Core	Synthesizable core, code compression, SmartMIPS ASE, crypto-acceleration, CorExtend user-instructions	License
Configurable	Optional	16 dual-entry jTLB with variable page size or FMT mechanism		Optional				N/A - Core	Synthesizable core, cacheless design for multiprocessor designs	License

# 2003 Microprocessor directory

32-BIT MICROPROCESSORS (by instruction set)

Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Altera <a href="http://www.altera.com">www.altera.com</a>	Nios	Nios	Up to 125	16/16, or 32/32	16	1.5, 1.8, 2.5, 3.3, 5.0		Clock reduction via static design	250-MHz 36x36 DSP block, two-cycle 16x16, 1-bit/clock, user-definable	Can be added via custom instruction	Configurable 1- to 16-kbyte instruction/data direct mapped, write-through
Motorola <a href="http://www.motorola.com/semiconductors">www.motorola.com/semiconductors</a>	MPC5500 family	PowerPC	23.2 to 150	24/16 or 32 data	32	1.5/3 to 5, external: 1.6 to 3.6, 5 ADC	1.2 W	Yes	SIMD signal processing engine, MAC units, FFT support	Single-precision scalar and SIMD floating-point instructions	8- to 32-kbyte instruction/data cache locking
	MPC500 family MPC53x	PowerPC	40	32/32, external: 24	32	2.6/5	800 mW	Doze, sleep, deep-sleep, powerdown	64-bit MAC	Double-precision	
	MPC500 family MPC55x	PowerPC	40	32/32, external: 24	32	3.3/5	800 mW	Doze, sleep, deep-sleep, powerdown	64-bit MAC	Double-precision	
	MPC500 family MPC56x	PowerPC	40, 56, 66	32/32, external: 24	32	2.6/5	800 mW	Doze, sleep, deep-sleep, powerdown	64-bit MAC	Double-precision	
	MPC5200	PowerPC	400	28/32, 25/16, 16/16, 24/8	32	1.5/3.3, 2.5 DDR RAM	815 mW	Nap, doze, sleep, deep sleep	Hardware multiplication	Double-precision	16-kbyte instruction/data
	MPC860 PowerQUICC I Family (860, 860P, 855T, 862T, 862P, 857T)	PowerPC	50, 66, 80, 100	32	32	3.3	1.35	sleep, doze, power-down	16x16 MAC	No	4- to 16-kbyte instruction, 4- to 8-kbyte data, two-way set-associative
	MPC866 PowerQUICC I Family (866, 852T, 859T)	PowerPC	100, 133	32	32	1.8	0.26	normal low	16x16 MAC	No	4- to 16-kbyte instruction, 4- to 8-kbyte data, two-way set-associative
	MPC885 PowerQUICC I Family (885, 880, 875, 870)	PowerPC	66, 80, 133	32	32	1.8	0.43	normal low	16x16 MAC	No	8-kbyte instruction/data, two-way set-associative
	MPC8260 PowerQUICC II Family (8260, 8250, 8255, 8264, 8265, 8266)	PowerPC	266, 300	64	32	1.8-2.2	3	doze, stop		Yes	16-kbyte instruction/data, four-way set-associative

# 2003 Microprocessor directory

(by instruction set) 32-BIT MICROPROCESSORS

Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
Up to 12 64-kbyte RAM blocks, multiple configuration register file	SRAM, SSRAM, SDRAM, Flash		TQFP, RQFP, PQFP, BGA, FBGA	32-bit, watchdog, PWM, configurable	Configurable, RS232, SPI, GPIO, IDE, PCI, Ethernet	Up to 64, configurable		N/A - Core	Custom instructions, simultaneous multiple master bus	License, royalty-free in Altera PLDs
Up to 4-mbyte of Flash memory, up to 128-kbyte of SRAM	16- to 64-channel DMA.	TLB with up to 24 entries and memory protection	208 to 416 PBGA.	Up to 64 24-bit, up to 24 24-bit	Three 64-buffer FlexCAN, two eSCI with DMA, four DSPI with six CS and DMA, up to 214 GPIO	Up to 503 sources, interrupt controller	Two channel, 12-bit with six independently triggered queues, 800-kHz conversion	-40 to +125	Pin serialization, pin slew rate, drive control, FMPLL, system memory ECC, Nexus 3 debug interface	\$20 to \$55
512- to 1024-kbyte Flash, 32- to 40-kbyte RAM	SRAM, EPROM, EEPROM, Flash		388 PBGA	22, MIOS14	CAN, SCI, SPI	32 levels	16 to 20 channel, 10-bit with 64 result registers	-40 to +85	USIU	\$21.70 to \$33.97
448-kbyte Flash, 26-kbyte RAM	SRAM, EPROM, EEPROM, Flash		272 PBGA	50-channel timer system, two TPU3, MIOS1	CAN, SCI, SPI	32 levels	32 two-channel, 10-bit ADC with 64 result registers	-55 to +125	USIU	\$43.26
512- to 1024-kbyte Flash, 32- to 36-kbyte RAM	SRAM, EPROM, EEPROM, Flash		388 PBGA	54- to 70-channel timer systems; two or three TPU3, MIOS14	CAN, SCI, SPI	32 levels	32 to 40 two-channel, 10-bit ADC with 64 result registers	-55 to +125	USIU	\$21.70 to \$50.91
16-kbyte SDRAM on BestComm DMA controller, 512-kbyte SDRAM addressable	Glueless DDR controller; separate local, memory bus, BestComm DMA controller	32-bit instruction and data MMU	272 PBGA	Eight, decrements, two slice	Six peripheral serial controllers (I2S, AC97), SPI, 10/100 Ethernet, two USB, two CAN, two I2C, J1850 BDLC-D, up to 56 GPIO	Four external, eight GPIO with wakeup, six GPIO with interrupt		-40 to 85 (400 MHz) -40 to 105 (264 MHz)	Automotive qualified, PCI, ATA	\$22.50
8-kbyte DPRAM	EDO, EPROM, FLASH, DRAM, SDRAM, SRAM	32-entry TLB, fully associative	357 PBGA	Four 16-bit or two 32-bit	10/100 Ethernet, four serial controllers (Ethernet, HDLC, UTOPIA, Async HDLC, UART, BiSync, transparent), I2C, SPI, PCMCIA	Seven IRQ, 12 pins with interrupt capability, 23 internal		0 to +105 -40 to 115	Time slot assigner, parallel interface port, four baud rate generators, debug interface	\$27 to \$50
8-kbyte DPRAM	EDO, EPROM, FLASH, DRAM, SDRAM, SRAM	32-entry TLB, fully associative	357 PBGA	Four 16-bit or two 32-bit	10/100 Ethernet, four serial controllers (Ethernet, HDLC, UTOPIA, Async HDLC, UART, BiSync, transparent), I2C, SPI, PCMCIA	Seven IRQ, 12 pins with interrupt capability, 23 internal		0 to +95 -40 to +100	Time slot assigner, parallel interface port, four baud rate generators, debug interface	\$8 to \$45
8-kbyte DPRAM	EDO, EPROM, FLASH, DRAM, SDRAM, SRAM	32-entry TLB, fully associative	256/357 PBGA	Four 16-bit or two 32-bit	USB, two 10/100 Ethernet, three serial controllers (Ethernet, HDLC, UTOPIA, HDLC, Async UART, BiSync, transparent), I2C, SPI, PCMCIA	Six IRQ, 12 pins with interrupt capability, 23 internal		0 to +95 -40 to +100	Hardware security, Time slot assigner, parallel interface port, four baud rate generators, debug interface	\$9 to \$19
32-kbyte DPRAM	EDO, EPROM, FLASH, DRAM, SDRAM, SRAM	64-entry TLB, two-way set associative	480 TBGA	Four 16-bit or two 32-bit	Three controllers (10/100 Ethernet, ATM, transparent) two 128-channel HDLC/transparent controllers, four serial controllers (Ethernet, UTOPIA, HDLC, UART, BiSync, transparent), I2C, SPI, PCI, local bus	Eight IRQ, 24 external		0 to +105 -40 to 105	Time slot assigner, eight TDM interfaces, Transmission Convergence layer for ATM, IMA, parallel I/O, eight baud rate generators, debug interface, RTC	\$33 to \$120

# 2003 Microprocessor directory

32-BIT MICROPROCESSORS (by instruction set)

Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
	MPC8280 PowerQUICC II Family (8280, 8275, 8270)	PowerPC	266, 333, 450	64	32	1.5	2	doze, stop		Yes	16-kbyte instruction/data, four-way set-associative
	MPC8272 PowerQUICC II Family (8272, 8271, 8248, 8247)	PowerPC	266, 300, 400	64	32	1.5	1.2	doze, stop		Yes	16-kbyte instruction/data, four-way set-associative
	MP8560 PowerQUICC III	PowerPC	600MHz-1GHz (CPU), 333MHz (Communications Processor Module)	Local Bus PCI/PCI-X(64/64), RapidIO (8Bit)	32-bit	1.2V	8 W				L1: 32-kbyte instruction/data L2: 256-kbyte unified
	MP8540 PowerQUICC III	PowerPC	600MHz-1GHz	Local Bus PCI/PCI-X(64/64), RapidIO (8Bit)	32-bit	1.2V	7 W				L1: 32-kbyte instruction/data L2: 256-kbyte unified
	MP8555 PowerQUICC III	PowerPC	600MHz-833MHz (CPU), 333MHz (Communications Processor Module)	Local Bus PCI(32)/PCI(32/64)	32-bit	1.2V	8 W				L1: 32-kbyte instruction/data L2: 256-kbyte unified
Xilinx <a href="http://www.xilinx.com">www.xilinx.com</a>	PowerPC 405 embedded in Virtex-II PRO FPGA	PowerPC	600	64/32 (Core-Connect)	32	1.0 to 3.3 (FPGA usage)	0.9 mW/MHz	Yes	556 multipliers, user-definable DSP, two-cycle 32x32 multiply, 32x32 multiply/divide		16-kbyte instruction/data

# 2003 Microprocessor directory

(by instruction set) 32-BIT MICROPROCESSORS

Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
64-kbyte DPRAM	EDO, EPROM, FLASH, SDRAM, SRAM	64-entry TLB, two-way set associative	480 TBGA, 516 PBGA	Four 16-bit or two 32-bit	Three controllers (10/100 Ethernet, ATM, transparent) two 128-channel HDLC/transparent controllers, four serial controllers (Ethernet, UTOPIA, HDLC, UART, BiSync, transparent), I2C, SPI, PCI, local bus, USB	Eight IRQ, 24 external		0 to +105 -40 to 105	Time slot assigner, eight TDM interfaces, Transmission Convergence layer for ATM, IMA, parallel I/O, eight baud rate generators, debug interface, RTC	\$30 to \$90
20-kbyte DPRAM	EDO, EPROM, FLASH, SDRAM, SRAM	64-entry TLB, two-way set associative	516 PBGA	Four 16-bit or two 32-bit	Two controllers (10/100 Ethernet, ATM, transparent) three serial controllers (HDLC, UART, BiSync, transparent, QMC), I2C, SPI, PCI, USB	Eight IRQ, 24 external		0 to +105 -40 to 105	Hardware security, Time slot assigner, two TDM interfaces supporting 64 HDLC channels, parallel I/O, eight baud rate generators, debug interface, RTC	\$19 to \$32
64-kbyte DPRAM	DDR-1 SDRAM, SDRAM, DRAM, SRAM, Flash	L1: 64-entry, four-way set-associative TLB L2: 16-entry, fully associative TLB, variable page size, 256-entry, two-way set-associative TLB	783 FC-BGA	Four 16-bit or two 32-bit	Two 10/100/1000 Ethernet, three controllers (10/100 Ethernet, ATM transparent), two 128-channel HDLC/transparent controllers, four serial controllers (Ethernet, HDLC, UART, BISYNC, transparent), I2C, SPI, PCI/PCI-X, local bus, RapidIO	16 priority levels, 12 external, four with 32-bit messages, 22 internal		-40 to +110	Time slot assigner, eight TDM interfaces, Transmission Convergence layer for ATM, IMA, parallel interface port, four baud rate generators, debug interface, RTC	\$115 to \$144
64-kbyte DPRAM	DDR-1 SDRAM, SDRAM, DRAM, SRAM, Flash	L1: 64-entry, four-way set-associative TLB L2: 16-entry, fully associative TLB, variable page size, 256-entry, two-way set-associative TLB	783 FC-BGA	Four 16-bit or two 32-bit	Two 10/100/1000 Ethernet, DUAR TI2C, PCI/PCI-X, local bus, RapidIO	16 priority levels, 12 external, four with 32-bit messages, 22 internal		-40 to +110		\$88 to \$110
64-kbyte DPRAM	DDR-1 SDRAM, SDRAM, DRAM, SRAM, Flash	L1: 64-entry, four-way set-associative TLB L2: 16-entry, fully associative TLB, variable page size, 256-entry, two-way set-associative TLB	783 FC-BGA	Four 16-bit or two 32-bit	Two 10/100/1000 Ethernet, two controllers (10/100 Ethernet, ATM, transparent) QMCI, three serial controllers (Ethernet, HDLC, UART, BISYNC, transparent), I2C, SPI, USB, RapidIO	16 priority levels, 12 external, four with 32-bit messages, 22 internal		-40 to +110	IPSec/SSL, time slot assigner, three TDM interfaces, parallel interface port, four baud rate generators, debug interface, RTC	\$88 to \$126
72- to 3456-kbyte, 216- to 10,006-kbit	SDRAM, DDR, SRAM, Flash, ZBT, SDARM (soft IP)	Embedded MMU	Virtex/E, SpartanII, SpartanIIE, Spartan3, VirtexII, VirtexII PRO	PIT, FIT, watchdog	CoreConnect-enabled UART, I <sup>2</sup> C, GPIO, SPI, 16450/550, EMAC10/100, UART lite, 1-Gigabit Ethernet	Core-Connect enabled controller, PowerPC interrupt capability		0 to +70 -40 to +85 -40 to +125	1200 I/O and 125,126 logic cells, chip scope PRO for FPGA debugging	From \$40

# 2003 Microprocessor directory

32-BIT MICROPROCESSORS (by instruction set)

Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Motorola <a href="http://www.motorola.com/semiconductors">www.motorola.com/semiconductors</a>	MCore family	RISC	16 to 33	32, external: MCore	16	1.8 to 3.6	0.09 to 0.66	Stop: 200 mA, wait: 19 mA, dose: 14 mA			
NetSilicon <a href="http://www.netsilicon.com">www.netsilicon.com</a>	NET+40	RISC	33	28/32	16, 32	3.3	15 mW/MHz		Yes		4-kbyte instruction/data
	NET+50	RISC	44	28/32	16, 32	2.5/3.3	480 mW		Yes		8-kbyte instruction/data
	NS7520	RISC	55	28/32	16, 32	1.5/3.3	500 mW		Yes		
STMicroelectronics <a href="http://www.st.com">www.st.com</a>	ST40RA (SH-4 core)	SH4	150, 166, 200	14/64 SDRAM, 26/32 peripheral, 32	16	1.8/3.3	980 mW	Three	64-bit FPU with vector operations	Single- and double-precision, IEEE-754, 3-D vector and matrix, transcendental functions	8-/16-kbyte instruction/data RAM/cache mode
Intel <a href="http://www.intel.com">www.intel.com</a>	IXC1100	StrongARM v5TE	266, 400, 533	24/16	16, 32	0.3 to 2.1	1.0 to 1.2 W	Stop, halt	40-bit accumulator DSP Co-processor		32-kbyte instruction/data 32-way set associative, 2-kbyte mini data cache
	IXP420	StrongARM v5TE	266	24/16	16, 32	0.3 to 2.1	1.0 W	Stop, halt	40-bit accumulator DSP Co-processor		32-kbyte instruction/data 32-way set associative, 2-kbyte mini data cache
	IXP421	StrongARM v5TE	266	24/16	16, 32	0.3 to 2.1	1.0 W	Stop, halt	40-bit accumulator DSP Co-processor		32-kbyte instruction/data 32-way set associative, 2-kbyte mini data cache
	IXP422	StrongARM v5TE	266	24/16	16, 32	0.3 to 2.1	1.0 W	Stop, halt	40-bit accumulator DSP Co-processor		32-kbyte instruction/data 32-way set associative, 2-kbyte mini data cache
	IXP425	StrongARM v5TE	266, 400, 533	24/16	16, 32	0.3 to 2.1	1.0 W	Stop, halt	40-bit accumulator DSP Co-processor		32-kbyte instruction/data 32-way set associative, 2-kbyte mini data cache
Renesas Technology <a href="http://www.renesas.com">www.renesas.com</a>	SH-2 Series SH7047F	SuperH	50	32/32	16	4.5 to 5.5	220 to 235 mA	Four	32x32+64		
	SH-2 Series SH7145F	SuperH	50	32/32	16	3.3	160 to 220 mA	Four	32x32+64		

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(by instruction set) 32-BIT MICROPROCESSORS

Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
128- to 256-kbyte Flash, 8- to 32-kbyte RAM	22- and 16-bit address bus, SRAM		100 LQFP, 144LQFP, 196 MAPBGA	Two	ISSI, SCI, SPI, Dual SCI	8 external	Up to eight channel, 8-bit	0 to +70 -40 to +85		
Cache optionally configurable as 8 kbyte of RAM	SRAM, SDRAM, EDO DRAM, Flash, 10-channel DMA		208 PQFP	Two 27-bit, watchdog, bus	Two UART, two HDLC, two SPI, 24 PIO, four 1284, 10/100BaseT Ethernet MAC	Four external		-40 to +85	Co-processor interface	\$24.95
Cache optionally configurable as 16-kbyte of RAM	SRAM, SDRAM, EDO DRAM, Flash, 10-channel DMA		208 PQFP, 208 BGA	Two 27-bit, watchdog, bus	Two UART, two HDLC, two SPI, 40 PIO, four 1284, 10/100BaseT Ethernet MAC	36 external		-40 to +85	Co-processor interface	\$13.95 to \$16.95
	SRAM, SDRAM, EDO DRAM, Flash, 13-channel DMA		177 BGA	Two 27-bit, watchdog, bus	Two UART, two HDLC, two SPI, 16 PIO, four 1284, 10/100BaseT Ethernet MAC	Four external		-40 to +85		\$9.95
RAM/cache mode, 8-kbyte RAM/data cache	64-bit SDRAM/DDR Flash, burst Flash, SRAM, SDRAM, five-channel DMA	64-entry fully-associative UTLB, four-entry fully associate microTLB	372 PBGA	Three 32-bit, real-time	Two UART, PCI, 24 PIO	17, four external, NMI		0 to +70 -40 to +85	JTAG, real-time trace	\$19.95 (166 MHz)
8-kbyte RAM	SRAM, Flash, PC133-SDRAM	32-entry, full-way associative and TLB	492 PBGA	Four 32-bit, watchdog	Two UART, 32-bit 33/66-MHz PCI bus v2.2, USB 1.1, two 10/100 Ethernet MAC, 16 GPIO	32, eight highest priority		-40 to +85	JTAG debug	\$20 to 63
8-kbyte RAM	SRAM, Flash, PC133-SDRAM	32-entry, full-way associative and TLB	492 PBGA	Four 32-bit, watchdog	Two UART, 32-bit 33/66-MHz PCI bus v2.2, USB 1.1, two 10/100 Ethernet MAC, 16 GPIO	32, eight highest priority		0 to +70	JTAG debug	\$20
8-kbyte RAM	SRAM, Flash, PC133-SDRAM	32-entry, full-way associative and TLB	492 PBGA	Four 32-bit, watchdog	Two UART, 32-bit 33/66-MHz PCI bus v2.2, USB 1.1, 10/100 Ethernet MAC/ATM, UTOPIA II multi-PHY/slave, 16 GPIO	32, eight highest priority		0 to +70	Two HSS, JTAG debug, eight-channel HDLC	\$22
8-kbyte RAM	SRAM, Flash, PC133-SDRAM	32-entry, full-way associative and TLB	492 PBGA	Four 32-bit, watchdog	Two UART, 32-bit 33/66-MHz PCI bus v2.2, USB 1.1, two 10/100 Ethernet, 16 GPIO	32, eight highest priority		0 to +70	AES/DES/DES3, SHA-1/MD-5, JTAG debug	\$21
8-kbyte RAM	SRAM, Flash, PC133-SDRAM	32-entry, full-way associative and TLB	492 PBGA	Four 32-bit, watchdog	Two UART, 32-bit 33/66-MHz PCI bus v2.2, USB 1.1, two 10/100 Ethernet MAC/ATM, UTOPIA II multi-PHY/slave, 16 GPIO	32, eight highest priority		-40 to +85	JTAG debug, Two HSS, AES/DES/DES3, eight-channel HDLC	\$25 to \$65
256-kbyte of Flash, 12-kbyte RAM	ROM, SRAM		100 QFP	Two to five 16-bit, six-phase PWM, watchdog	Three serial, CAN	49, five external	Two eight-channel, 10-bit ADC	-40 to +85	Data-transfer controller, on-chip debug	\$11
256-kbyte of Flash, 8-kbyte RAM	SRAM, ROM, four-channel DMAC		144 LQFP	Two to five 16-bit, watchdog	Four serial, I <sup>2</sup> C	51, nine external	Eight channel, 10 bit	-40 to +85	Data-transfer controller, on-chip debug	\$10

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32-BIT MICROPROCESSORS (by instruction set)

Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
	SH-3 DSP Series SH7729	SuperH	200	32/32, external: 29	16	2.0/3.3	1W	Four	32x32+64		16-kbyte four-way set associative
	SH-3 Series SH7705	SuperH	133	32/32, external: 29	16	1.5/3.3	250 mW	Four	32x32+64		32-kbyte four-way set associative
	SH-4 Series SH7750R	SuperH	240	32/64, external: 29	16	1.5/3.3	345 mW	Four	32x32+64	Single- and double-precision	16-/32-kbyte instruction/data
	SH-4 Series SH7751R	SuperH	240	32/32, external: 29	16	1.5/3.3	382 mW	Four	32x32+64	Single- and double-precision	16-/32-kbyte instruction/data
SuperH <a href="http://www.superh.com">www.superh.com</a>	SH-4 CPU core soft/hard cores	SuperH 16	Soft core up to 600	32, external: 9, 8 to 1024 (definable) 64 paths	16	Process dependent	0.15 to 0.7 mW/MHz	Sleep, standby, module standby, clock-domain frequency control	Four 32x32 floating-point multipliers, three 32-bit floating-point adders	Single- and double-precision, IEEE-754, 3-D vector and matrix, transcendental functions	Implementation-dependent, direct mapped and two-way set associative options.
	SH4-202 CPU hard core	SuperH 16	266 (worst case)	32, external: 9, 8 to 1024 (definable) 64 paths	16	1.2	180 mW	Sleep, standby, module standby, clock-domain frequency control	Four 32x32 floating-point multipliers, three 32-bit floating-point adders	Single- and double-precision, IEEE-754, 3-D vector and matrix, transcendental functions	16-/32-kbyte instruction/data two-way set associative, LRU, write-back/write-through selectable, RAM/cache mode
Toshiba America Electronic Components <a href="http://www.toshiba.com">www.toshiba.com</a>	900/H1 family	TLCS	8 to 40	24/16	8, 16, 32	3 to 3.6	30	Idle2: 4.5 mA idle1: 2 mA stop: 1.0 mA	16x16 to 32-bits signed/unsigned		
	900/H2 family	TLCS	20	24/16	8, 16, 32	4.5 to 5.5	90	Run: 50 mA idle: 5 mA stop: 0.5 mA	16x16 to 32-bits signed/unsigned		
Infineon Technologies <a href="http://www.infineon.com/microcontrollers">www.infineon.com/microcontrollers</a>	TC1765	TriCore V1.2	40	32/16/8	16, 32	2.5/3.3 to 5	675 mW	Idle, sleep, deep sleep	Dual MAC, signed fraction, modulo, bit-reverse, pre/post-increment, saturation, rounding		1-kbyte instruction, two-way set associative
	TC1775	TriCore V1.2	40	32/16/8	16, 32	2.5/3.3 to 5	675 mW	Idle, sleep, deep sleep	Dual MAC, signed fraction, modulo, bit-reverse, pre/post-increment, saturation, rounding		1-kbyte instruction, two-way set associative
	TC111B	TriCore V1.3	96	32/16/8	16, 32	1.8/3.3	900 mW	Idle, sleep, deep sleep	Dual MAC, signed fraction, modulo, bit-reverse, pre/post-increment, saturation, rounding		8-kbyte instruction/data two-way set associative

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(by instruction set) 32-BIT MICROPROCESSORS

Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
16-kbyte RAM: 8-kbyte X and 8-kbyte Y memory	SDRAM, SRAM, ROM, four-channel DMAC	Yes	208 LQFP, 216 TFBGA	Three 32-bit, real-time	Three serial, IrDA	27, 19 external	Eight-channel, 10-bit ADC; two-channel, 8-bit DAC	-40 to +85	Smart-card interface, on-chip debug	\$17.50
	SDRAM, SRAM, ROM, four-channel DMAC	Yes	208C FP, 208A TBP	Three 32-bit, three 16-bit, real-time, watchdog	Two serial, USB	27, 23 external	Four channel, 10-bit	-40 to +85	Smart-card interface, on-chip debug	\$10
	SDRAM, SRAM, ROM, eight-channel DMAC	Yes	208E FP, 256 BP	Three 32-bit, real-time	Two serial	34, 16 external		-40 to +85	Smart-card interface, on-chip debug	\$22
	SDRAM, SRAM, ROM, eight-channel DMAC	Yes	208E FP, 256 BP	Five 32-bit, real-time	Two serial, PCI	39, 16 external		-40 to +85	Smart-card interface, on-chip debug	\$25
Application dependent	External, application dependent	64-entry fully-associative UTLB, four-entry fully associate microTLB	Application dependent	Application dependent	Application dependent	128+, four external, 16 levels	Application dependent	N/A - Core supports -55 to +125	SuperHyway VSI compliant interconnect, UDI (JTAG), 1-kbyte debug RAM, AUD trace, hardware break points	License
Application dependent	External, application dependent	64-entry fully-associative UTLB, four-entry fully associate microTLB	Application dependent	Three 32-bit, watchdog, real-time with alarm and calendar functions	Full-duplex serial with 16-byte send/receive FIFOs, modem control, baud rate generator	128+, four external, 16 levels	Application dependent	0 to +70	SuperHyway VSI compliant interconnect, UDI (JTAG), 1-kbyte debug RAM, AUD trace, hardware break points	License
Up to 256-kbyte of ROM, 32-kbyte RAM	SDRAM, eight micro DMA channels	Yes	100 LQFP, 144 LQFP	Up to eight 8-bit, up to two 16-bit, 22-bit, watchdog, real-time,	Up to three UART, synchronous SIO, SEI, CAN, IrDA, I2C, up to 70 PIO	40, nine CPU, four external, seven levels	Up to 12 channel, 10-bit		Four 32-bit register banks, LCD controller	\$5 to \$8
Up to 512-kbyte of ROM, 16-kbyte RAM	Four micro DMA channels		100 QFP, 160 QFP, 100 LQFP	Up to eight 8-bit, up to four 16-bit, 22-bit watchdog	Two UART, synchronous SIO, two SEI, CAN, up to 70 PIO	18, 10 external, seven levels	12-channel (maximum), 10-bit ADC; two-channel, 8-bit DAC		Four 32-bit register banks	\$7.25 to \$10
48-kbyte SRAM	32-bit, glueless, burst mode, DMA		260 PLBGA	Three 32-bit, 34 24-bit, 64 16-bit	TwinCAN, two SSC/SPI, two ASC, 77 PIO, 24 analog input	More than 100 IRQ nodes	Dual 12-channel, 8/10/12-bit	-40 to +125	Prescaler, duty cycle, phase discrimination, digital PLL	\$22
92-kbyte SRAM	32-bit, glueless, burst mode		329 PBGA	Three 32-bit, 34 24-bit, 64 16-bit	TwinCAN, J1850, two SSC/SPI, two ASC, 11 16-bit parallel port	More than 100 IRQ nodes	Dual 16-channel, 8/10/12-bit	-40 to +125	Peripheral-control processor, prescaler, duty cycle, phase discrimination, digital PLL	\$27
1.5-Mbyte eDRAM, 68-kbyte SRAM	32-bit, glueless, burst mode, PC100 support	Yes	388 PBGA	Six 32-bit (usable as 8- and 16-bit)	PCI, fast Ethernet, SSC/SCI, ASC (IrDA), MMCI, 96 PIO	86, 24 external		-25 to +85	Peripheral control processor	\$65

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32-BIT MICROPROCESSORS (by instruction set)

Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
	TC1910	TriCore V1.3	66	32/16/8	16, 32	1.8/3.3		Idle, sleep, deep sleep	Dual MAC, signed fraction, modulo, bit-reverse, pre/post-increment, saturation, rounding		8-kbyte instruction/data two-way set associative
	TC1912	TriCore V1.3	66	32/16/8	16, 32	1.8/3.3		Idle, sleep, deep sleep	Dual MAC, signed fraction, modulo, bit-reverse, pre/post-increment, saturation, rounding		8-kbyte instruction/data two-way set associative
	TC1920	TriCore V1.3	100	32/16/8	16, 32	1.8/3.3		Idle, sleep, deep sleep	Dual MAC, signed fraction, modulo, bit-reverse, pre/post-increment, saturation, rounding		8-kbyte instruction/data two-way set associative
Toshiba America Electronic Components <a href="http://www.toshiba.com">www.toshiba.com</a>	TMPR 3911BU 3911BxB	TX	58.9	13 to 26/ 16 to 32	32	2.6/3.3	150 mW	Doze, sleep	One-cycle 32x32+64 MAC		4-kbyte instruction, 1-kbyte data, direct map, two-way set associative
	TMPR 3912AU-92 3912XB-92	TX	92	13 to 26/ 16 to 32	32	3.3	360 mW	Doze, sleep	32x32+64 MAC		4-kbyte instruction, 1-kbyte data, LRU, two-way set associative
	TMPR 3922CU	TX	129	13 to 26/ 16 to 32	32	2.7/3.3	500 mW	Doze, sleep	One-cycle 32x32+64 MAC		16-kbyte instruction, 8-kbyte data, LRU, two-way set associative
	TMPR 3927CF	TX	133	20 to 28/ 16 to 32	32	2.5/3.3	1.0 W	Reduced frequency, doze, halt	One-cycle 32x32+64 MAC		8-kbyte instruction, 4-kbyte data, LRU, two-way set associative
	TMPR3916F	TX	60	26/16 to 32	32	3.3	1.2 W	Doze, sleep	One-cycle 32x32+64 MAC		4-kbyte instruction, 1-kbyte data, direct map, two-way set associative
NEC Electronics America <a href="http://www.necelam.com">www.necelam.com</a>	V850/V850S	V800	2 to 33	24/16	32	2.7 to 5.5	56 to 480 mW	Halt, idle, stop	16x16		
	V850E1	V800	2 to 150	24/16, 26/32	32	1.5 to 3.6/ 3.0 to 5.5	270 to 630 mW	Halt, idle, stop	32x32		Yes
	V850ES/Kx1	V800	2 to 20	24/16	32	2.7 to 5.5	27 to 150 mW	Halt, idle, stop	16x16		Yes
	V850ES/SAx	V800	2 to 20	24/16	32	2.2 to 5.5	30 to 105 mW	Halt, idle, stop	16x16		Yes

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(by instruction set) 32-BIT MICROPROCESSORS

Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
144-kbyte SRAM	32-bit, glueless, burst mode	Yes	208 PLBGA	Three 32-bit	SSC/SPI, two ASC, I <sup>2</sup> C	More than 100 IRQ nodes	Dual 14-bit CODEC	-40 to +85	Peripheral control processor, PLL	\$18
144-kbyte SRAM	32-bit, glueless, burst mode	Yes	208 PLBGA	Three 32-bit	TwinCAN, SSC/SPI, three ASC, I <sup>2</sup> C	More than 100 IRQ nodes	Dual 14-bit CODEC	-40 to +85	Peripheral control processor, PLL	\$18.50
164-kbyte SRAM	32-bit, glueless, burst mode	Yes	260 PLBGA	Six 32-bit	TwinCAN, J1850, SSC/SPI, three ASC, two I2C	More than 100 IRQ nodes	Six channel, 8/10/12-bit, dual 14-bit CODEC	-40 to +85	Peripheral control processor, PLL	\$27
	SDRAM, DRAM, SRAM, ROM, Flash	32-entry, 4-kbyte pages	176 LQFP, 177 BCSP	Real-time, watchdog	UART, CHI, IrDA, SPI, 39 PIO	Up to 39 external			Codec I/F (softmodem, voice recognition/synthesis)	\$9
	SDRAM, DRAM, SRAM, ROM, Flash	32-entry, 4-kbyte pages	208 LQFP, 217 FBGA	Real-time, watchdog	UART, CHI, IrDA, SPI, 39 PIO	Up to 39 external			Codec I/F (softmodem, voice recognition/synthesis)	\$15
	SDRAM, DRAM (EDO), SRAM, ROM, Flash	64-entry, 4-kbyte to 4-mbyte pages	208 LQFP	Two, watchdog	UART, CHI, IrDA, SPI, 48 PIO	Up to 48 external			Companion chip TC6358TB	\$28
	SDRAM, SGRAM, DIMM, Flash, SMROM, SRAM, ROM, DMA	64-entry, 4-kbyte to 4-mbyte pages	240 PQFP	Three 32-bit, watchdog	Two UART, 16 PIO	Six external			Debug support unit	\$17
	SDRAM, DRAM, SRAM, ROM, Flash, two DMA	32-entry, 4-kbyte pages	208 LQFP	Two 16-bit	Four UART, two-channel CAN (16 mailboxes), 30 PIO	Three external, NMI	Three-channel, 6-bit RGB DAC		Digital RGB	\$20
Up to 512-kbyte of ROM/Flash, up to 24-kbyte of SRAM	Four DMA		LQFP, FBGA	Up to 10 16-bit, four PWM	UART, CSI, I <sup>2</sup> C	12 external	Up to 16 channel, 10-bit	-40 to +85		\$5.50 to \$15
Up to 128-kbyte of ROM/Flash, up to 4-kbyte of SRAM	EDO SDRAM, SRAM, four DMA		LQFP, FBGA	Up to 12 16-bit, six PWM	UART, CSI, I <sup>2</sup> C, USB	Up to 32 external	Up to eight channel, 10-bit	-40 to +85	ROM correction	\$8 to \$24
Up to 128-kbyte of ROM/Flash, up to 6-kbyte of SRAM			LQFP, FBGA	Up to 10 16-bit	UART, CSI, I <sup>2</sup> C	Eight external	Six-channel (maximum), 16-bit ADC; two-channel, 8-bit DAC	-40 to +85	ROM correction	\$4.50 to \$13
Up to 256-kbyte of ROM/Flash, up to 16-kbyte of SRAM			LQFP, FBGA	Up to 10 16-bit	UART, CSI, I <sup>2</sup> C	Eight external	Up to six channel, 16-bit	-40 to +85		\$4.50 to \$13

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32-BIT MICROPROCESSORS (by instruction set)

Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
AMD www.amd.com	ElanSC520	x86	100, 133	32, external: 26/16	32	3.3/ 5 tolerant	1.4W			Yes	16-kbyte writeback
Intel www.intel.com	80386DX	x86	16, 20, 25, 33	32/32	32	5	300 mA				
	80386EX 80386EXTB	x86	25, 33 25	32, external: 26/16	32	3.3 to 5	250 to 320 mA	Idle, powerdown			
	80386SSX 80386SX	x86	25, 33, 40		32	5					
	80486DX2 80486DX4	x86	50, 66 100	32/32	32	3.3/ 5 tolerant	318 to 395 mA 825 to 1075 mA	Stop, auto halt/idle powerdown		32-, 64-, 80-bit formats	8- or 16-kbyte instruction/data write-back
	80486SX 80486GX 80486SSX	x86	33	32/16	32	3.3/ 5 tolerant	220 to 289 mA 180 to 220 mA	Stop clock, auto halt powerdown			8-kbyte instruction/data write-through
	Celeron	x86	650	32/32	32	1.15	8.3W	Autohalt, stopgrant, sleep, deepsleep		Yes	L1: 16-kbyte instruction/data L2: 256-kbyte
	Celeron CuMine	x86	300, 400	32/32	32	1.1 to 1.35	5.7 to 10.1W	Autohalt, stopgrant, sleep, deepsleep		Yes	L1: 16-kbyte instruction/data L2: 128-kbyte
	Celeron Northwood	x86	300, 366, 433, 566, 733	32/32	32	1.5 to 1.75	17.8 to 52.8W	Autohalt, stopgrant, sleep, deepsleep		Yes	L1: 16-kbyte instruction/data L2: 128/256-kbyte
	Celeron Tualatin	x86	400, 650,	32/32	32	0.95 to 1.1	4.2 to 8.3W	Autohalt, stopgrant, sleep, deepsleep		Yes	L1: 16-kbyte instruction/data L2: 256-kbyte
	LV Xeon	x86	1600, 2000	32/32	32	1.30	30 to 35W	Autohalt, stopgrant, sleep			L1 and L2: 512-kbyte
	Pentium 4	x86	2000, 2400	36/32	32	1.50	52.4 to 57.8W	Autohalt, stopgrant, sleep, deepsleep		Yes	L1: 8-kbyte data L2: 512-kbyte
	Pentium 4M	x86	1700	36/32	32	1.30	30W	Autohalt, stopgrant, sleep, deepsleep, deeper sleep		Yes	L1: 8-kbyte data L2: 512-kbyte
	Pentium III	x86	800	32/32	32	1.15	11.2W	Autohalt, stopgrant, sleep, deepsleep		Yes	L1: 16-kbyte instruction/data L2: 512-kbyte
	Pentium III CuMine	x86	500, 700	32/32	32	1.35	10.1 to 12.2W	Autohalt, stopgrant, sleep, deepsleep		Yes	L1: 16-kbyte instruction/data L2: 256-kbyte
	Pentium III CuMine/ Tualatin	x86	600, 700, 733, 850, 866	32/32	32	1.45 to 1.75	19.6 to 29.5W	Autohalt, stopgrant, sleep, deepsleep		Yes	L1: 16-kbyte instruction/data L2: 256- to 512-kbyte
	Pentium III Tualatin	x86	800, 933	32/32	32	1.15	11.2 to 12.2W	Autohalt, stopgrant, sleep, deepsleep		Yes	L1: 16-kbyte instruction/data L2: 512-kbyte
	Xeon	x86	2000, 2400	32/32	32	1.50	58 to 65W	Autohalt, stopgrant, sleep			L1 and L2: 512-kbyte

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(by instruction set) 32-BIT MICROPROCESSORS

Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
See cache	SDRAM, Flash, ROM, SRAM, EPROM	Standard 486 MMU plus 16 programmable address regions	388 PBGA	Programmable interval, general purpose, software, real-time, watchdog	Two 16650 UART, synchronous serial, 32 PIO, PCI bus rev. 2.2	22 levels		0 to +85 -40 to +85	Integrated PC-AT peripherals, AMDebug on-chip debug, JTAG debug	\$19.74 to \$22.70
			132 PGA/PQFP			Maskable, NMI				\$5.90 to \$21
	Refresh control unit		144 TQFP, 100/132 PQFP	32-bit down-counter, watchdog	UART, SIO, three 8-bit GPIO	10				\$8 to \$10.40
										\$5.12 to \$5.20
			208 SQFP, 168 PGA			Reset, maskable, NMI				\$15.20 to \$26.33 \$16.80 to \$29.28
			168 PGA, 196 PQFP, 176 TQFP			Reset, maskable, NMI				\$28.75 to \$33.25 \$6.40 (SSX)
			MicroFCBGA						Streaming SIMD extensions	\$116
			BGA2					0 to +100	Streaming SIMD extensions	\$45 to \$50
			FCPGA, FCPGA2					0 to +90 (566 MHz) 0 to +70 (2000 MHz)	Streaming SIMD extensions	\$35 to \$65
			Micro FCBGA					0 to +100	Streaming SIMD extensions	\$35 to \$94
			604 FCmPGA2p						Hyperthreading technology	\$220, \$250
			MicroFCPGA2						Rapid execution engine, hyper pipelined, dynamic execution, SSE2 instructions, NetBurst microarchitecture	\$393, \$191
			MicroFCPGA						Rapid execution engine, hyper pipelined, dynamic execution, SSE2 Instructions, NetBurst microarchitecture	\$236
			MicroFCBGA						Dual-processor-capable, streaming SIMD extensions	\$273
			BGA2					0 to +100	Streaming SIMD extensions	\$90 to \$119
			FCPGA, FCPGA2					0 to +82 (600 MHz) 0 to +69 (1.26 GHz)	Dual-processor-capable, streaming SIMD extensions	\$75 to \$115
			MicroFCBGA					0 to +100	Streaming SIMD extensions	\$183 to \$231
			603 INT3, 604 FCmPGA2p						Hyperthreading technology	\$194, \$183

# 2003 Microprocessor directory

32-BIT MICROPROCESSORS (by instruction set)

Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
National Semiconductor <a href="http://www.national.com">www.national.com</a>	Geode GX1	x86	200 to 333	64/64, external: PCI 32	8, 16, 32, 48	1.8 to 2.2/3.3	1.2 W	Active idle: 0.6 W standby: 170 mW sleep: 140 mW	(8, 16, 32)x(8, 16, 32), MMX instructions	IEEE-754 compatible, single-precision, 64 or 80 bits	16-kbyte instruction/data
	Geode GX2	x86	333 to 400	64/64, external: PCI 32	8, 16, 32, 48	1.5/3.3	1 to 2 W	Active idle: 1.4 W standby: less than 300 mW	(8, 16, 32)x(8, 16, 32), MMX and 3DNow instructions	IEEE-754 compatible, single-precision, 64 or 80 bits	16-kbyte instruction/data
	Geode SOC	x86	200 to 300	64/64, external: PCI 32	8, 16, 32, 48	1.8 to 2.1/3.3	1.6 to 2.1 W	Active idle: 1.5 W standby: 110 mW	(8, 16, 32)x(8, 16, 32), MMX instructions	IEEE-754 compatible, single-precision, 64 or 80 bits	16-kbyte instruction/data
STMicroelectronics <a href="http://www.st.com">www.st.com</a>	STPC Atlas Consumer-II Elite	x86	66 to 133	64	32	2.5/3.3, 5 tolerant	3W	Three		8087 compatible, IEEE-754, single and double precision	8K unified or instruction/data
	STPC Vega	x86	66 to 200	64	32	1.8/3.3, 5 tolerant	1.85W	Three		8087 compatible, IEEE-754, single and double precision	8K unified or instruction/data
Transmeta <a href="http://www.transmeta.com">www.transmeta.com</a>	Crusoe TM5800 TM5500	x86	Up to 1000	32	32	0.9 to 1.3	1 W	Auto-halt, quick start, deep sleep	Yes	Yes	L1: 64-kbyte instruction/data L2: 512-kbyte
VIA Technologies <a href="http://www.viatech.com">www.viatech.com</a>	Antaur	x86	1.0 to 1.2 GHz	32/64		1.25	12 W	Autohalt, stopgrant, sleep, deepsleep		Yes	L1: 64-kbyte instruction/data L2: 64-kbyte
	C3	x86	800	32/64		1.65	17 W	Autohalt, stopgrant, sleep, deepsleep		Yes	L1: 64-kbyte instruction/data L2: 64-kbyte
	C3	x86	1.0 to 1.2 GHz	32/64		1.45	17 W	Autohalt, stopgrant, sleep, deepsleep		Yes	L1: 64-kbyte instruction/data L2: 64-kbyte
	Eden	x86	400 to 733	32/64		1.05, 1.15	6 W	Autohalt, stopgrant, sleep, deepsleep		Yes	L1: 64-kbyte instruction/data L2: 64-kbyte
Tensilica <a href="http://www.tensilica.com">www.tensilica.com</a>	Xtensa V	Xtensa	350 (worst case 0.13)	32/32, 64, 128 (custom)	16, 24 modeless mix	Process dependent	0.1 mW/MHz (0.13, 1.0 V)	Powerdown during wait	Five 16x16, 32x32 Vectra DSP co-processor options, user instructions, options: 16x16 MAC, 16x16 and 32x32 multiply	Configuration option, IEEE-754 compatible	Configurable: 0- to 32-kbyte instruction/data four-way set associative

# 2003 Microprocessor directory

(by instruction set) 32-BIT MICROPROCESSORS

Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
1-Gbyte SDR SDRAM	64-bit SDRAM, 66 to 111 MHz, four 168-pin DIMMs, 1-Gbyte total	32-entry, four way set associative TLB	352 EBGA			Standard PC/AT-compatible, PCI IRQ native		0 to +85	2-D graphics accelerator, display controller, PCI host controller	\$27 to \$35
1-Gbyte DDR/SDR SDRAM	64-bit SDR (66 to 133) or DDR (133 to 266) SDRAM, four banks, 1-Gbyte total	Eight-entry fully associative instruction and data L1 TLB, 64-entry two-way associative instruction and data L2 TLB	368 BGA			Standard PC/AT compatible, SERIRQ, PCI IRQ native		0 to +85	2-D graphics accelerator, display controller, PCI host controller	\$35 to \$41
1-Gbyte SDR SDRAM	64-bit SDRAM, 66 to 100 MHz, two banks, 1-Gbyte total	32-entry, four-way set associative TLB	432 EBGA, 481 TEPBGA	ACPI, watchdog	Three UART, parallel printer port, IR, three USB, up to 27 PIO	Standard PC/AT compatible, SERIRQ, PCI IRQ native		0 to +85	2-D graphics accelerator, display controller, PCI host controller, audio	\$26 to \$38
	64-bit SDRAM UMA controller	PC Compatible	388 or 516 PBGA	PC-compatible	PCI, ISA, EIDE, PCMCIA, I <sup>2</sup> C, keyboard, mouse, USB, UART	PC-compatible		0 to +85 -40 to +115	VGA, SVGA, TFT controller, video input/output port	\$20 to \$30
	64-bit SDRAM controller	PC Compatible	388 PBGA	PC-compatible	PCI, ISA, EIDE, I <sup>2</sup> C, UART, USB Host, Ethernet	PC-compatible		0 to +85		\$28 to \$40
	64-bit DDR, SDR	Yes	474 BGA					0 to +100		\$85 to \$200
			EBGA					0 to +85 (Tase)	3DNow!	\$70 to \$150
			EBGA					0 to +70 (Tase)	3DNow!	\$45
			EBGA					0 to +85 (Tase)	Streaming SIMD extensions	\$50
			EBGA					0 to +85 (Tase)	3DNow!	\$50 to \$100
Configurable local memories for instruction/data, up to 256-kbyte RAM and ROM, XLMI interface to other memories or tightly coupled hardware		Optional and configurable	Application dependent	Up to three 32-bit		Up to 32		N/A - Core	Automated processor-generation system creates new processor and tool suite in one hour	License