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64-BIT MICROPROCESSORS (by company)

Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
Broadcom www.broadcom.com	BCM1125H	MIPS 64	400 to 1 GHz	256 (internal bus)	64	1.2	3 to 6 W (400 to 800 MHz)		8-bit MDMX	Two 64-bit FPUs with paired-single and MIPS-3D	L1: 32-kbyte instruction/data per core, L2: 256-kbyte shared, four-way set associative
	BCM1250	MIPS 64	600 to 1 GHz	256 (internal bus)	64	1.2	10 W (800 MHz)		8-bit MDMX	Two 64-bit FPUs with paired-single and MIPS-3D for each CPU	L1: 32-kbyte instruction/data per core, L2: 512-kbyte shared, four-way set associative
MIPS Technologies www.mips.com	20Kc	MIPS64	600	36/64	32	1.0	2.5 mW/MHz (0.13)	Wait	32x32, 32x64, 64x64	64-bit paired-single with MIPS-3D	32-kbyte instruction/data
	5Kc 5Kf	MIPS64	310 to 350	36/64	32	Process dependent	0.17 to 1 mW/MHz	Wait	32x32, 32x64, 64x64	Optional, IEEE-754-compliant	0- to 64-kbyte instruction/data
NEC Electronics America www.necelam.com	VR4131	MIPS64	200	64, external: 32/16	16, 32	1.5/3.3	220 mW	Standby, suspend, exsuspend, hibernate	Single-cycle 32x32+64 MAC		16-kbyte instruction/data two-way set associative
	VR4133	MIPS64	266	32	16	1.5/3.3	370 mW	Full speed, standby, suspend, exsuspend, hibernate	IPSec engine		16-kbyte instruction/data
	VR4181A	MIPS64	131	64, external: 32/16	16, 32	2.5/3.3	250 mW	Standby: 100 mW suspend: 50 mW hibernate: 165 mW			8-kbyte instruction/data direct mapped
	VR5432	MIPS64	167	64, external: 32	32	2.5/3.3	1.8 W		32x32+64 MAC and barrel shift, special instructions	IEEE-754, 64-/32-bit floating-point arithmetic and multiply	32-kbyte instruction/data two-way set associative, line locking
	VR5500	MIPS64	300 to 400	64, external: 64, 32 option	32	1.5/3.3	1.5 W	Standby	MAC, 32x32 and 64x64 floating point, integer multiply, integer multiply-accumulate	IEEE-754, 64-/32-bit floating-point arithmetic and multiply	32-kbyte instruction/data two-way set associative, line locking, four pending instructions, blocking, prefetch

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
12-kbyte trace buffer	64-bit DDR, SDRAM, 200-MHz DDR, ECC protected	64 dual-entry, 4 kbyte to 64-Mbyte page size	899 FCBGA	Yes	32-bit/66-MHz PCI, two serial (synchronous or asynchronous), two 10/100/1000 MAC, PCMCIA, GPIO, HyperTransport	Yes			JTAG, fully coherent	\$89 (25,000)
12-kbyte trace buffer	Two 64-bit DDR, SDRAM, 200-MHz DDR, ECC protected	64 dual-entry, 4 kbyte to 64-Mbyte page size	860 FCBGA	Yes	32-bit/66-MHz PCI, two serial (synchronous or asynchronous), three 10/100/1000 MAC, PCMCIA, GPIO, HyperTransport	Yes			JTAG, fully coherent	\$399
Configurable	Optional	48 dual-entry jTLB, 8-entry uTLB, 4 kbyte to 16-Mbyte pages		Optional				N/A - Core	Full custom hard core, dual-issue seven-stage pipeline	License
Configurable	Optional	16, 32, or 48 dual-entry jTLB with variable page size, optional FMT		Optional				N/A - Core	Synthesizable core, coprocessor interface	License
	ROM, Flash, synchronous 100-MHz DRAM	32 double-entry fully associative TLB, 1- to 256-kbyte variable page size, full 32-bit (4-Gbyte) addressing	224 FBPGA	Real-time	Two-channel 16550 compatible, serial debugging, synchronous three-line serial clock			-40 to +85	Programmable clock management for each on-chip peripheral.	\$25
	133-MHz SDRAM	32 double-entry fully associative TLBs, 4-kbyte to 1-Gbyte page size	240 FPBGA	Real-time, watchdog	Two 16550-compatible, serial debugging, synchronous three-line serial clock, 32/66MHz PCI v2.3	Yes	Yes	-40 to +85	Clock-generator unit	\$25
	ROM, Flash, synchronous 66-MHz DRAM	32 double-entry fully associative TLB, 1- to 256-kbyte page size, full 32-bit (4-Gbyte) addressing	240 FBGA	Four 32-bit	1.5-Mbps SIO, USB host/slave	Yes	Four-channel, 10-bit ADC; one-channel, 10-bit DAC	-40 to +85	Clock-generator unit, ISA-bus subset interface	\$15 to \$20
	83/100-MHz SDRAM	48 double-entry fully associative TLB, 4-kbyte to 1-Gbyte page size	208 PQFP	Two 32-bit				-40 to +85	Dual-issue superscalar, DSP instruction, JTAG, N-Wire/N-Trace, 32-bit SysAD bus	\$20
	133-MHz SDRAM	48 double-entry fully associative TLB, 4-kbyte to 1-Gbyte page size	272 BGA	Two 32-bit for 11 events		6-bit addressing		-40 to +85	Dual-issue superscalar, DSP instruction, JTAG, N-Wire/N-Trace, 64 and 32-bit SysAD bus, clock modes from x2 to x5.5	\$35 to \$42

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	VR7701	MIPS64	400	64	32	1.5/2.5 or 3.3	4 W	Standby	MAC, 32x32 and 64x64 floating point, integer multiply, integer multiply-accumulate	IEEE-754, 64-/32-bit floating-point arithmetic and multiply	32-kbyte instruction/data two-way set associative, line locking, four pending instructions, blocking, prefetch
PMC-Sierra MIPS Processor Division www.pmc-sierra.com	RM5200	MIPS64	250, 300, 350, 400	32/64	32	1.65, 1.8/2.5, 3.3	Less than 1 W (400 MHz)	Standby	MAC/MAD/MADU, multiply (three-operand and cycle)	One/two-cycle rate single/double-precision	32-kbyte instruction/data two-way set associative
	RM7000	MIPS64	300, 350, 400, 450	32/64	32	1.3 to 1.8, /3.3, 2.5, 1.5	4 W (400 MHz)	Standby	MAD/MADU, multiply (three-operand and cycle)	Single/double-precision	16-kbyte instruction/data L2: 256-kbyte, four-way set associative, line locking, write back/through
	RM9000X2	MIPS64	800, 1000	64/8, local: 8, 16, 32, Hyper-Transport 8	32	1.2, 2.5, 3.3	5 W single core, 10 to 12 W dual core	Standby	Yes	IEEE-754	16-kbyte instruction/data L2: 256-kbyte, four-way set associative
Sun Microsystems www.sun.com/ ultrasparc	UltraSPARC IIe	UltraSPARC	400, 500	64 with ECC, external: PCI 32	32	1.5/3.3	10 W	Full, 1/2, 1/6th frequency with SDRAM self-refresh	32x32, 64x64, 128x128	IEEE 754-1985 single/double-precision, 1596.5-1992 quad-precision	16-kbyte instruction/data two-way set-associative, indexed, tagged, write-through, direct-mapped, L2: 256-kbyte
	UltraSPARC III	UltraSPARC	400, 500	64 with ECC, external: PCI 32	32	1.5/3.3	10 W	Full, 1/2, 1/6th frequency with SDRAM self-refresh	32x32, 64x64, 128x128	IEEE 754-1985 single/double-precision, 1596.5-1992 quad-precision	16-kbyte instruction/data two-way set-associative, indexed, tagged, write-through, direct-mapped, L2: 256-kbyte
	UltraSPARC IIIi	UltraSPARC	400, 500	64 with ECC, external: PCI 32	32	1.5/3.3	10 W	Full, 1/2, 1/6th frequency with SDRAM self-refresh	32x32, 64x64, 128x128	IEEE 754-1985 single/double-precision, 1596.5-1992 quad-precision	16-kbyte instruction/data two-way set-associative, indexed, tagged, write-through, direct-mapped, L2: 256-kbyte
	UltraSPARC IIIli	UltraSPARC	400, 500	64 with ECC, external: PCI 32	32	1.5/3.3	10 W	Full, 1/2, 1/6th frequency with SDRAM self-refresh	32x32, 64x64, 128x128	IEEE 754-1985 single/double-precision, 1596.5-1992 quad-precision	16-kbyte instruction/data two-way set-associative, indexed, tagged, write-through, direct-mapped, L2: 256-kbyte
SuperH www.superh.com	SH-5 CPU core soft/hard cores	SuperH 16	Soft core up to 900	32 or 64, 8 to 1024, 64 paths	16, 32	Process dependent	0.3 to 1.0 mW/MHz	Economy, sleep, quick wakeup standby, deep standby, module (peripheral) stop, clock-domain gearing	Two-, four- and eight-way SIMD packed arithmetic in 64-bit registers, permute, shuffle, extract, conversion	Single- and double-precision, IEEE-754, 3-D vector and matrix, transcendental functions	Implementation-dependent, Four-way set associative, LRU, write-back/write-through selectible, cache locking

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	133-MHz SDRAM/PC266 6 DDR 64-bit	48 double-entry fully associative TLB, 4-kbyte to 1-Gbyte page size	500 BGA	Two 32-bit for 11 events	Two UART, clocked serial interface	6-bit addressing		-40 to +85	Dual-issue superscalar, L2 cache interface	\$97
		48 dual entries map 96 pages (4-kbyte to 16-Mbyte)	128/208 QFP 128/216 ExposedPad			Optional exception vector				\$15 to \$25
		64 dual-entry TLB maps 128 pages	256/304 BGA 128/216 ExposedPad			10 external, NMI			ECC on L2 cache, on-chip EJTAG	\$60 to \$119
8-kbyte scratch RAM linear address mapping	DDR, SDRAM, 200-MHz DDR, DMA	64 dual entries, 4-kbyte to 256-Mbyte page size	656 SBGA 672 FCBGA 896 FCBGA		Two UART, 2BI, PCI, GPI, HyperTransport, three 10/100/1000 Ethernet MAC	10 external, NMI, 256 levels, intra-CPU			Can DMA packet header to L2 cache and put remainder into main memory	\$290 to \$389
	64-bit SDRAM interface, four DIMMs, up to 2 Gbytes	Dual 64-entry, 8- to 4096-kbyte page size	Socketable 370 ceramic PGA	Two 63-bit	32-bit, 66-MHz, 3.3V PCI 2.1 compatible, four GPIO	Up to 48			Energy Star power management	\$145 to \$225
	64-bit SDRAM interface, four DIMMs, up to 2 Gbytes	Dual 64-entry, 8- to 4096-kbyte page size	Socketable 370 ceramic PGA	Two 63-bit	32-bit, 66-MHz, 3.3V PCI 2.1 compatible, four GPIO	Up to 48			Energy Star power management	\$145 to \$225
	64-bit SDRAM interface, four DIMMs, up to 2 Gbytes	Dual 64-entry, 8- to 4096-kbyte page size	Socketable 370 ceramic PGA	Two 63-bit	32-bit, 66-MHz, 3.3V PCI 2.1 compatible, four GPIO	Up to 48			Energy Star power management	\$145 to \$225
	64-bit SDRAM interface, four DIMMs, up to 2 Gbytes	Dual 64-entry, 8- to 4096-kbyte page size	Socketable 370 ceramic PGA	Two 63-bit	32-bit, 66-MHz, 3.3V PCI 2.1 compatible, four GPIO	Up to 48			Energy Star power management	\$145 to \$225
Application dependent	External, application dependent	64-entry fully associative UTLB, four-entry fully associate microTLB	Application dependent	Application dependent	Application dependent	Up to 64	Application dependent	N/A - Core supports -55 to +125	SuperHyway VSI compliant interconnect, SHdebug runtime control and trace on-chip debugging with watchpoints	License

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	SH5-103 CPU hard core	SuperH 16	400 (worst case)	32 or 64, 8 to 1024, 64 paths	16, 32	1.2	Less than 400 mW	Economy, sleep, quick wakeup standby, deep standby, module (peripheral) stop, clock-domain gearing	Two-, four- and eight-way SIMD packed arithmetic in 64-bit registers, permute, shuffle, extract, conversion	Single- and double-precision, IEEE-754, 3-D vector and matrix, transcendental functions	32-kbyte instruction/data four-way set associative, LRU, write-back/write-through selectable, cache locking
Toshiba America Electronic Components www.toshiba.com	TMPR 4925XB	MIPS64	200	20 to 28/8 to 64	32	1.5/3.3	0.9 W	Halt, doze, reduced frequency	One-cycle 64x64 MAC	IEEE-754-compliant, single/double-precision	16-kbyte instruction/data four-way set associative, FIFO, lock
	TMPR 4926XB	MIPS64	200	20 to 28/8 to 32	32	1.5/3.3	0.9 W	Halt, doze, reduced frequency	One-cycle 64x64 MAC	IEEE-754-compliant, single/double-precision	16-kbyte instruction/data four-way set associative, FIFO, lock
	TMPR 4927ATB-200	MIPS64	200	20 to 28/8 to 64	32	1.5/3.3	1.2 W	Halt	One-cycle 64x64 MAC	IEEE-754-compliant, single/double-precision	32-kbyte instruction/data two-way set associative, FIFO, lock
	TMPR 4937XB	MIPS64	300	20 to 28/8 to 32	32	1.5/3.3	1.2 W	Halt	One-cycle 64x64 MAC	IEEE-754-compliant, single/double-precision	32-kbyte instruction/data two-way set associative, FIFO, lock
	TMPR 4938XB	MIPS64	300	20 to 28/8 to 32	32	1.5/3.3	1.2 W	Halt	One-cycle 64x64 MAC	IEEE-754-compliant, single/double-precision	32-kbyte instruction/data two-way set associative, FIFO, lock
	TMPR 4955AF-200 4955BF-300	MIPS64	200, 300	32	32	1.5/3.3	450 or 600 mW	Halt, doze	One-cycle 64x64 MAC	IEEE-754-compliant, single/double-precision	32-kbyte instruction/data two-way set associative, FIFO, lock
	TMPR 4955CF	MIPS64	350, 400, 450	32	32	1.2/3.3	600 mW	Halt, doze	One-cycle 64x64 MAC	IEEE-754-compliant, single/double-precision	32-kbyte instruction/data two-way set associative, FIFO, lock
	TMPR 4956CXB	MIPS64	350, 400, 450	64/32	32	1.2/3.3	700 mW	Halt, doze	One-cycle 64x64 MAC	IEEE-754-compliant, single/double-precision	32-kbyte instruction/data two-way set associative, FIFO, lock
	TMPR 7901XB	MIPS64	200	64	32	1.5/3.3	2 W	Halt	One-cycle 64x64 MAC	IEEE-754-compliant, single/double-precision	32-kbyte instruction/data two-way set associative, FIFO, lock

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Application dependent	External, application dependent	64-entry fully associative UTLB, four-entry fully associate microTLB	Application dependent	Three 32-bit, watchdog, real time with alarm and calendar functions	Full duplex serial with 16-byte send and receive FIFOs, modem control, baud rate generator	Up to 64	Application dependent	0 to +70	SuperHyway VSI compliant interconnect, SHdebug runtime control and trace on-chip debugging with watchpoints	License
	Four-channel SDRAM, NOR/NAND Flash, DMA	48-entry fully associative TLB	256 PBGA	Three 32-bit, real-time, watchdog	PCI 2.2 32-bit, 33-MHz, two serial, up to 32 PIO, SPI, ACLC, PCMCIA	Seven external, NMI			EJTAG debug	\$18
	Four-channel SDRAM, NOR/NAND Flash, ROM, DMA	48-entry fully associative TLB	256 PBGA	Three 32-bit, real-time, watchdog	PCI 2.2 32-bit, 33-MHz, two serial, up to 32 PIO, SPI, ACLC, PCMCIA	Seven external, NMI			DES/3DES, EJTAG debug	\$20
	Four-channel SDRAM, NOR Flash, ROM	48-entry fully associative TLB	420 TBGA	Three 32-bit, watchdog	PCI 2.1 32-bit, 66-MHz, two serial, up to 16 PIO, ACLC	Five external, NMI			EJTAG debug	\$25
	Four-channel SDRAM, NOR Flash, ROM, DMA	48-entry fully associative TLB	484 PBGA	Three 32-bit, watchdog	PCI 2.2 32-bit, 66-MHz, two serial, up to 16 PIO, ACLC	Five external, NMI			EJTAG debug	\$32
	Four-channel SDRAM, NAND/NOR Flash, ROM, DMA	48-entry fully associative TLB	484 PBGA	Three 32-bit, watchdog	PCI 2.2 32-bit, 66-MHz, ACLC, SPI, two EtherMAC, two serial, up to 16 PIO	Five external, NMI			EJTAG debug	\$36
		48 double-entry TLB	160 QFP			Six external			EJTAG debug	\$10 to \$15
		48 double-entry TLB	160 QFP			Six external			EJTAG debug	\$22
		48 double-entry TLB	217 FPBGA			Six external			EJTAG debug	\$25
	Four-channel SDRAM, DMA	48-entry fully associative TLB	484 PBGA	Three 24-bit, watchdog	Dual PCI 2.2 32-bit 33/66-MHz, two EtherMAC, two serial, SPI	Seven external, NMI			JTAG	\$30