

PRESERVE PC-BOARD SIGNAL INTEGRITY WITH THIS UNIQUE METHOD FOR CREATING LAYER INTERCONNECTS (VIAS) THAT CLOSELY MATCH THE SIGNAL-TRACE IMPEDANCE.

Designing controlled-impedance vias

AS DATA-COMMUNICATION SPEEDS increase beyond 3 Gbps, signal integrity becomes crucial for successful data transmission. Board designers try to eliminate every impedance mismatch along the high-speed signal path, because those discontinuities generate jitter and decrease the data eye opening—not only reducing the maximum possible distance of data transmission, but also minimizing the margin to common jitter specifications, such as SONET (synchronous optical network) or XAUI (10-Gigabit attachment-unit interface).

Due to the increasing signal density on pc boards, more signal layers are necessary, and transitions with layer interconnects (vias) become unavoidable. In the past, vias represented a significant source of signal distortion, because their impedance is usually around 25 to 35Ω. This large impedance discontinuity can reduce the data eye opening by as much as 3 dB and can create a significant amount of jitter depending on the data rate. As a result, board designers have either tried to avoid vias on the high-speed lines or implemented new techniques, such as counter boring or blind vias. Those methods help but add complexity and greatly increase board cost.

You can eliminate the significant impedance mismatch of standard vias with a new “coaxlike” via structure. This structure places ground vias around the signal via in a special configuration. Vias designed with this technique show an impedance discontinuity of less than 4% ($50 \pm 2\Omega$) on a TDR (time-domain-reflectometry) plot and improved signal quality. This new approach creates a vertical channel with a tunable impedance. Developers created the via structure using a simple coax model with the signal wire in the center; the surrounding ground shield builds a homogeneously distributed impedance. Four ground vias, which align in a ring around the signal via in the center, replace the uniform ground shield (Figure 1). Because these outer vias connect to the pc-board ground or V_{DD} (supply), they carry a charge, and a capacitance builds between each of them and the signal via. The

calculated capacitances depend on the via diameters, the dielectric constant, and the distance between the signal and ground via. The clearance (antipad) of the center via “touches” the outer vias so that the capacitance is homogeneous along the vertical channel—preventing a dramatic capacitance increase at every power and ground plane. The ground vias on the outside provide the path for the signal-return current and form an inductance loop between signal and ground vias.

You can calculate the capacitance and inductance formed by one ground via and the signal via with simple formulas (Reference 1). For the calculation, you can assume that the two vias are essentially two wires of equal diameters. D is the diameter of one via, and a is the center-to-center distance between the signal and the ground via. The inductance, L , of one via pair calculates to:

$$L = \frac{\mu}{\pi} \cdot \cosh^{-1}\left(\frac{D}{2a}\right).$$

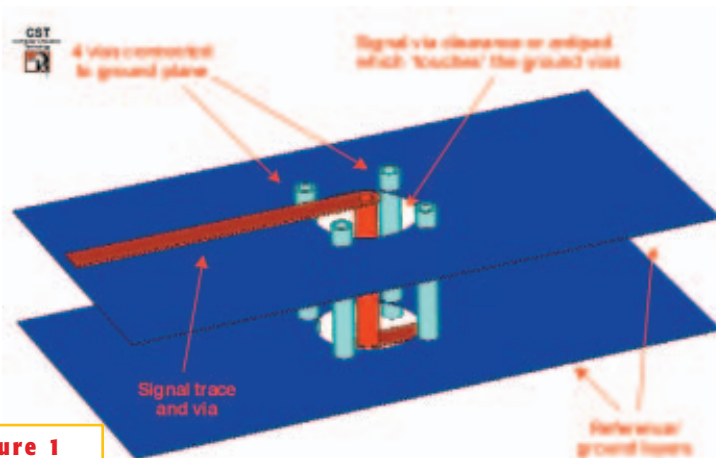


Figure 1

New techniques for pc-board-layer-interconnect design provide predictable path impedance and improved signal integrity.

The capacitance C calculates to:

$$C = \frac{\pi \cdot \epsilon}{\cosh^{-1}\left(\frac{D}{2a}\right)} \quad (1)$$

Because the vertical channel, mainly formed by the five vias, is homogeneous, the impedance Z calculates to:

$$Z = \sqrt{\frac{L}{C}}$$

Equation 1 calculates the capacitance in a standard two-wire system. The improved via structure adds three more ground vias so that the amount of positive charges in the signal via stays the same, but all the negative charges distribute evenly among the four ground vias. Therefore, the overall capacitance of the improved via structure is about the same as that of a two-wire system. However, the inductance of this via model is one-quarter of the inductance of a two-wire system, because four parallel inductance loops form between the signal and the four ground vias, resulting in via impedance Z:

$$Z = \sqrt{\frac{L}{4 \cdot C}}$$

Experimenters tested this via structure using FR4 polyclad 370, Getec, and Rogers board materials on pc boards varying from 60 mils and six layers thick to 130 mils and 16 layers thick. They verified the calculated via impedance with TDR measurements and a 3-D field solver from CST (Computer Simulation Technology). The formulas they derived predict the impedance exceptionally well ($\pm 2\Omega$), regardless of the board thickness, because the formula for the via impedance is independent of the board thickness. Table 1 compares calculated impedances for a six-layer, 62-mil FR4 test board ($\epsilon_r=4.1$) with the TDR measurement results and simulated impedance values from the Microwave Studio 3-D field solver from CST. The calculated via impedances are within 2Ω of the measured results.

A TDR plot is a good method for determining the impedance of vias or other discontinuities on a signal channel. Figure 2 shows the TDR plot measured on two almost-identical channels of the test board. The only difference is that one channel has a regular via with a diame-

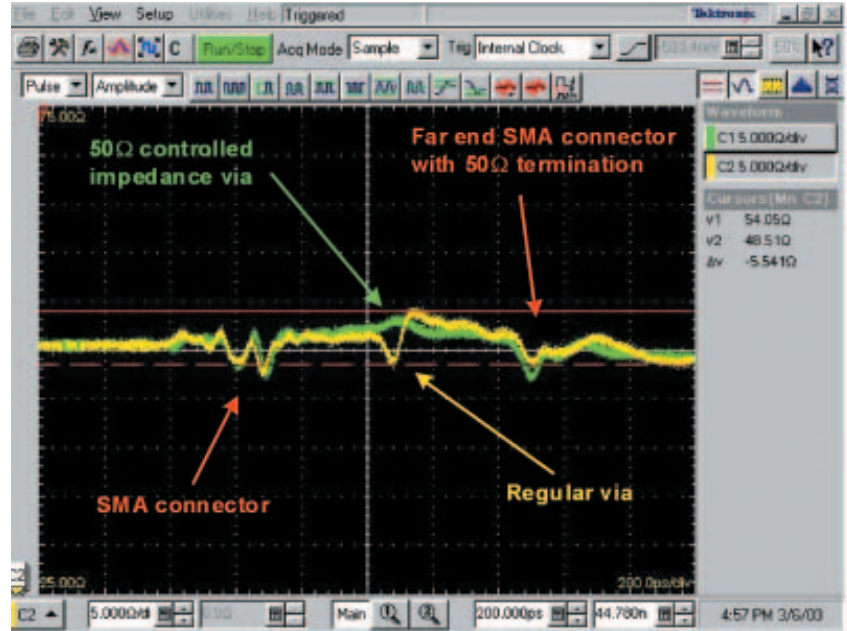
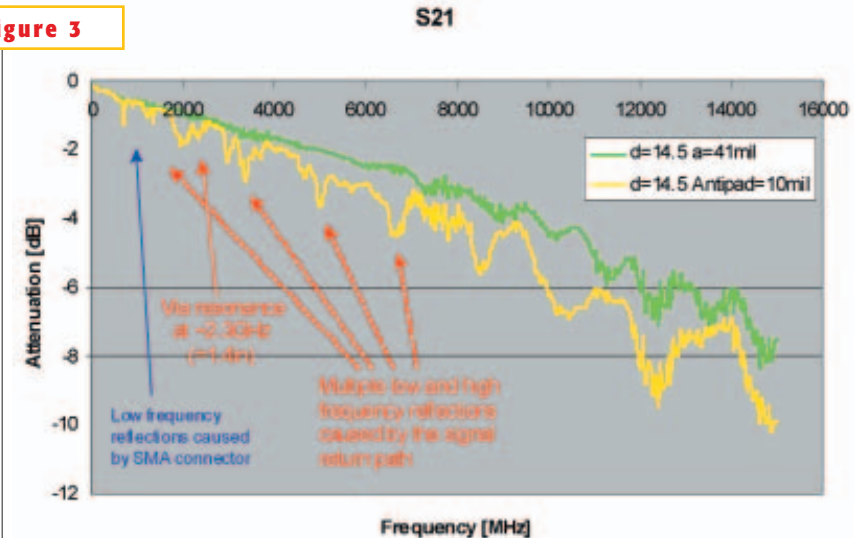


Figure 2

The yellow trace shows a TDR plot of a channel with a regular via. The green trace shows the TDR plot for a channel with a controlled-impedance via.

ter of 14.5 mils and an antipad (clearance) of 10 mils, and the other channel has the improved via structure with via diameters of 14.5 mils and center-to-center distances of 41 mils. The TDR plot shows that the impedance mismatch of the SMA connector is the same in both cases. The controlled-impedance via has an impedance of about 52Ω , and the impedance of the regular via is 48 to 54Ω . The impedance match of the regular via is worse than that of the via structure.

Figure 3



This S21 plot shows the controlled-impedance-via channel in green and the regular-via channel in yellow.

However, for a regular via, the match is good, and, according to this plot, you should expect little signal distortion.

One disadvantage of the TDR measurement is that the results are relative to the rise time of the equipment. It does not show the frequency response of the discontinuity for discrete frequencies. A better way to demonstrate and compare the impedance mismatch of the vias is to look at the S21 scatter parameter on a network analyzer (Figure 3). A plot of the

S21 shows how specific frequencies of the signal pass through the transmission-line channel and how others get reflected or attenuated.

Figure 3 shows the S21 plot of the two channels in the TDR measurement. They are identical, except that one channel has the via structure (green curve), and the other channel has a regular via (yellow curve). The via structure shows an exceptional frequency response, and the first resonances are visible at about 10 GHz. The regular via, on the other hand,

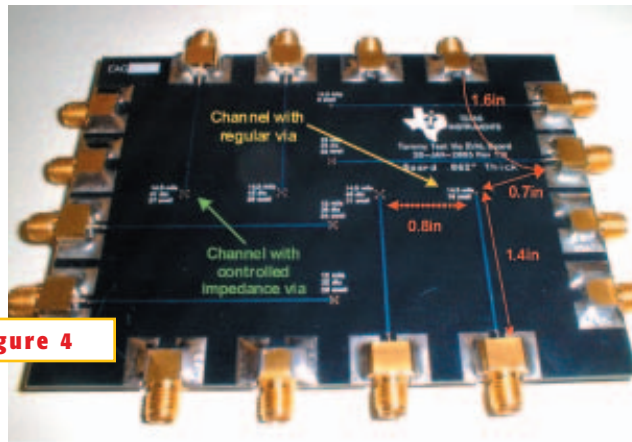


Figure 4

Experimenters developed a test board with both standard and improved impedance vias to measure signal performance.

shows multiple reflections over the entire frequency band, even though the impedance mismatch is small. These reflections cause certain frequencies of a signal to be more attenuated than others, thus further degrading the high-speed signal.

On this test board (**Figure 4**), the distance between the SMA connectors and the via is about 1.4 in., which equates to a frequency of about 2.35 GHz (using **Equation 2**) that is clearly visible in the S21 plot. Although the frequency response of discontinuities for an asymmetrical channel may differ slightly, the channels are designed to be symmetric. The signal-return-current path mainly causes the other reflections on the yellow, regular-via curve.

Because the regular via provides no path for the signal-return current, the current takes the least inductive path closest to the regular via. The signal-return current flows through the ground vias of the SMA connector and through the ground-via structure of the adjacent channel. Because the return current takes the closest path, resonance frequencies in the S21 plot are, as you would expect, at about 5 GHz (0.7 in.) and not at 4.2 GHz (0.8 in.). Furthermore, the return current flows from the ground vias of that SMA to the far-end SMA connector (an approximately 1.6-in.-long current path), causing another resonance at about 2 GHz (**equations 3 and 4**). You can clearly observe both phenomena, which the return current causes, in the S21 plot.

The following equations calculate the resonance frequencies of the channel with the regular via:

$$f_{\text{VIA}} = \frac{1}{2 \cdot \text{DISTANCE} \cdot \text{PROPAGATION DELAY}} = \frac{1}{2 \cdot 1.4 \text{ IN.} \cdot 150 \frac{\text{pSEC}}{\text{IN.}}} = 2.35 \text{ GHz.} \quad (2)$$

$$f_{\text{VIA-SMA}} = \frac{1}{2 \cdot 0.7 \text{ IN.} \cdot 150 \frac{\text{pSEC}}{\text{IN.}}} = 4.8 \text{ GHz.} \quad (3)$$

$$f_{\text{RETURNPATH(SMA-SMA)}} = \frac{1}{2 \cdot 1.6 \text{ IN.} \cdot 150 \frac{\text{pSEC}}{\text{IN.}}} = 2 \text{ GHz.} \quad (4)$$

The first conclusion you can draw from the S21 measurement is that the resonance frequency depends greatly on the location of the discontinuity on the transmission line. This statement does not imply that you should place the via close to the transmitter or connector so that the impedance mismatch appears at frequencies greater than 10 GHz. Unfortunately, in practice, this approach would work only if there were a perfect impedance match at the receiver. Otherwise, a

reflection would appear at the receiver, and another reflection would appear at the via closest to the transmitter. These reflections result in a lengthy distance from receiver to via to receiver, which again translates to a low resonance frequency.

The second S21 measurement conclusion is that the signal-return current contributes a considerable amount of reflection. The S21 measurement in **Figure 3** shows two almost-identical channels that differ only in their signal-return path and a slightly different impedance mismatch. The S21 plot shows more reflections at the absence of this close return path for the regular via because the signal-return current takes the closest, least inductive path available, even if it is an inch away, thereby causing resonances.

The signal-return current could flow through the inner-plane capacitance of adjacent power and ground planes, but that capacitance is usually so small that only high frequencies can pass. In most cases, the signal-return current flows through the closest via that connects the reference layers of the signal trace. Those return-current vias can be far from the actual signal via (**Figure 5**). To demonstrate this effect, experimenters placed a ground via approximately 100 mils from the regular via and plotted the current density in a controlled-impedance via (**Figure 5a**) with the current density for the structure (**Figure 5b**). It is clear that most of the return current flows through the added ground via some distance away. This extra distance for the return current

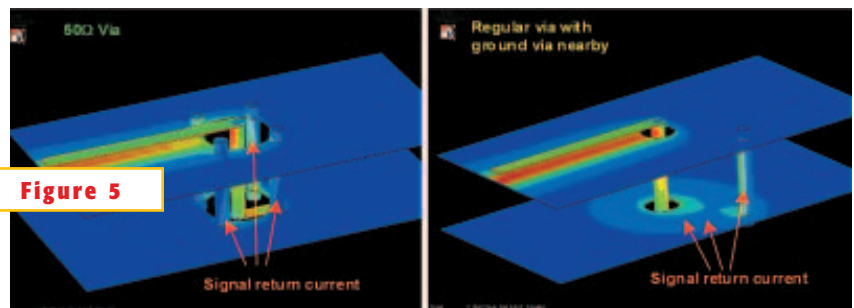


Figure 5

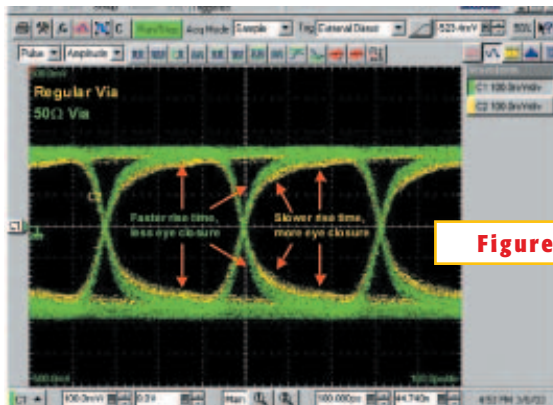
(a) (b)
A plot comparing the current densities for the controlled-impedance via (a) and the regular via (b) shows that the return current flows through the added ground via some distance away.

causes reflections that appear in the S21 plot.

The impact of broadband reflections becomes more visible when you examine a real data signal with a wide frequency spectrum, such as a PRBS (pseudorandom-bit-stream) pattern. To illustrate this impact, experimenters sent a 2^7-1 PRBS pattern at 3.125 Gbps through both channels and recorded the output waveforms (Figure 6). The channels are only 2.8 in. long, but the impact of the vias is clearly visible. The regular via (yellow curve) attenuates multiple frequencies, resulting in a smaller data eye and a slower rise time than a controlled-impedance via (green curve).

Finally, the impedance mismatch should be as small as possible. Even the smallest mismatch shows up at one discrete frequency on the S21 plot and impact the signal quality. You can maximize the performance of controlled-impedance vias by following important design parameters, such as spacing, trace widths, and pad widths. For example, the antipad, or clearance size, of the signal via is critical. It must be at least the difference of distance between signal and ground via, a , and the via diameter, D , so that the signal-via antipad touches the ground via. Otherwise, the metal on the ground, power layer, or both comes too close to the signal via and creates additional unwanted capacitance thereby reducing the via impedance to less than the calculated 50Ω .

Likewise, every via that connects a microstrip line on the top or the bottom layer with a stripline on an inner layer creates a stub. When the stub length is smaller than the signal rise time, the stub is barely noticeable. If the stub length is longer, it can cause considerable signal distortion. For example, a stub of 40 mils has a run length of about 14 psec in a system with a 3.125-Gbps signal with a rise time of approximately 50 psec. In the worst case, the stub length is a quarter-wavelength of an



A data-eye plot of a bit stream shows that the regular via (yellow curve) attenuates multiple frequencies, resulting in a smaller data eye and a slower rise time than does a controlled-impedance via (green curve).

important frequency, and the stub becomes a short circuit for that frequency, canceling out the original signal.

The above equations assume that the diameter is the same for the signal and the ground vias. To use different diameters, you need to modify the formula for the capacitance. Designers should choose the via diameters according to the width of the connected traces. If the trace is much smaller than the via, the transition from the 50Ω trace to the via pad causes an unwanted discontinuity. Designers should also consider the distance between the ground vias and the connected trace. It can become an issue when the separation between the ground via and the trace is smaller than the distance between the trace and the reference layer, creating additional capacitance for the trace and again dropping the trace impedance to less than 50Ω . On the test board, for example, the distance between the signal trace and the ground vias is about 11 mils, and the trace is about 10 mils above the ground-reference layer.

Another important design consideration is pad size, because every via that connects to a trace requires a pad. This pad should be as small as possible, because the distance from the pad to the ground vias is smaller than the distance from the signal via to the ground vias. A shorter dis-

tance results, due to the pads, and increases the capacitance, which reduces the overall impedance.

In a typical design, four ground vias are not always available. The via structure works equally well with power vias as long as the return current has a path from V_{DD} to ground through a nearby bypass capacitor.

For example, consider boards that contain this via structure inside a BGA pinout with a 1-mm grid. Because of the fixed pinout, you may connect only two outer vias to ground; you connect the other two vias to V_{DD} . The via structure works well because you can also place SMD bypass capacitors between V_{DD} and ground inside the BGA.

You can also use the via structure for differential signals. The signals can share the two outer vias, saving board space. Texas Instruments uses this method on the evaluation boards for its XAUI transceivers, which offer limited space inside the BGA. For controlled-impedance vias, the size of the layer separation does not matter, because the ground vias and not the metal layers form the capacitance. Regular vias, however, depend on the capacitance from the layers. Therefore, you must design them specifically for different layer stackups even if the board thickness does not change. □

REFERENCE

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TABLE 1—COMPARISON OF CALCULATED, SIMULATED, AND MEASURED VIA IMPEDANCE

Diameter (mils)	14.5			12		
Distance from signal-via center to ground-via center (mils)	41	43	45	32	34	36
Calculated impedance (Ω)	50.3	51.8	53.3	48.5	50.4	52.2
Simulated impedance (Ω)	51.2	52	52.1	51.5	51.6	51.6
Measured impedance (Ω)	52	54	55	50	51	53