

CAREFUL ATTENTION TO PC-BOARD DESIGN INCREASES

THE FLEXIBILITY OF BOUNDARY-SCAN TESTING.

Boundary-scan tips pay board-test dividends

AS A DIGITAL DESIGNER, you probably recognize the benefits of using boundary-scan circuits that comply with the IEEE 1149.1 standard. But you can run into difficulty when your circuits involve using devices that do not comply with the boundary-scan standard. And, even if you pay careful attention to the IEEE 1149.1 standard, subtle problems can delay debugging and testing steps. The design tips that follow will help you overcome some of these problems and make the pc boards that you produce easier to test and debug. You can apply these tips right away or save them for future use.

STANDARDIZE CONNECTIONS

If at all possible, specify a standard type of connector for the boundary-scan connections to each pc board you design. A standard arrangement of the boundary-scan signals will let you apply the same hardware tools to all the pc boards you design. At a minimum, use a 10-pin connector that provides the five boundary-scan signals and five grounds (Figure 1). You can use a larger connector to accommodate additional signals provided by proprietary boundary-scan tools.

Even if you provide a standard connector for boundary-scan signals, consider connecting the boundary-scan signals to an edge connector or another connector, which a pc board will use to communicate with other elements in a system. Access to the boundary-scan signals at an edge connector can eliminate the need for separate connections, such as bed-of-nail probes during production testing. Edge-connector access also may facilitate testing when your board connects to a backplane.

ENSURE SIGNAL INTEGRITY

Always ensure a pc-board layout connects the TCK (test-clock), TMS (test-mode-select), and TRST* (test-reset) signals in parallel to all the boundary-scan devices in a chain. As with any clock signals, keep the TCK and TMS signal runs as short as possible. You should declare these two signals "critical" within the autorouter used for pc-board design. (Not all designs require the TRST* signal.)

If your design will include vector-intensive operations, such as testing SDRAMs or programming flash memories that require TCK frequencies in excess of 10 MHz, you should use high-speed terminations (Figure 2). The TCK clock-termination circuit should match the impedance of the TAO (test-access-port) cable that connects a pc board to a boundary-scan tester. The 22Ω resistor on the TDO (test-data-output) line helps damp reflections that might occur on this line when you use a high-frequency TCK input.

You can reduce signal fan-out problems by buffering the IEEE 1149.1 inputs before you distribute

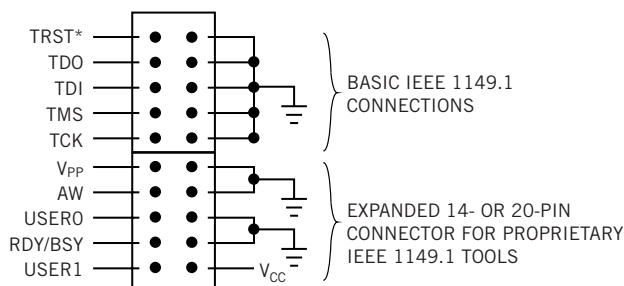


Figure 1 A standard connector for boundary-scan signals makes it easy to use the same testing and debugging tools with different pc-board designs.

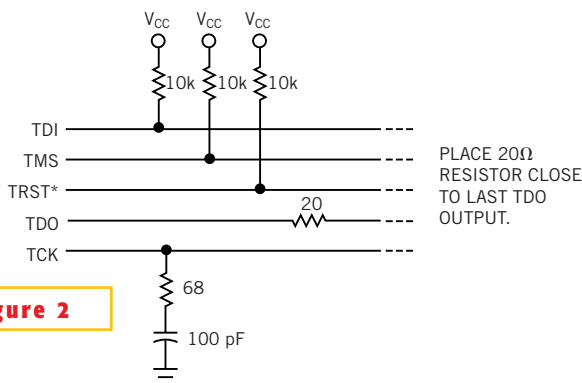


Figure 2 Termination circuits on boundary-scan lines help ensure proper signal levels and timing for devices in a scan chain.

their signals on a pc board. The circuit in **Figure 3** shows the use of a 74ABT244 noninverting octal buffer in which the TMS and TCK inputs each drive four internal buffers. Pay special attention to the fan-out of the TMS and TCK signals, which must connect to each boundary-scan IC in a chain. In general, plan on a fan-out of four to six from a 74ABT244 buffer for nearby connections, and a fan-out of only one to two for devices that require more than a 10-cm trace to route the TMS or TCK signal to them. If your design includes the TRST* signal, buffer it, as well.

ADD A BYPASS

During prototyping, you may need to bypass the boundary-scan chain in an IC. In such a case, provide resistor pads on the pc board for a bypass loop around the IC, and also provide pads for resistors on the TDI (test-data-input) and TDO connections to the IC you plan to isolate (**Figure 4**). For normal operation, you would place 0Ω resistors at the TDI and TDO inputs and would not place a 0Ω resistor at the bypass position. To bypass the IC, simply specify DNP (do not place) for the TDI and TDO resistors, but do place the 0Ω bypass resistor. Opening the TDI signal path to the IC prevents the chip from accepting any boundary-scan instructions passed down the chain. You need no pullup resistor on the unconnected TDI line, because an internal pullup will produce a “string” of logic ones at TDI, equivalent to the Bypass instruction.

When you need to bypass multiple

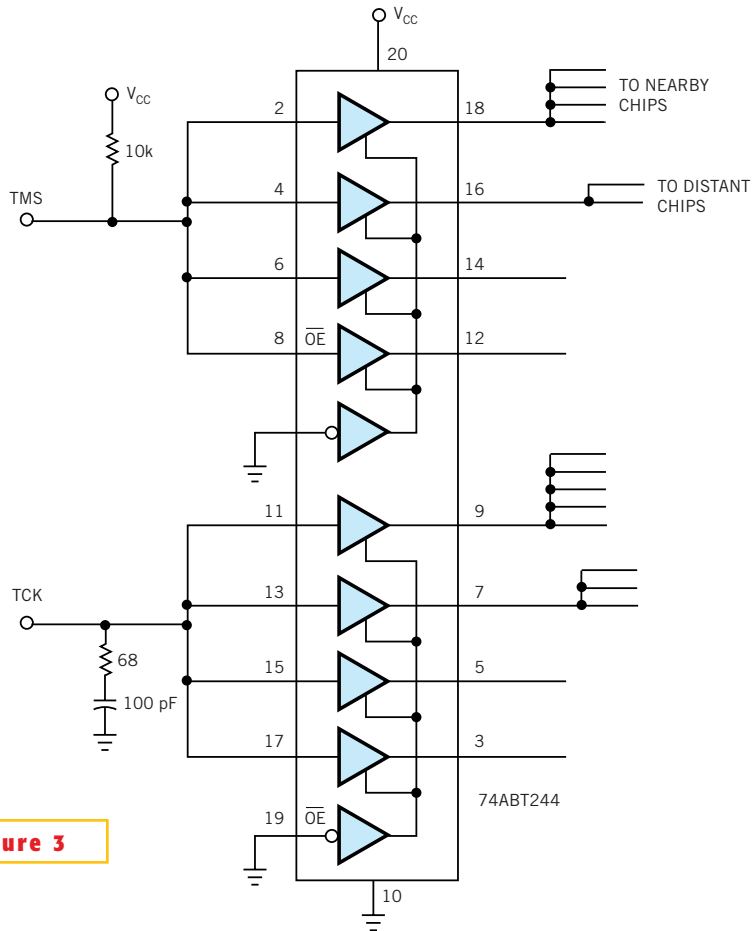


Figure 3

A 74ABT244 octal buffer can increase the fan-out of the TMS and TCK boundary-scan signals. Note that each input drives four buffers in parallel.

consecutive devices in a chain, provide a bypass loop around the group of devices as well as resistor pads between the devices’ TDO and TDI pins. By placing or removing 0Ω resistors on the proper

pads, you can bypass all devices as well as isolate individual devices.

During testing and debugging, you may need to control the onboard clock signals routed to memories, processors,

IEEE 1149.1 BACKGROUND

In 1985, a group of electronics manufacturers formed the JTAG (Joint Test Action Group) to tackle the problem of increasingly complex tests required by the latest electronic products. The group’s efforts led to the IEEE 1149.1 standard that specifies a protocol for shifting test information into components, pc boards, and entire systems. Test results come out of these devices on a separate serial line. By adopting the standard in everything from individual ICs to complete systems, manufactur-

ers have reduced not only the time needed to test complex systems, but also the time needed to develop the tests.

At its most basic, the test protocol—generally called boundary scan—provided a “register” for each I/O pin on a device. This register lets the pin operate with bits shifted in during testing. In a typical circuit, boundary-scan tests stimulate outputs and record the state at the devices connected to them. By matching the test patterns, also called vectors, applied to devices with

the patterns shifted out, test engineers can locate faults in a circuit and locate defective components.

In many cases, boundary-scan testing provides the simplest, fastest, and least expensive way to test connections between components. And designers can reuse many of the patterns they develop for testing, further improving the economics of test. The addition of boundary-scan capabilities to a pc board requires only a small amount of extra space for boundary-scan

pins on compliant devices and for connections to test and debug tools.

Additional boundary-scan benefits include:

- highly automated development of tests and diagnosis of faults;
- no limit to the number of boundary-scan test points,
- high production-line throughput for testing and in-system programming, and
- low-cost tools and capital investment.

and other devices. Unfortunately, many designers simply connect an onboard oscillator's OE (output-enable) signal directly to V_{CC} , which makes it impossible to disable the oscillator during testing. If you have two unused I/O pins on an FPGA, a CPLD, or a similar device, you can disable the onboard oscillator and supply your own clock signal (Figure 5). In this circuit, one line from the FPGA can turn off the oscillator and force its output into a high-impedance state. The other line supplies a clock signal. The FPGA must supply two spare boundary-scan cells, one for each connection. By using the Extest (external-test) boundary-scan instruction, you can disable the oscillator and generate your own clock signal from the FPGA.

If you plan to provide an external clock signal to a clock-distribution IC, make sure your boundary-scan output can provide the minimum clock frequency the IC requires. In some cases, distributed clocks may connect 20 to 30% of the clocked devices on a boundary-scan pc board, so account for all clocked devices when you determine the minimum required frequency for proper testing and debugging.

MIX 'EM UP

Your circuits may mix nonboundary-scan and boundary-scan devices that share common output signals. In this situation, provide the means to disable the shared outputs from the nonboundary-scan devices. In the circuit shown in Figure 6, an FPGA and a nonboundary-scan device connect to the same address and data lines. Disabling the outputs from the nonboundary-scan device prevents pos-

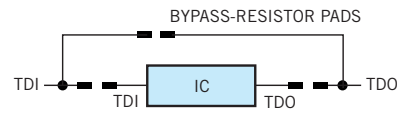


Figure 4 Resistor pads at the input and output of a boundary-scan device, combined with a bypass loop, let you isolate and bypass problem devices when debugging a new circuit.

sible signal contentions that could lead to erroneous test results. In this example, the FPGA provides an otherwise-unused output that it asserts only during testing. This signal disables the data- and address-bus signals from the nonboundary-scan device. You must ensure that the output-enable signal from the FPGA to the nonboundary-scan device does not connect to any internal FPGA circuits that would alter its state during normal circuit operation.

FORCE THE ISSUE

Some FPGAs from Altera and Xilinx require special connections to enable their boundary-scan circuits at power-up. In normal operation, these devices enter a configuration mode upon application of power. While operating in that mode, though, they cannot respond to boundary-scan signals.

To force a Xilinx XC4K or Spartan device into boundary-scan mode requires a ground connection to its Init input and a V_{CC} connection to its Prog input (Figure 7). Placing jumpers on a pc board to make these connections during testing forces devices in these families to respond properly to boundary-scan commands upon power-up. Use jumpers to

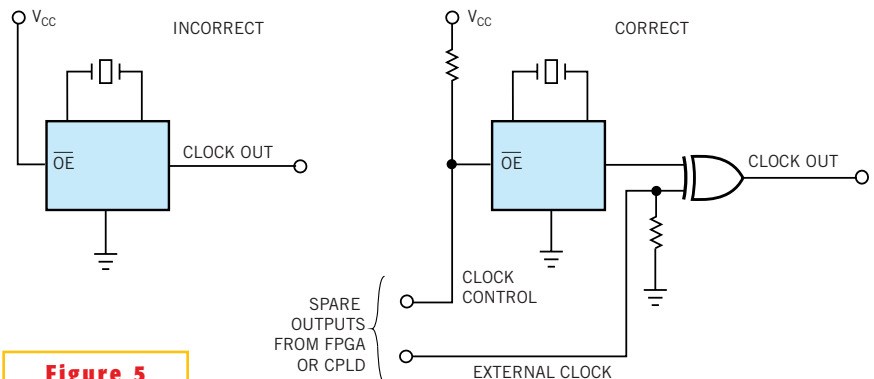


Figure 5

Two unused outputs on a CPLD or FPGA let you control an onboard clock as well as supply your own clock signal for testing.

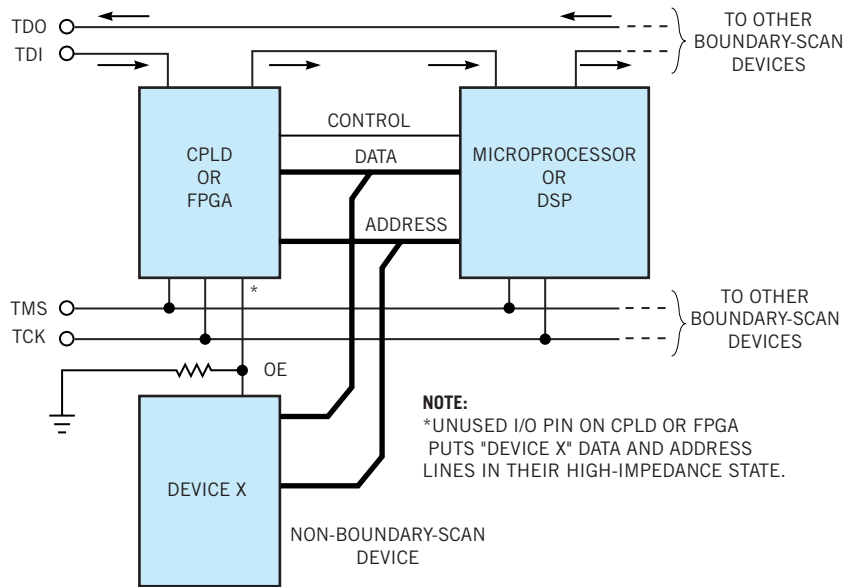


Figure 6 When you plan to mix device types on a pc board, ensure that one of your boundary-scan devices can “disconnect” the nonscan devices from connections they share with scanned ICs.

connect the devices to the Prog and Init signals for normal operations.

Altera Flex and Apex devices also may require special control at power-up to place them in a mode that responds to boundary-scan signals. A jumper that grounds the nconfig input on these devices ensures they can respond to boundary-scan signals on power-up. The Flex 6000 devices default to a disabled boundary-scan function during bit-stream generation, unless you enable the boundary-scan feature from within the Altera MaxPlus2 tool suite. But, even if you en-

able this mode, the chip does not execute boundary-scan tests as it configures itself. Grounding the chip’s nconfig input ensures that the chip will hold off configuration and allow for boundary-scan operations.

As an alternative, you can wait to run boundary-scan tests until the chips configure themselves. But this approach can cost time and energy. You should obtain a BSDL (boundary-scan-description-language) file that describes the post configuration status of the chip’s pins. Unfortunately, few design tools automati-

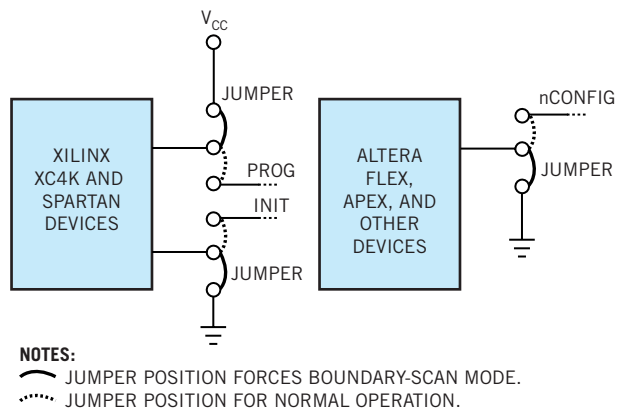


Figure 7 Jumpers can force Xilinx SRAM-based FPGAs to enter the boundary-scan mode of operation on power-up. A jumper at the nconfig input of an Altera SRAM-based device forces the device to configure itself as a boundary-scan device at power-up.

cally generate postconfiguration BSDL files, so you must manually edit the pre-configuration BSDL file to reflect the post-configuration state you want for these devices. Manual editing can introduce errors.

Keep in mind that a chip may redefine some of its I/O pins during configuration. The BSDL description of a preconfigured FPGA defines all I/O pins as bidirectional, but your design can redefine pins as only input or only output, in which case a pin can either sense or drive a signal but can't do both. If you use the architectural information the preconfigured BSDL file provides to generate the interconnect test with any ATPG (automatic-test-pattern-generation) tool, it tries to sense and drive each pin, which may be impossible in the postconfiguration state. As a result, you're better off forcing the FPGA into its preconfiguration state on power-up, rather than developing test vectors for the postconfiguration state.

Remember that you need to enforce the preconfiguration state during manufacturing test. But, to test a configured FPGA in system or field applications, you must develop tests for the postconfiguration state.

DIVIDE AND CONQUER

In some cases, you may need to partition a pc-board design into several boundary-scan chains rather than provide a single long chain. Here are a few of the circumstances that might demand separate chains:

- A third-party debugging or emulation tool may expect devices in a chain to have a different register length than other boundary-scan ICs used in a design. Don't try to mix register lengths; instead, set up a separate chain.

- FPGAs and CPLDs that require special in-circuit programming tools may require separate tools. Chips that comply with the IEEE 1532 standard for in-circuit configuration work in a normal boundary-scan chain, however.

- If you plan to mix logic families, say ECL and TTL, or voltages within families—1.8, 2.5, or 3.3V—segment logic families and voltages into their own boundary-scan chains.

- You may need to separate vector-intensive devices, such as flash memories

and SRAMs, into separate chains to minimize test and programming times.

- If you're designing system components, you may want to segregate those devices that provide access to backplanes and board-to-board connections in their own chains. Doing so can reduce test times and let you confine tests to similar types of connections.

Boundary-scan techniques can provide powerful testing and debugging tools, but you must carefully assess your system needs and think through what you want testing to do. These tips can help you think more about the types of changes you can make to a pc-board design to maximize the use of boundary-scan elements. □

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