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EDN

# DSP Directory 2001

**DSPs ARE HOT.** According to market analysis from Forward Concepts (www.fwdconcepts.com), DSPs in 2000 became the largest processor-market segment, passing the traditionally strong 8-bit-microcontroller market. Compared with 1999 statistics, DSP worldwide shipments in dollars were up 40%, outpacing the overall processor market, which was up a healthy 31%. Reflecting the growth in DSP shipments, this year's DSP directory includes more devices than ever before.

In addition to the traditional general-purpose and reconfigurable DSPs, our directory identifies application-specific devices. This category is duly warranted: More than half of the devices fall into it. The directory lists only programmable devices, so it does not include devices with integrated DSP cores that restrict users to just setting some operating parameters.

You can sum up the overwhelming trend for this year's devices in two words: "networks" and "communications." Networks have become the enabling vehicles by which vendors are developing and delivering so many new (or repackaged) applications, most notably wired and wireless infrastructure devices, as well as video-over-network and voice-over-network devices, such as voice over IP, voice over DSL, and voice over ATM. Without DSP devices, streaming multimedia over the Internet would be severely limited.

Over the years, multiple MAC (multiply-accumulate) units have become more common. Further upping the performance ante, vendors have designed a number of devices to support multiple parallel DSP cores and computational units. These devices especially suit the inherent parallelism in the high volume of data that central-office voice- and data-processing as well as image-processing applications manage. These types of applications may provide the parallel-data width necessary to take advantage of the nearly 1 billion-MAC/sec usable performance on some of these devices.

As Moore's law continues to march forward, it has become practical to include on-chip accelerators, such as Viterbi decoders for forward error correction, not just on application-specific devices, but also on some general-purpose devices. In spite of the increase in processing performance, low power consumption remains a significant concern, especially for those devices serving the wireless- and portable-application market.

DSPs have become integral to many high-volume designs in which time to market is critical. As a result, DSP vendors are partnering with third-party vendors; investing in development suites that include not only a full tool chain of assemblers, compilers, debuggers, emulators, and profilers, but also libraries of application-software modules. These partnerships are crucial to the DSP market, because they provide software that's difficult to write and make these chips feasible to use. All of the performance and functions on these devices means little if you can't complete the coding for them in less than a year.

EEMBC, the *EDN* Embedded Microprocessor Benchmark Consortium, has a variety of benchmarks that target the applications that the DSPs described in this directory perform. Benchmark scores are available at www.eembc.org.

## ADSP-218x and ADSP-219x
## Analog Devices Inc, www.analog.com

The ADSP-21xx family executes all instructions in one cycle. Each family member extends the code compatibility of the ADSP21xx family. The processors feature an algebraic programming syntax and can execute multiple operations per cycle. Family members have X and Y DAGs (data-address generators) and separate program and data buses.

Analog Devices opted for a 16-bit-wide data word and a 24-bit-wide instruction word. The wider instruction word lets the device use more complex instructions and offers more flexibility than 16-bit operation code. The ADSP-21xx family integrates as much as 2 Mbits of SRAM around the DSP core to increase data-transfer efficiency. It also integrates DMA ports that connect to external hosts or external memory. These bidirectional, byte-wide ports can directly access as much as 4 Mbytes of external memory for off-chip storage of program overlays and or data tables. The ADSP-219x DSP supports as many as 16M words of addressable memory space with 24 bits of addressing width. It also provides two 40-bit accumulators and a 40-bit shifter, which help with overflow.

- Architecture is code- and pin-compatible.
- Devices feature low power consumption and cost less than $5 in high volume.
- High memory integration increases data-transfer efficiency.

**Addressing modes:** The ADSP-21xx family supports immediate, register-direct, memory-direct, and register-indirect addressing modes. The ADSP-219x adds register, indirect-post-modify, immediate-modify, and direct- and indirect-offset addressing modes. Each address generator supports as many as four circular buffers, each with three registers. The ADSP-219x supports as many as 16 circular buffers using a DAG shadow register and a set of base registers for additional circular-buffering flexibility.

**Special instructions:** The ADSP-21xx can conditionally execute most instructions. A "do-until" command establishes a sequence of instructions that can be arbitrary in length and nested four deep for repeat operations. The ADSP-219x allows as many as eight nesting levels. In addition to the standard arithmetic and logic instructions, the ALU (arithmetic-logic unit) supports division primitives. Because the ADSP-21xx is nonpipelined, it incurs no penalties for jumps and calls.

**Support:** Software- and hardware-development tools include the VisualDSP and VisualDSP++ IDE, an evaluation kit, and a serial-port emulator, for development, debugging, and deployment. The EZ-Kit Lite contains an evaluation board and software that provides developers a cost-effective method for initial evaluation of the ADSP-218x DSP family architecture. The ADSP-218x EZ-ICE (in-circuit emulator) provides an easier and more cost-effective method for engineers to develop and optimize DSP systems, shortening product-development cycles for faster time to market. VisualDSP++ integrates an RTOS kernel, a C++ compiler, and a debugger into an easy-to-use environment.

## OakDSPCore
## DSP Group, www.dspg.com OakDSPCore

This 16-bit, fixed-point, licensable DSP core features single-MAC (multiply-accumulate) architecture. Its instruction set includes DSP and microcontroller instructions, and the processor features high code density and low power consumption.

- The OakDSPCore handles bit-manipulation, control, and DSP instructions.
- Devices feature high code density and low power consumption.

The OakDSPCore has two data buses and one program bus, configurable memory (ROM/RAM) size, a DAAU (data-address-arithmetic unit), a multiplier, a 36-bit ALU (arithmetic-logic unit), two sets of two 36-bit accumulators, and support for a C compiler. It also includes a bit-manipulation unit with a 36-bit barrel shifter, an exponent-evaluation unit that supports fast normalization, and a bit-field-operation unit. The zero-overhead-loop mechanisms include an interruptible single-word instruction loop and four-level nesting of block repeats.

User-definable registers speed hardware acceleration and provide coprocessor support. It has four pipeline stages, single-cycle interrupt latency, and automatic context switching. Power management includes active, slow, and idle operation modes. OakDSPCore is compatible with the PineDSPCore.

**Addressing modes:** The OakDSPCore supports register, single- and double-indirect, short- and long-immediate, short- and long-index, and stack-pointer addressing modes. It also supports circular (modulo) buffering for all its pointers and direct addressing for the entire 64k-word data space. In addition, it has a program-memory-indirect addressing mode.

**Special instructions:** Instructions for the OakDSPCore include single-cycle minimum/maximum calculation with pointer latching, double-precision calculations, normalization, exponent, conditional accumulator modifications, division step, read-modify (add/subtract/OR/AND/XOR)-write, test 16-bit mask bits and test bit, delayed return, interruptible single-word repeat loop and block repeat, 36-bit shift left or right in a single cycle, and a bank exchange of alternative registers.

**Support:** DSP Group has a set of advanced GUI-based development tools, including an optimizing C/C++ compiler, an assembler, a linker, common-object-file-format converters, a debugger with an emulation interface and extendable simulator for system-on-chip simulation, a profiler, and the Evaluation Development Platform. DSP Group has an infrastructure of third-party vendors, offering software, tools, and design services.

## PineDSPCore
## DSP Group, www.dspg.com

PineDSPCore is the first generation of the SmartCores family, introduced in 1991. PineDSPCore is a 16-bit, fixed-point, licensable DSP core, with a single-MAC (multiply-accumulate) architecture. It has a compact DSP and control instruction set with a high code density, low power consumption, and a small die. PineDSPCore has two data buses and one program bus, a configurable memory (ROM/RAM) size, and a DAAU (data-arithmetic-addressing unit). The computation unit includes a multiplier, a 32-bit product register, a 36-bit ALU (arithmetic-logic unit), two 36-bit accumulators (with 4 guard bits), and a normalization mechanism. The ALU performs arithmetic and logic operations on the data operands and functions, such as step division and rounding.

- DSP and control instruction set is compact.
- Device perfectly fits low-end high-volume applications.
- DSPCore is licensable.

PineDSPCore also includes two zero-overhead loop mechanisms: a single-word instruction loop and a block repeat. It has user-definable registers for hardware acceleration, coprocessor support, or both. It has three pipeline stages and single-cycle interrupt latency. Power management includes active, slow, and idle operation modes.

**Addressing modes:** PineDSPCore supports register, single- and double-indirect, and short- and long-immediate addressing modes. It supports circular (modulo) buffering for all its pointers and direct addressing for the entire 64k-word data space. In addition, it has a program-memory indirect addressing mode.

**Special instructions:** Instructions include conditional accumulator modifications, conditional and unconditional call and branch, arithmetic and logical operations, round, rotate, shift, compare, division step, MAC, square, single-word repeat loop, and block repeat.

**Support:** DSP Group provides a full set of advanced graphical-user-interface-based development tools, including an optimizing C/C++ compiler, an assembler, a linker, common-object-file-format converters, a debugger with an emulation interface and an extendable simulator (ASSYST) for system-on-chip simulation, a profiler, and the Evaluation Development Platform. DSP Group has a large infrastructure of third-party vendors offering software, tools, and design services.

## Teak
## DSP Group, www.dspg.com

Teak is a low-power, 16-bit, fixed-point DSP soft core with a dual-MAC (multiply-accumulate) architecture and ILP (instruction-level parallelism). Teak is a process- and library-independent, fully synthesizable soft core, and its design meets the needs of the ASIC design environment.

- Compact code has 16-bit instruction width.
- FFT butterflying completes in five cycles, and Viterbi decoding completes in three cycles.
- Devices feature a dual-MAC architecture and a soft DSP core.

Teak has configurable memory size, a data-address-arithmetic unit, two multipliers, a 40-bit three-input split ALU (arithmetic-logic unit), four 40-bit accumulators, an exponent unit, and a bit-manipulation unit. It has built-in accelerators for complex FFT; a Viterbi decoder; wide automatic context switching; and support for a C-compiler, an RTOS, and bit-exact standards, such as Global System for Mobile communications. It has zero-overhead loop mechanisms with infinite levels of repeat and block repeat.

Teak has compact code with an instruction width of only 16 bits, including parallel instructions. Teak's program memory can be as large as 4M words.

With user-definable registers for hardware acceleration, coprocessor support, or both, and mechanisms for power-consumption reduction, Teak is code-compatible with the OakDSPCore and TeakLite instruction sets of the SmartCores family.

**Addressing modes:** Teak supports circular (modulo) buffering, register, short- and long-direct, short- and long-immediate, relative, bit-reversal, and short- and long-index-based addressing modes. It can also perform quadruple-indirect addressing (for example, to simultaneously feed four inputs of the two multipliers or four inputs of the split ALU).

**Special instructions:** Instructions include dual-MAC performance, read/write double words to and from memory, and single-cycle minimum/maximum search with pointer latching. The device handles complex FFT butterflying in five cycles and Viterbi decoding in three cycles. Devices also perform bit-manipulation and microcontroller instructions, double-precision multiplication, normalization, exponent, conditional instructions, division step and infinite levels of repeat and block repeat.

**Support:** DSP Group provides a full set of advanced graphical-user-interface-based development tools, including an optimizing C/C++ compiler, an assembler, a linker, common-object-file-format converters, a debugger with an emulation interface and an extendable simulator (ASSYST) for system-on-chip simulation, a profiler, and the Evaluation Development Platform. DSP Group has a large infrastructure of third-party vendors offering software, tools, and design services.

## TeakLite
## DSP Group, www.dspg.com

TeakLite is a 16-bit, fixed-point DSP soft-core, single-MAC (multiply-accumulate) architecture that is code-compatible with the OakDSPCore instruction set. It enhances the OakDSPCore in several areas, mainly portability. It is a soft core and is process- and library-independent; it increases operating speed by 30% in the same process technology and reduces power consumption by architecture and complex power-reduction mechanisms. Its new design methodology better meets ASIC-design-environment requirements by employing a single-edge design (still with four pipeline stages) and full or partial testability and by using standard memories.

- TeakLite is the first licensable DSP in a soft-core implementation.
- Devices feature high code density, high performance, low-power, and small size.

TeakLite has a configurable memory size, a data-address-arithmetic unit, a multiplier, an ALU (arithmetic-logic unit), four 36-bit accumulators, a bit-manipulation unit, zero-overhead loop mechanisms for repeat and block repeat, and support for a C compiler. Its instruction set includes microcontroller instructions, and it has a high code density. It has user-definable registers for hardware acceleration, coprocessor support, or both; cycle-stealing DMA support, burst-mode DMA support, or both; and power-management operation modes.

**Addressing modes:** TeakLite supports register, single- and double-indirect, short- and long-immediate, short- and long-index , and stack-pointer addressing modes. It supports circular (modulo) buffering for all its pointers and direct addressing for the entire 64k-word data space. In addition, it has a program-memory-indirect addressing mode.

**Special instructions or integral peripheral functions:** Instructions include single-cycle minimum/maximum calculation with pointer latching, double-precision calculations, normalization, exponent, conditional accumulator modifications, division step, read-modify (add/subtract/OR/AND/XOR)-write, test 16-bit mask bits and test bit, delayed return, interruptible single-word repeat loop and block repeat, 36-bit shift left or right in a single cycle, and a bank exchange of alternative registers.

**Support:** DSP Group provides a full set of advanced graphical-user-interface-based development tools, including an optimizing C/C++ compiler, an assembler, a linker, common-object-file-format converters, a debugger with an emulation interface and an extendable simulator (ASSYST) for system-on-chip simulation, a profiler, and the Evaluation Development Platform. DSP Group has a large infrastructure of third parties offering software, tools, and design services.

## Carmel DSP 10xx Core
## Infineon Technologies, www.infineon.com/dsp

The Carmel DSP 10xx is a 16-bit, fixed-point core for integration into system-on-chip designs. The core combines both a predefined instruction set and CLIW (configurable-long-instruction-word) technology to deliver high performance and an efficient DSP instruction rate without sacrificing power dissipation or code-compactness requirements. User-defined CLIW instructions execute in one clock cycle without wait states or setup overhead, allowing software code to switch between execution units on a clock-by-clock basis. This feature is useful for reducing the cycle count of the inner loops, increasing the overall performance of application code by a factor two or more over software implementations that use only instructions from the predefined instruction set. The Carmel DSP is inherently modular with extensive libraries of synthesizable system peripherals and memories, as well as software functions.

- 200 MHz, single-cycle instruction rate achieves as many as 2.8 billion operations per second.
- User-defined instructions provide exceptional flexibility without performance penalty.
- Performance, power-dissipation, and price are optimized for wireless, wired, and consumer applications.

**Addressing modes:** The Carmel DSP supports immediate addressing in the instruction; direct referencing to operand registers, or indirect referencing to an operand data memory. Addresses may be 16 or 32 bits, with linear, bit-reverse, and modulo (aligned and non-aligned) address modification. Each address modification includes increment, decrement, and offset modifications.

**Special instructions or integral peripheral functions:** CLIW technology allows user definition of 96-bit instructions, comprising as many as six individual parallel subinstructions, to increase the efficiency of the core in tight DSP loops. The DSP includes built-in support for Viterbi decoding as well as for minimum/maximum searches. You can add peripheral functions via the Infineon standard FPI (Flexible Peripheral Interconnect) bus.

**Support:** Third-party partners provide a complete suite of hardware and development tools to aid in system design and application-software development. Infineon also provides development-chip implementations of the core with large on-chip memory and multiple I/O options, as well as evaluation boards and hardware and software cosimulation models.

## Carmel DSP 20xx Core
## Infineon Technologies, www.infineon.com/dsp

The Carmel DSP 20xx is a second-generation, reconfigurable DSP core for integration into SOC (system-on-chip) designs. The 16-bit, fixed-point core base architecture uses CLIW (configurable-long-instruction-word) technology to define application-specific instructions and PowerPlug technology to design optimized execution units for specific algorithms. The core includes six standard arithmetic units and accommodates as many as four additional PowerPlug modules to boost computation-intensive functions, such as MAC (multiply-accumulate), Viterbi, image, and video functions. SOC designers benefit from a reconfigurable instruction set and the high-performance of custom execution units. The combined effect is a dramatic increase in flexibility and greater efficiency than fixed cores that use only predefined instruction sets. The Carmel DSP is inherently modular with extensive libraries of synthesizable system peripherals and memories, as well as software functions.

- Core consumes as little as 0.07 mW/MMAC (million MACs), operating at 0.9V.
- Device enables user-defined execution units for maximum efficiency.
- The Carmel DSP is ideal for next-generation-wireless, broadband, multimedia, and consumer-electronics applications.

**Addressing modes:** The Carmel DSP supports immediate addressing in the instruction set; direct referencing to operand registers; or indirect referencing to an operand data memory. Addresses may be 16 or 32 bits, with linear, bit-reverse, and modulo (aligned and nonaligned) address modification; each address modification can include increment, decrement, and offset modifications.
**Special instructions or integral peripheral functions:** CLIW technology allows user definition of 96-bit instructions, comprising as many as six individual parallel subinstructions for better efficiency. Designers can also create as many as four PowerPlug modules, which are user-defined execution units designed and optimized for specific applications and seamlessly integrated into the regular tool chain.
**Support:** Third-party partners provide a complete suite of hardware and development tools to aid in system design and application-software development. Infineon also provides development-chip implementations of the core with large on-chip memory and multiple I/O options, as well as evaluation boards and hardware/software cosimulation models.

## DSP56800 family
## Motorola, www.motorola.com/semiconductors

The DSP56800 family is the first digital-signal-processing architecture designed from the ground up to integrate into one chip a powerful DSP architecture and instruction set with embedded-microcontroller capabilities. Combining the traditional control functions of a microcontroller with the performance of a DSP allows control-based systems to run advanced algorithms, bringing precision and reliability.

- Devices feature an advanced PWM module.
- Integrated, mixed-signal peripherals include ADCs, onboard voltage regulation, controller-area-network 2.0 A/B modules, and asynchronous serial communications interfaces.
- The DSP56800 has a high-speed synchronous SPI.

**Addressing modes:** Devices in the DSP56800 family support 14 addressing modes, including indirect, indexed, immediate, absolute, and others.
**Special instructions or integral peripheral functions:** None
**Support:** Motorola joins Metrowerks and other independent development-tool companies to provide a development environment that includes advanced software-generation and -debugging tools, evaluation-and-development systems cards, and integrated software modules. The offering includes a software-development kit and an application-programming interface that enables portability of applications software between microcontrollers and DSPs, preserving customers' investments in legacy code.

## ZSP400 Core
## LSI Logic, www.lsilogic.com

The ZSP400 is a fully synthesizable, high-performance, 16-bit, fixed-point DSP based on LSI Logic's ZSP architecture. The ZSP400 synthesizable core targets customer-design-flow environments. The ZSP400 provides an optimized superscalar DSP processor that can efficiently support both control- and DSP-algorithm functions with a peak of 800 MIPS. The ZSP400 Core is a 200-MHz processor with a 40-bit accumulator that can simultaneously issue and execute four instructions delivering as many as 400 million MAC (multiply-accumulate) operations per second. The core can also sustain one 32×32-bit MAC per cycle. The ZSP400 is ideally suited to be embedded with ARM, MIPS, or other host processors, into a single-silicon device and complemented with memory, Ethernet, WAN, telecomm, memory, and mixed-signal cores for complete system-on-a-chip functions with the highest level of integration available in the industry today.

- Devices feature fully synthesizable superscalar DSP architecture.
- The ZSP400 is available in LSI Logic's Coreware library or as licensable RTL.
- The ZSP400 is optimized for voice-over-network and communications-infrastructure applications.

**Addressing modes:** The ZSP architecture supports bit-reversed addressing in either hardware or software. It includes hardware support for immediate or register-content, indexed, indirect, and register-to-register addressing modes. Four looping instructions and associated registers support zero-overhead loops. The flexible instruction set allows you to use any register as source or destination operand.

**Special instructions or integral peripheral functions:** The ZSP architecture has special instructions to support add-compare-select and parallel-add and -subtract operations for FFT and Viterbi decoding, single-cycle bit-manipulation to calculate real and imaginary components in a complex multiplication operation, and specialized load instructions.

**Support:** The ZSP400 core features hardware based scheduling to allow concurrent execution of multiple instructions in each clock cycle without the need for special programming techniques. Internal and external data and instruction interfaces provide flexible RAM-, peripheral-, and coprocessor-integration capabilities. The ZSP400 integrates onboard timers, real-time interrupt generation and ICE (in-circuit-emulation) capabilities. The dual MAC units and dual ALUs (arithmetic-logic units) can perform two 16×16-bit MACs or one 32×32-bit MAC per cycle.

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## DSP56800E family
## Motorola, www.motorola.com/semiconductors

The newly enhanced DSP56800E core family of DSPs offers low-power, low-cost, single-chip options for a growing range of applications in industrial, motor-control, automotive, and converging telecommunications and data-communications markets. With a core design that consumes little power, Motorola has opened a number of new battery-powered and portable applications for its signal-processing products, such as portable digital audio, Internet appliances, and personal digital assistants. Combining microcontroller and DSP capability on one IC, rather than relying on two chips, reduces system cost and power demands while improving efficiency and performance.

- The 56800E combines DSP performance with microcontroller-control functions.
- The device includes choices for single-chip options featuring low power consumption and a maximum fivefold improvement in MIPS performance over the 56800 core.
- Processor supports industrial, motor-control and automotive applications, and telecomm and datacomm markets.

**Addressing modes:** Devices in the DSP56800E family support 19 addressing modes, such as indirect, indexed, immediate, absolute, and others. These modes support 8-, 16-, and 32-bit data transfers.

**Special instructions or integral peripheral functions:** The instruction set is an enhanced version of the DSP56800 that offers true software-stack-support subroutines and flexible, user-defined, multilevel interrupt-priority support.

**Support:** The Metrowerks Compiler and IDE tool set support the 56800E core. The products have development boards for software development and companion daughtercards for market-specific applications.

## SC100 core architecture, includes the SC140 core and the SC110 core
## StarCore Technology Center (from Agere Systems and Motorola SPS), www.starcore-dsp.com

StarCore's SC100, the company's first-generation of DSP core architecture, is a 16-bit, fixed-point architecture with an extensible 16-bit instruction word. The SC100 is a scalable architecture across performance, power, and cost requirements targeting the needs of computation-intensive communications applications. Low power dissipation per function helps extend battery life and helps you meet power-per-channel budgets, and compact code density requires less memory, thereby reducing system cost. Customers can use one DSP architecture for entry-level as well as advanced applications. And the ability to reuse key kernels and code from low-end to high-end applications can save OEM developers time and money.

- Variable-length execution set promotes scalable resources.
- Associated compiler detects parallelism and group-independent instructions.
- Four parallel DALUs (data-arithmetic-logic units) and two address-generation units surround five-stage pipeline.

**Addressing modes:** The SC100 architecture supports register-direct mode, address-register indirect mode, PC (program-counter)-relative modes, and special address modes.

**Special instruction or integral peripheral functions:** The SC100 multipliers support all combinations of signed and unsigned operands and both fractional and integer formats. The SC100 architecture supports a single-instruction-multiple-data version of maximum and minimum additions and subtractions (MAX2, ADD2, SUB2). The SC140 can perform eight 16-bit additions or maximum and minimum operations per cycle; the SC110 can perform two. The SC100 architecture also includes the MAX2VIT, which works with the VSL (Viterbi shift left) to support efficient implementation of Viterbi decoding algorithms. A user-defined instruction-set accelerator module enhances the SC100 basic instruction set.

**Support:** StarCore creates low-level, baseline development tools, including a C Compiler; an assembler; a linker; an instruction-set simulator; and optimized, hand-coded C-callable DSP-core libraries to assist programmers in their application development. StarCore has also partnered with third-party developers, such as Green Hills, Tasking, Embedded Power, and Enea Ose Systems.

## TMS320C5000
## Texas Instruments, www.dspvillage.com

The TMS320C5000 DSP platform uses a modified Harvard architecture and includes the TMS320C54x and the new TMS320C55x DSP generations. The C55x DSPs are source-code-compatible with the C54x DSPs. The C54x focuses on low power consumption, but the C55x takes power efficiency to a new level: A 300-MHz C55x delivers a maximum fivefold improvement in performance over and dissipates as little as one-sixth the core power of a 120-MHz C54x. The C55x has 12 independent buses (the C54x has eight). Both architectures include one program bus and an associated program-address bus. The C55x bus is 32 bits wide, and the C54x bus is 16 bits wide. The C55x has three data-read buses and two data-write buses; the C54x has two data-read buses and one data-write bus. Each data bus also has its own address bus. The corresponding address buses are 24 bits wide on the C55x and 16 bits wide on the C54x.

- The C55x is one of the most power-efficient programmable DSPs in the industry.
- All C5000-platform DSPs are source-code compatible.
- Devices consume as little as 0.9V and 0.05 mW/MIPS with a maximum performance of 800 MIPS.

The C5000 DSP platform has 17 power-efficient, code-compatible DSPs sampling or shipping in high volume.

**Addressing modes:** The C54x supports single data-memory-operand addressing that also supports 32-bit operands. It also supports dual-data-memory-operand addressing, which parallel instructions use. It provides immediate, memory-mapped, circular, and bit-reversed addressing. In addition to the C54x modes, the C55x supports absolute addressing; register-indirect addressing; and direct-addressing, or displacement, mode. The C55x includes dedicated registers to support circular addressing for instructions that use indirect addressing. Your program can simultaneously use as many as five independent circular buffer locations with as many as three independent buffer lengths. These circular buffers have no address-alignment constraints. The C54x supports two circular buffers of arbitrary lengths and locations.

**Special instructions or integral peripheral functions:** The C54x performs dedicated-function instructions, such as FIR filters; single and block repeat; eight parallel instructions; multiply, accumulate, and subtract (10 multiply instructions); and eight dual-operand memory moves. The C55x also has special instructions that take advantage of the additional functional units and increase parallelism capabilities. User-defined parallelism allows you to combine instructions to perform two operations. You can also combine a built-in parallel instruction with a user-defined parallel instruction.

**Support:** EXpressDSP Real-Time Software Technology comprises the TMS320 DSP Algorithm Standard, a standard set of coding conventions and application programming interfaces; the Code Composer Studio integrated development environment; DSP/BIOS, a scalable real-time kernel; and the world's largest third-party network. TI also offers data converters, power-management products, and power-amplifier products to support the C5000 DSP platform.

## ARC Tangent
## ARC Cores Inc, www.arccores.com

- Integrated RISC/DSP core simplifies design and software development.
- Configurable architecture lets developers customize the core.
- CPU with DSP extensions requires only about 57,100 gates.

ARC Tangent is a synthesizable, user-configurable, 32-bit RISC microprocessor core with optional DSP extensions. Developers can add and configure the DSP extensions in minutes with ARChitect, a graphical design tool that automatically generates RTL output. DSP features include 16×16-, 24×24-, and dual 16×16-bit MACs (multiply-accumulate) units with 8 guard bits for the accumulator; saturating add-and-subtract instructions; fractional arithmetic; zero-overhead looping; as many as four banks of XY memory that support single-cycle parallel data moves and fast context switching; and support for modulo and bit-reverse addressing with variable-offset pre-increment and postincrement modes. ARC Cores also offers a DSP function library written in optimized assembly language. The ARC Tangent core is available in VHDL and Verilog, is synthesizable with industry-standard design tools, and is portable to any foundry or process technology. The integrated RISC/DSP core lowers costs, reduces power consumption, accelerates development, and allows programmers to use one tool chain.

**Addressing modes:** The address-generation units for the ARC Tangent XY memories support modulo and bit-reverse addressing with variable-offset pre-increment and postincrement modes. The ARC Tangent core supports as many as four banks of XY memories of 512 bytes to 16 kbytes and has a user-extensible register file.

**Special instructions or integral peripheral functions:** Instructions include saturating add and subtract, fractional arithmetic, normalize (find first bit), swap, minimum/maximum, 16×16-bit MAC, 24×24-bit MAC, dual 16×16-bit MAC, 32×32-bit barrel shifter, 32×32-bit multiplier, and as many as four banks of XY memories. The fully conditional, user-extensible instruction set has as many as 16 user-defined condition codes.

**Support:** The ARC Tangent RISC/DSP core comes with an extensively documented VHDL or Verilog source code. ARC Cores provides customer training and technical support. MetaWare, an ARC Cores subsidiary, provides software-development tools and technical support. A growing network of ARC Certified Design Centers provides a full range of design services.

## ADSP-21000 SHARC DSP family
## Analog Devices Inc, www.analog.com

- Architecture is programmable, high-performance, and compatible with 32-bit fixed and floating-point code.
- Seamless multiprocessing configurations require no glue hardware.
- Rich peripheral sets offer integrated on-chip features.
- Architecture maintains balance between core performance and I/O bandwidth.

The ADSP-21161N joins the SHARC family of processors. Although the device is ideal for floating-point applications, it can also perform fixed-point computation. This new member of the SHARC family is based on Super Harvard ARChitecture and has both SIMD (single-instruction-multiple-data) and SISD (single-instruction-single-data) functions. The SHARC SIMD core contains two computational blocks—each with a multiplier, an ALU (arithmetic-logic unit), a data-register file, and a barrel shifter—that process in parallel in SIMD mode. The core also contains dual DAGs (data-address generators), independent data- and address-memory buses, a program sequencer with zero-overhead looping, an instruction cache, and a timer. While the core operates at full speed, the I/O processor moves data on and off chip. SHARC DSPs integrate 1 to 4 Mbits of on-chip SRAM; as many as four serial ports, six link ports, and 14 zero-overhead DMA channels; an SPI-compatible port; a synchronous-DRAM controller; a parallel host interface; cluster multiprocessing support; and an IEEE JTAG standard 1149.1 test-access port with on-chip emulation. The two independent on-chip, dual-ported SRAM blocks are selectable between program and data memory. The independent synchronous serial ports operate in TDM (time-division-multiplexed) multichannel mode and, on the ADSP-21065L and ADSP-21161, offer $I^2S$ mode, which is useful for audio applications.

**Addressing modes:** The ADSP-21000 SHARC DSPs support absolute and relative-direct addressing, and pre- and postmodify register and immediate-value indirect addressing. It also supports modulo and bit-reverse addressing modes. The dual-ported memory allows independent data transfers from the core and the I/O. Three on-chip buses allow two data transfers from the core and one from I/O in one cycle.

**Special instructions or integrated peripheral functions:** The ADSP-21000 SHARC family features distributed on-chip bus arbitration. Devices allow you to connect as many as six processors (two for the ADSP-21065L) in parallel, plus a host. All SHARC instructions execute in one cycle. Special instructions include bit manipulation, division iteration, reciprocal of square-root seed, conditional subroutine call, single and block repeat with zero-overhead looping, average of two numbers, bit packing and unpacking fixed to and from floating-point conversion, and conditional execution of most instructions. SHARC supports IEEE-754 single-precision floating-point, 32-bit fixed-point, and a 40-bit extended IEEE format for additional accuracy.

**Support:** Analog Devices offers a complete set of software- and hardware-development tools, including the VisualDSP and VisualDSP++ IDE , ICEs, and a developers' evaluation kit. VisualDSP/VisualDSP++ supports fast-and-easy development, debugging, and deployment.

## TMS320C6000

## Texas Instruments, www.dspvillage.com

TI's C6000 DSP platform is a general-purpose DSP based on VLIW (very-long-instruction-word) architecture. This architecture includes the fixed-point C62x, the floating-point TMS320C67x, and the new C64x. The C62x has eight independent, multipurpose functional units and can perform two 16×16-bit MAC (multiply-accumulate) operations per cycle. The C64x is object-code-compatible with the C62x but has significant architectural enhancements, such as four 16×16-bit MAC operations per cycle and an initial operating frequency of 600 MHZ. TI created the C67x instruction set by adding floating-point capabilities to six of the C62x's eight functional units, so the C67x instruction set is a superset of the C62x instruction set. The C6000 lacks a dedicated MAC unit. Instead, it performs MAC operations by using separate multiply and add instructions. TI has nine high-performance, code-compatible C6000 DSP products that are available for sampling or are shipping in high volume. The C6000 platform offers software and development systems to enable advanced imaging and third-generation wireless- and broadband-communications-infrastructure applications

- The C64x architecture will in time scale to more than 1.1 GHz.

**Addressing modes:** The C6000 performs linear and circular addressing. However, unlike most other DSPs, which have dedicated address-generation units, the C6000 calculates addresses using one or more of its functional units.

**Special instructions or integral peripheral functions:** All C6000 processors conditionally execute all instructions, a method of reducing branching. On the C64x, the MPYU4 instruction performs four 8×8-bit unsigned multiplies. The ADD4 instruction performs four 8-bit additions. All functional units can perform dual 16-bit addition/subtraction, compare, shift, minimum/maximum, and absolute-value operations. The M units and four of the six remaining functional units support quad 8-bit addition/subtraction, compare, average, minimum/maximum, and bit-expansion operations. TI has also added instructions that operate directly on packed 8- and 16-bit data.

**Support:** The C6000 includes eXpressDSP Real-Time Software Technology, which comprises the TMS320 DSP Algorithm Standard a single, standard set of coding conventions and application-programming interfaces; the Code Composer Studio IDE; DSP/BIOS, a scalable real-time kernel; and a large third-party network.

## BOPS, www.bops.com
## ManArray family

**Suitable applications:** Five configurations using the ManArray architecture target different application areas. BaseRay supports cellular base stations and wireless LANs. WirelessRay supports mobile-wireless-appliance and phone applications. DSLRay supports DSL SOHO (small-office/home-office) and central-office equipment. VoiceRay supports VoIP (voice-over-Internet Protocol) SOHO and carrier-gateway applications. MoRay supports digital-audio and -video applications.

- Hardware scalability allows system architects to match the performance levels, cost, and power points of each DSP core with the application requirements.
- Instructions execute in one or two cycles with single-cycle throughput, providing a simple pipeline.
- One programming model, a simple pipeline design, and the independence of each level of parallelism make BOPS IP cores easy to program.

**Number of bits**: The basic BOPS DSP Core PE (processing element) consists of an arithmetic-logic unit, a MAU (multiply-accumulate unit), a DSU (data-select unit), a load unit, and a store unit—that can each support 8-,16-,32-, and 64-bit packed-data formats. The architecture is scalable by adding PEs, each with five execution units to increase the performance proportionally.

**Product description:** This fully scalable, synthesizable DSP architecture is programmable and reusable in an array of implementations for evolving communications, mobile-multimedia, and wireless applications.

**Addressing Modes:** The BOPS architecture supports SIMD (single-instruction-multiple data), MIMD (multiple-instruction-multiple-data) and SMIMD (synchronous-multiple-instruction-multiple-data) operation. A fully programmable, patternable, scalable DMA engine supports the addressing modes and data-flow management necessary to meet the computational requirements of the high-performance, scalable DSP cores.

**Special instructions or integral peripheral functions:** You can easily integrate all functions—from a RISC coprocessor to a simple PCI interface—into a BOPS SOCs (systems on chip).

**Support:** The BOPS SDK (software-development kit) is an ever-growing development tool box that tightly integrates tools for application-software programmers, SOC designers, firmware designers, and system architects into one development environment. The Jordan EVB (evaluation board) enables BOPS customers to evaluate BOPS' highly scalable ManArray architecture. The Jordan EVB is also a powerful tool for the development of high-performance DSP applications that use the BOPS' ManArray-based family of programmable DSP cores.

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## CS49300 family
## Cirrus Logic Inc, www.cirrus.com

**Suitable applications:** audio-decoder applications, such as Dolby Digital, Dolby Pro Logic II, DTS-ES, MPEG, AAC, MP3, THX-ES, and MLP.

**Number of bits:** 24

- The architecture is optimized for audio applications.
- Input and control modes are flexible.
- Rich onboard memory can mean standard applications require no external memory.

The CS49300 is a family of multistandard audio decoders targeting audio-video receivers, set-top boxes, and DVD players. The DSP incorporates dual DSP cores for enhanced audio processing. The family offers several standard audio-processing algorithms.

**Addressing modes:** Flexible addressing modes handle audio data and coefficient access using direct and indirect, linear and modulo, bit-reverse, and pointer-modification modes.

**Special instructions or integral peripheral functions:** The CS49300 family employs control-dedicated input FIFO, bit-extraction for parsing audio stream, and output-buffer control for block-level PCM transfer to DACs.

**Support:** Cirrus Logic has developed all standard applications for advanced audio processing, allowing the company to offer its customers a strong technical-support program.

## ISL5314 Direct Digital Synthesizer
## Intersil Corp, www.intersil.com

**Suitable applications:** wireless communications, cellular base stations
**Number of bits:** 14 bits for analog channels; 48 bits for digital I/O

- Devices achieve 125M-sample/sec output-sample rate with 5V digital supply.
- Devices achieve 100M-sample/sec output-sample rate with 3.3V digital supply.
- Parallel control interface, serial control interface, or both allow fast tuning.

As part of Intersil's growing CommLink family of signal-processing and high-speed-converter options, the ISL5314 DDS (direct digital synthesizer) delivers the fine-tuning resolution, accurate digital control, and high-speed performance that today's evolving wireless-communications standards require.

The ISL5314 DDS targets wireless-communications equipment, such as base stations that link cellular telephones to the wired telephone network, satellite receivers, video-broadcast equipment, instrumentation, and cellular test equipment. DDS generates frequency-agile, highly accurate, and low-distortion output waveforms that are critical in generating clear wireless signals.

**Addressing modes:** Addressing modes include microprocessor-interface and serial-interface modes. The microprocessor interface loads a set of master registers, which are then transferred to a slave set of registers. The serial interface loads a tuning frequency control, and you can use it in addition to the parallel microprocessor interface for loading the center frequencies, the offset frequencies, or both.
**Special instructions or integral peripheral functions:** A stand-alone DDS integrates a 48-bit, programmable-carrier numerically controlled oscillator and a high-speed, 14-bit DAC.
**Support:** Intersil offers evaluation boards, application notes, data sheets, and central-application support.

## HSP50415 WPM
## Intersil Corp, www.intersil.com

**Suitable applications:** cellular base stations, satellite terminals, point-to-point microwave, and WLL (wide-area-local-loop).
**Number of bits:** 16

- I- and Q-shaping FIR filters are programmable.
- Output sample rates reach 100M samples/sec.
- Input-data rates reach 25M samples/sec (I/Q).
- 32-bit carrier NCO is programmable.

Intersil's CommLink HSP50415 WPM (wideband programmable modulator) is a standard IC that provides global flexibility for SDR (software-definable-radio) applications. The programmable HSP50415 supports multiple modulation schemes and is designed into point-to-point-microwave, satellite, cellular-base-station, WLL, phased-array-antenna, and other last-mile wireless Internet applications. The HSP50415 enables SDR applications by processing tomorrow's evolving communication standards to ensure compatibility with future system requirements.

**Addressing modes:** The HSP50415 is highly configurable, with 16 writeable/readable control registers and four addresses reserved for generating internal control signals. It also uses a parallel-bus microprocessor interface and indirect addressing through a constellation mapper.
**Special instructions or integral peripheral functions:** The HSP50415 WPM combines in one IC shaping and interpolation filters, a complex modulator, timing-and-carrier numerically controlled oscillators, and a 12-bit dual-channel DAC.
**Support:** Intersil provides evaluation boards, application notes, data sheets, and central-application support.

## D16k, D36k
## DSP Group Inc, www.dspg.com

- Families offer low-cost, low-power DSP architecture and integrated peripherals.
- D16k and D36k suit digital-telephony and voice-over-packet applications, including VoIP and VoDSL.

**Suitable applications:** digital telephony, digital answering machines, cordless telephony, VoIP (voice over Internet Protocol), VoDSL (voice over digital-subscriber line), DVRs (digital voice recorders), and hands-free car kits.
**Number of bits:** 16

The D16k and D36k families of integrated digital-telephony processors contain all the necessary peripheral circuits on chip for this application. Chips contain an advanced 16-bit DSP core (PineDSPCore for D16k and TeakLiteDSPCore for D36k), as well as sigma-delta ADCs and DACs, I/O amplifiers, mixers, and multiplexers. The devices also integrate oscillator circuitry, PLL references, and voltage regulators. Besides traditional telephony functions, the D36k family also include baseband controller modules providing a glueless interface to the RF chips for digital and spread-spectrum cordless telephony.
**Special instructions or integral peripheral functions:** Instructions include analog front-end with sigma-delta codecs, amplifiers, multiplexers, micropower oscillators, PLLs, and core-voltage regulators.
**Support:** DSP Group offers a full suite of development tools with JTAG in-system emulators, debuggers, assemblers, linkers, and C compilers.

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## LSI402ZX
## LSI Logic, www.zsp.com

- Architecture is four-way superscalar.
- Devices reach a maximum throughput of 800 DSP MIPS at 200 MHz.
- The LSI402ZX is optimized for voice-over-network and communications-infrastructure applications.

**Suitable applications:** Voice over networks, customer-premises equipment, such as integrated-access devices, wireless infrastructure, audio applications
**Number of bits:** 16

The LSI402ZX is a high-performance, 16-bit, fixed-point DSP based on the LSI Logic ZSP400 DSP core. The ZSP400 architecture applies several advances in microprocessor design to the LSI402ZX implementation. The device is also software-compatible with all other ZSP-architecture products and combines code density, performance, and ease of use.

The device operates at 180 MHz for a maximum throughput of 720 MIPS. The RISC architecture is easy to program and uses a four-way-superscalar pipeline with five stages to process as many as 20 instructions at a time. The processor's execution unit contains two MAC (multiplier-accumulate) units and two ALUs (arithmetic-logic units).

The LSI402ZX provides 124k words of on-chip instruction and data cache supported by an eight-channel DMA controller that can transfer instructions or data to and from memory. For optimum I/O performance and flexibility, the LSI402ZX contains two high-speed TDM (time-division-multiplexed) serial ports, one 16-bit host-interface port; an external-memory-interface unit; an eight-pin, programmable I/O port; and an IEEE 1149.1 JTAG port for program downloading and debugging.
**Addressing modes:** The LSI402ZX provides hardware for implementing two independently enabled circular buffers as well as for reverse-carry addressing. Reverse-carry addressing is an alternative mode of indexing the base-address registers. It speeds fast FFTs and similar operations that require you to modify the next-load or next-store address in a reverse-carry fashion.
**Special instructions:** The LSI402ZX can perform a single-cycle add-compare-select for Viterbi decoding. In addition, the device supports bit manipulation, 32-bit arithmetic and logic operations, and two-cycle complex multiply instructions.
**Support:** Both LSI Logic and third-party tools fully support the LSI402ZX. LSI provides a Gnu-based compiler, a linker, and an assembler for Windows and Solaris platforms. The LSI402ZX also supports a full commercial tool chain from Green Hills Software and Corelis JTAG debugging tools. In the first quarter of 2001, LSI Logic will release the ZOpen algorithm-integration framework for the LSI402ZX, supporting seamless integration into RTOSs, including Enea.

## LSI403Z
## LSI Logic, www.zsp.com

**Suitable applications:** voice-over-network, customer-premises equipment, such as integrated-access devices, and audio.
**Number of bits**: 16

The LSI403Z is a low-power, 16-bit, fixed-point DSP based on the LSI Logic ZSP400 DSP core. The ZSP400 architecture applies several advances in microprocessor design to the LSI403Z implementation. The device is also software-compatible with all other ZSP-architecture products and combines code density, performance, and ease of use.

The device operates at 150 MHz for a maximum throughput of 600 RISClike MIPS. The RISC architecture is easy to program and uses a four-way-superscalar pipeline with five stages to process as many as 20 instructions at a time. The processor's execution unit contains two MAC (multiply-accumulate) units and two ALUs (arithmetic-logic units).

- Devices achieve 600-MIPS peak performance at low cost.
- Device consumes low power per voice channel.
- The LSI403Z is ideal for voice-over-DSL Internet-access-device designs.

The LSI403Z provides 32k words of on-chip instruction and data cache supported by an eight-channel DMA controller that can transfer instructions or data to and from memory. For optimum I/O performance and flexibility, the LSI403Z contains two high-speed TDM (time-division-multiplexed) serial ports, one 8-bit host-interface port, an external-memory-interface unit, a four-pin, programmable I/O port, and an IEEE 1149.1 JTAG port for program downloading and debugging.

**Addressing modes:** The LSI403Z provides hardware for implementing two independently enabled circular buffers as well as for reverse-carry addressing. Reverse-carry addressing is an alternative mode of indexing the base-address registers. It speeds FFTs and similar operations that require you to modify the next-load or next-store address in a reverse-carry fashion.
**Special instructions:** The LSI403Z can perform a single-cycle add-compare-select for Viterbi decoding. The device also supports bit manipulation, 32-bit arithmetic and logic operations, and two-cycle complex-multiply instructions.
**Support:** Both LSI Logic and third-party tools fully support the LSI403Z. LSI provides a Gnu-based compiler, a linker, and an assembler for Windows and Solaris platforms. It also supports a full commercial tool chain from Green Hills Software and Corelis JTAG debugging tools. LSI Logic will release in the first quarter of 2001 an algorithm-integration framework (ZOpen) for the LSI403Z, supporting seamless integration to RTOSs, including Enea.

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## DSP56300 Family DSPs
## Motorola, www.motorola-dsp.com

**Suitable applications:** networking infrastructure

The DSP56300 family is optimized for networking-infrastructure applications yet fully programmable. It targets multimedia-, telecommunications-, networking-, and wireless-infrastructure applications. The DSP56300 provides an outstanding power-to-performance ratio, with an intelligent power-management system and low-voltage process technology. Products range from 100 MIPS, 3.6V to 270 MIPS with only 1.8V of power consumption. Some of these DSPs contain large amounts of on-chip memory.

- Single-pin compatibility provides an upgrade path to higher performance, lower power family members.
- Large-memory configurations offer the opportunity to add features and support for more voice and data channels.
- EFCOP (Enhanced Filter Coprocessor) optimizes voice quality without sacrificing channel processing.

**Addressing modes:** The DSP56300 family supports standard addressing modes, such as register-direct, address register-indirect, and program-counter-relative with special modes specifying the operand or operand address in a field of the instruction or implicitly referencing an operand.
**Special instructions or integral peripheral functions:** The DSP56300 family supports Viterbi-shift-left instructions that optimize the implementation of the Viterbi decoder algorithm.
**Support:** Motorola provides application-software modules, software-development tools, and evaluation modules for the 56300 family.

## MSC8101 DSP
## Motorola, www.motorola-dsp.com

**Suitable applications:** networking-infrastructure applications, such as wireless infrastructure, IP (Internet Protocol) telephony, ATM edge/carrier switches, modem banks, and centralized DSP services
**Number of bits:** 16

With its unique combination of a SC140 DSP core, programmable CPM (communications-processor module), and PowerPC bus interface, the MSC8101 offers signal-processing performance, flexible network connectivity, and seamless system integration.

The SC140 core, comprising four 16-bit ALUs (arithmetic-logic units), uses an internal 300-MHz clock to deliver 1200 MMACS (million multiply-accumulate instructions/second) or 3000 RISC MIPS of usable DSP performance. The MSC8101 CPM is a programmable 32-bit RISC-protocol machine that allows connectivity to such standard network backbones as ATM, Fast Ethernet, and fast TDM (time-division-multiplexing) highways.

- Devices achieve high signal-processing performance.
- Network connectivity is flexible.
- System integration is seamless.

**Addressing modes:** The MSC8101 supports standard addressing and variable-width access to data memory, including byte, word, long-word, and two-long-word accesses.
**Special instructions or integral peripheral functions:** The MSC8101 family supports Viterbi-shift-left instructions that optimize the implementation of the Viterbi decoder algorithm.
**Support:** Motorola provides software-development tools, including an assembler, a linker, a C/C++ compiler, an optimizer, a simulator, and other utilities. Application-software modules include speech coders, echo cancelers, faxes, and modems. Motorola is working with a variety of third-party developers to supply a choice of IDEs and RTOSs.

## iDSP
## Oak Technology Inc, www.oaktech.com

**Suitable applications:** imaging
**Number of bits:** 32

Oak Technology's iDSP family is a programmable device for low-cost, high-performance, image-processing applications, such as imaging-enabled printers and multifunction peripherals. The iDSP provides designers with all the flexibility of a software-based image processing option at the price and performance of fixed-function silicon. Based on an advanced SIMD (single-instruction-multiple-data) parallel-processing architecture, the iDSP takes full advantage of the parallelism inherent in image data to deliver better price and performance in image-processing applications than conventional DSPs based on VLIW (very-long-instruction-word) architectures. The newest addition to the iDSP family, the PM-44ix, contains four symmetric parallel-pipelined processors and runs at 233 MHz to deliver 3700 MIPS and 930 million multiply-accumulate instructions/sec. The iDSP programming environment includes an IDE, an image-processing library, and an evaluation board.

- Devices feature advanced SIMD parallel-processing architecture.
- Device delivers software-based image processing.
- Flexible platform accelerates time to market.

**Addressing modes:** To maximize memory bandwidth, all memory accesses in the iDSP are 32-bit. Specialized extraction and insertion units allow bit fields of any size to be manipulated within 32-bit registers.
**Special instructions or integral peripheral functions:** The iDSP instruction set contains specialized instructions for manipulating image data and coordinating parallel processing.
**Support:** Oak Technology's worldwide direct-sales and support organization supports the iDSP.

## MECA Voice over Packet Processors
## PMC-Sierra, www.pmc-sierra.com

**Suitable applications:** VoATM (voice over ATM) and VoIP (voice over IP)
**Number of bits:** 128-bit VLIW (very-long-instruction-word) packet processing and interface: 32-bit PCI 2.1 bus interface

The MECA family comprises: the MECA-4A for VoATM applications and the MECA-4I for VoIP applications. The MECA architecture was the first to integrate DSP and packet-processing functions into one device. The device replaces more than 10 devices, including eight general-purpose DSP chips, typically used in current designs. The MECA processors are designed to bridge the legacy voice network with the new high-speed data networks by converting voice traffic into compressed ATM or IP packets.

- High-channel-density processors target VoATM and VoIP applications.
- Devices achieve toll-quality speech compression.
- Devices handle ATM-cell formatting and packetization.

Each MECA device can process as many as 96 channels of compressed voice or 512 channels of uncompressed voice, including ATM or IP packetization. MECA fundamentally changes the scale and economies of next-generation voice equipment by enabling systems that are scalable to tens of thousands of voice channels at a lower power and cost per channel than previously possible. The MECA processors are fully programmable to enable voice-coding and protocol upgrades through firmware.
**Addressing modes:** Devices support 32-bit wide and 64-bit burst modes with an address space as large as 32 Mbytes.
**Special instructions or integral peripheral functions:** The products executes DSP and packetization functions.
**Support:** For document information, contact document @pmc-sierra.com; for application Information, contact apps@pmc-sierra.com.

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## QuickDSP
## QuickLogic, www.quicklogic.com

**Suitable applications:** VoIP (voice over IP)
**Number of bits:** 8 to 24 (user configurable)

QuickLogic's new QuickDSP family, the third line of ESPs (Embedded Standard Products), combines the power of a DSP with the flexibility of programmable logic. This dedicated hardware option achieves a fourfold improvement over traditional programmable logic for a range of functions, including floating-point arithmetic, FIR, IIR, adaptive filtering, FFTs, FEC (forward-error correction), and HDLCs (high-level data-link control).

- Devices offer high performance, great flexibility, and low power consumption.
- Integrated option couples with a portfolio of intellectual property for a systems on chip.

QuickLogic embeds a reprogrammable computational unit and RAM blocks into silicon to allow DSP design engineers to efficiently implement complex algorithms and multiple-sample processing across single or multiple datapaths without sacrificing performance. Because the logic usage is efficient even for complex designs, design engineers can use smaller, less expensive devices with the added advantage of low power consumption.
**Addressing modes:** With the 18 ECUs (embedded computational units) on the largest part (QL7180), you can implement 18 8-bit MAC (multiply-accumulate) functions per cycle. You can configure the ECUs for eight arithmetic functions via a dynamically reprogrammable instruction-set sequencer. This flexibility gives designers the ability to reconfigure the ECU for algorithm-intensive applications, such as adaptive filtering.
**Special instructions or integral peripheral functions:** The QuickDSP comes with 18 ECUs on the largest part (QL7180), an instruction-set sequencer, and multiple dual-port 2304-bit RAM modules. These RAM modules vary from 12 to 36 blocks for a total of 82.9 kbits of RAM. The QuickDSP comes with four PLLs that create a master clock from a lower input-frequency clock. One of the four PLLs is multiplexed with the dedicated clock, and the remaining three connect to global clocks.
**Support:** QuickLogic provides state-of-the-art real and virtual support for its customers' software and hardware technical issues. The Corporate Applications Group at QuickLogic is also at customers' disposal. The group is available by e-mail, phone, or fax. In addition, an array of support options is available from the QuickLogic Web site at www.quicklogic.com/support1/.

## RSC 300/364
### Sensory Inc, www.sensoryinc.com

**Suitable applications:** speech recognition, speech synthesis
**Number of bits:** 16

The RSC-300/364 from the Interactive Speech family of products features a high-performance microcontroller with on-chip ADC, DAC, RAM, and ROM (RSC-364 only). It brings a high degree of integration and versatility into low-cost, power-sensitive applications in consumer-electronic products. The RSC-300/364 is a single-chip option that combines the flexibility of a microcontroller with advanced-speech-processing technology, including high-quality speech recognition, speech and music synthesis, speaker verification, and record and playback. The RSC-300/364 uses a neural network to perform speaker-independent speech recognition, and devices achieve high-quality speech synthesis using a time-domain-compression scheme that improves conventional ADPCM (adaptive differential pulse-code modulation). In addition to providing the necessary horsepower to perform speech recognition and speech synthesis, the processor has sufficient cycles available for general-purpose product control through 16 I/O lines.

- Speaker-independent and -dependent recognition and word spotting is highly accurate.
- Devices achieve low power, low voltage, and low system cost.

**Addressing modes:** Devices support sequential modes.
**Special instructions:** None
**Support:** Sensory's tools include the 364 development kit, the 364 demonstration unit, the Voice Extreme (C-programmable version), full turnkey product development, and linguistics services.

## TMS320C2000
### Texas Instruments, www.dspvillage.com

**Suitable applications:** digital motor control and power conversion
**Number of bits:** 16

TI DSPs control even the most advanced motor types, such as switched-reluctance motors that offer inherent advantages, including highest speed and torque per current, robustness, and lowest manufacturing cost. DSPs negate the traditional disadvantages, such as high-torque ripple in electric motors. TI has developed a comprehensive line of DSP options that is driving the digital-motion-control revolution. With the addition of the new TMS320C28x DSP generation core, the TMS320C2000 DSP platform sets the standard for performance and peripheral integration in digital controllers. It uniquely combines as much as 400 MIPS of processing power with on-chip peripherals, such as flash memory, ultrafast ADCs, onboard event managers providing PWM and I/O features to drive all motor types, and robust CAN (controller-area network) modules.

- Devices achieve the highest performance and peripheral integration in the industry.
- The broadest product portfolio of code-compatible DSPs is optimized for motor control.

**Addressing modes:** The C2000 DSP platform includes indirect and direct addressing.
**Special instructions or integral peripheral functions:** TI's C2000 DSP platform offers the most integrated peripheral and DSP set in the market. This set includes flash memory, an ADC, and an event manager with pulse-width modulation. It also includes the CAN module, SCI, and SPI.
**Support:** The open-software platform for digital control supports the C2000 DSP platform and all major types of motors with control options. The software platform builds on the elements of eXpressDSP real-time software technology to allow the C2000 to reach its full potential. TI's broad library of proven, interoperable motor-control software modules extends the algorithm standard for digital-motor control.

## TMS320DRE200 Eureka DAB digital baseband
## Texas Instruments, www.dspvillage.com

**Suitable applications:** Eureka DAB digital radio
**Number of bits:** 16

- Low-cost baseband reduces system costs by as much as 40%.
- Devices reduce baseband power consumption by 27% over the competition.
- You can quickly and easily update and upgrade products via software.
- TI and third-party support eases designing.

The ETSI 300 401-compliant DRE200 baseband performs channel and source decoding on one chip. In addition, the digital baseband can decode all Eureka modes and performs user-interface functions. The DRE200 baseband is compatible with standard audio DAC interfaces and can interface to an external microcontroller, DRAM, and SRAM. Devices achieve disturbance-free operation during multiplex subchannel reconfiguration or ensemble switching, and they can feed data to external TPEG (Transport Protocol Expert Group) or MOT (multimedia-object-transfer) decoders and external memory.
**Addressing modes:** The DRE200 offers immediate, absolute, accumulator, indirect, direct, stack, and memory-mapped-register addressing modes.
**Special instructions or integral peripheral functions:** None
**Support:** A $5000 evaluation board based on the DRE200 baseband will be available to OEMs in the first quarter of 2001. The DRE200 samples will be ready in the first quarter of 2001.

## TMS320DA250 (DA250)
## Texas Instruments, www.dspvillage.com

**Suitable applications:** Internet audio
**Number of bits:** 16

- Battery consumption is the lowest in the industry (typically 17 mW for MP3 applications).
- First device in the Internet-audio industry to offer dual-MAC and embedded-USB support.
- First device in industry to offer built-in secure-digital memory stick, and SP3 (secure-portable-player-platform) security software.

TMS320DA250 is a member of TI's C55x generation of fixed-point DSPs. It is the fourth-generation chip for use in the Internet-audio market and is ideal for portable Internet-audio players, car stereos, home-audio juke-boxes and other audio applications. The DA250 supports the broadest offering of digital-audio formats and digital-rights-management technologies. The GPIO (general-purpose I/O) functions provide sufficient pins for status, interrupts, and bit I/O for LCDs, keyboards, and media interfaces for a "microless" design. The parallel interface operates either as a slave to a microcontroller or as a media interface. The media interface includes an ATA flash card or a memory buffer for spinning media. In addition, new peripherals include USB, real-time clock, watchdog timer, $I^2C$ interface, and a secure-device ID. Integrating these components result in reductions in cost, size, and power while maintaining code compatibility.
**Addressing modes:** Addressing modes include synchronous SRAM interfaces, SDRAM interfaces, or both, with GPIO capabilities or enhanced 16-bit EHPI16 with GPIO capabilities. The device also includes an enhanced 16-bit host-port interface (EHPI16) mixed with address bus.
**Special instructions or integral peripheral functions:** Integrated peripherals include a real-time clock, a USB1.1 interface, a memory stick and MMC/SD (multimedia-card/secure-digital) interfaces, an $I^2C$ multimaster and slave interface, two 16-bit timers and one watchdog timer, and an integrated 10-bit ADC for battery monitoring, buttons, and control signals.
**Support:** TI offers support for DA250 through regional training classes on C5000 DSP architecture.

## TMS320DSCx family, including TMS320DSC21 and TMS320DSC24
## Texas Instruments, www.dspvillage.com

**Suitable applications:** TMS320DSC21 targets digital still cameras; TMS320DSC24 suits image- and audio-processing for multimedia-Internet-appliance applications
**Number of bits:** 16, plus an onboard ARM7.

The TMS320DSC21 and TMS320DSC24 DSPs are digital-imaging systems on a single chip that combine a TMS320C5000 DSP and an ARM7TDMI RISC processor to perform media-processing and system-control functions. The chips integrate a video encoder with an on-screen display, an SDRAM controller with a bandwidth transfer rate of 320 Mbytes/sec, and a preview engine that performs 30-frame/sec NTSC and PAL previewing (DSC21). It can also achieve real-time frame capture in burst mode to the full resolution of the 2 million-pixel image sensor.

- Devices enables multifunction digital-imaging devices on one chip.
- Devices enable fast time to market through software and hardware development.
- Code compatibility enables single platform, multiple-product strategy.

With the DSCx DSPs, cameras and Internet appliances can capture high-resolution still photos with a fast shot-to-shot delay, record video clips with audio, and download and play music from the Internet. The chip supports the broadest offering of popular digital- audio and -video formats, including real-time MPEG 1, MPEG 4, JPEG, MJPEG, H.263 and MP3, as well as data-communication standards, such as IrDA, USB, and RS-232.
**Addressing modes:** Addressing modes include SDRAM, SRAM, flash, and removable media interfaces. The SDRAM transfer rate is 80 Mbytes/sec, with both ×32 (DSC21/24) and ×16 (DSC24) interface capabilities. DSC24 enables 2-D-to-2-D data transfer from SDRAM to an on-chip image buffer, as well as direct SDRAM access via an SDRAM controller. ARM can access the DSP via the host-port interface, and its bus controller has on- or off-chip access to general-purpose I/O, flash, Compact Flash, and Smart Media applications.
**Special instructions or integral peripheral functions:** In addition to the TMS320C54x DSP-generation instruction set, the DSCxx DSP subsystem incorporates imaging enhancements to provide fast-block-based processing for imaging- or video-encoding and -decoding functions.
**Support:** TI supports these products on a worldwide basis, offering evaluation modules, technical-training classes, and customer-application support.

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## TMS320IP5472; www.ti.com/sc/ipphone
## Texas Instruments, www.dspvillage.com

**Suitable applications:** IP (Internet Protocol) telephony
**Number of bits:** 16

An enterprise IP phone is a desktop business telephone that delivers enhanced, low-cost telephony services by leveraging the corporate-data-networking infrastructure (LAN). Within an IP private-branch exchange, the telephones use standards, such as H.323, SIP, and Megaco. TI's award-winning IP telephone is a low-risk, complete option for IP phone manufacturers that consists of TI's 5472 IP phone processor and includes VoIP (voice-over-IP)-enabling Telogy Software products and a codec chip. The low-power C54xDSP is integrated with a RISC microprocessor and includes a three-port Ethernet switch and all the necessary peripherals for an IP phone. The device achieves voice quality that matches or exceeds the audio quality of traditional circuit-switched telephony. It also leads the industry in availability of features and standards support and is driving the evolution of related network protocols. Telogy Software products, which feature a variety of standards-based packet-network protocols and user interfaces, enable manufacturers to create a diverse portfolio of customer applications.

- Optimal silicon/software platform supports a variety of IP phone options.
- Field-proven software emphasizes quality of service, interoperability, and remote monitoring.
- Devices allow rapid implementation of customer-unique features and services.
- TI provides committed roadmap support, code compatibility, process technology, and production facilities.

**Addressing modes:** The device supports all addressing modes of TI's TMS320C54x DSP family. In addition, it supports all addressing modes of the ARM7TDM RISC CPU.
**Special instructions or integral peripheral functions:** The device implements the complete instruction set of both TI's TMS320C54x DSP CPU and the ARM7TDM RISC CPU from ARM Ltd.
**Support:** Technical support includes product upgrades, product training, maintenance support, repair, and other customer services.

## PalmDSPCore
## DSP Group, www.dspg.com

PalmDSPCore is a family of three licensable soft-cores—of 16, 20, and 24 bits each—designed to meet market-segment requirements. PalmDSPCore has an ILP (instruction-level-parallelism) architecture, dual-MAC (multiply-accumulate) parallel architecture, multiple-instruction-multiple-data and single-instruction-multiple-data instructions, seven computation units working in parallel, and symmetrical cross-coupled MAC paths. PalmDSPCore has two multipliers, a three-input ALU (arithmetic-logic unit), a three-input split ASU (adder-subtracter unit), four orthogonal 40-bit accumulators, and a bit-manipulation unit including insert-extract operations. The DAAU (data-address-arithmetic unit) contains two additional ASUs. It has powerful built-in accelerators for FFT and Viterbi decoding and support for a C compiler, RTOS, and bit-exact standards. It has zero-overhead-loop mechanisms with infinite levels of repeat and block repeat and six pipeline stages. It also has coprocessor support and 16 user-defined registers for hardware acceleration.

- Family includes three licensable cores of 16, 20, and 24 bits each.
- SIMD and MIMD operations use seven arithmetic units.
- High code density has only 16- and 32-bit instruction width.

PalmDSPCore has high code density through variable instruction width (16 or 32 bits). Maximum PalmDSPCore program-memory space is 16M words. PalmDSPCore is a process- and library-independent, fully synthesizable soft core and is compatible with previous SmartCores generations.

**Addressing modes:** PalmDSPCore supports circular (modulo) buffering, register, short- and long-direct, short- and long-immediate, relative, bit-reversal, double-word, parallel, index-based, and stack-pointer addressing. It also supports a maximum quadruple-indirect addressing mode (for example, to simultaneously feed four inputs of the two multipliers or four inputs of the split ALU).

**Special instructions:** The device supports single, parallel, and multiparallel instruction sets. It also supports dual-MAC, complex FFT butterfly in two cycles, Viterbi decoding in two cycles, microcontroller instructions, delayed branches and return, normalization, exponent, conditional instructions (parallel moves, logic, arithmetic, accumulator), and infinite levels of repeat and block repeat.

**Support:** DSP Group provides a full set of advanced graphical-user-interface-based development tools, including an optimizing C/C++ compiler, a common-object-file-format assembler and linker, a debugger with an emulation interface and extendable simulator for system-on-chip simulation, a profiler, and the Evaluation Development Platform. DSP Group has a large infrastructure of third parties, offering tools and design services.

## Vectra DSP Engine
## Tensilica Inc, www.tensilica.com

The Vectra DSP Engine is a powerful Xtensa coprocessor targeting high-performance DSP applications using fixed-point arithmetic. The DSP engine uses an SIMD (single-instruction-multiple-data) architecture, optimized for executing DSP algorithms. The architecture allows you to maintain data, coefficient, and intermediate results of an algorithm in vector registers. The engine's large vector-register file reduces memory bandwidth requirements and improves overall system performance.

- Vectra meets embedded-applications needs by using efficient vector architecture.
- The Vectra DSP Engine provides a powerful vector-register combination for high bandwidth and low power dissipation.
- Unlike rigid DSP processors, Xtensa with Vectra delivers optimized options for control and signal processing.

The Vectra engine simultaneously supports single- and double-width operand sizes for greater computational accuracy. This setup allows you to store the results of multiply or MAC (multiply-accumulate) operations in double-width registers and eliminates overflow and accumulated truncation or rounding errors within an algorithm iteration.

Vectra is a key Xtensa building block in a unified option for high-integration system-on-chip designs. For the first time, you can rapidly configure one processor architecture to satisfy both control and signal-processing requirements. The unified option ensures a common foundation for software development, simulation, and RTOS environments.

**Addressing modes:** The Vectra DSP engine's four addressing modes include immediate (base register and offset value in instruction) and indexed (base register and index register) addressing with or without updates to the base register. Base-register updates are used, for example, as general-purpose auto increments of the base register.

**Special instructions or integral peripheral functions:** The Vectra DSP Engine adds approximately 100 new instructions to the Xtensa instruction-set architecture. A variety of special vector instructions includes vector-load/store instructions, ALU (arithmetic-logic-unit) and shift operations, and a sophisticated set of multiply operations for multiple MAC/ALU units. You can fine-tune the Vectra DSP engine for the best possible signal-processing fit. Designer-configurable parameters include the number of elements in a vector register, the number of memory or register bits per element, and multiplier and multiplicand widths.

**Support:** Like all Xtensa options, software-development tools fully support Vectra. Such tools include new world-class, vectorizing compilers, assemblers, simulators, RTOSs (VxWorks and Nucleus), co-verification tools (Seamless and Eaglei), and instruction-set simulators, as well as optimized DSP libraries.