

Edited by Brad Thompson

Single-wire keypad interface frees microcontroller-I/O pins

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IN MOST KEYPADS, pressing a key closes a contact that bridges two lines in an xy matrix. If you use a microcontroller to detect a key closure, checking the states of $(x+y)$ lines requires an equal number of I/O pins. Occupying only one free I/O pin, the circuit **Figure 1** communicates with a microcontroller by generating a single pulse each time someone presses a key. The pulse's width is proportional to the number of the pressed

key, and the microcontroller identifies the pressed key by measuring the pulse's width.

IC₂, a CMOS LMC555 version of the popular 555 timer, operates as a monostable one-shot multivibrator. In the circuit's resting state, a transistor internal to IC₂ at Pin 7 shunts C₆, and IC₂'s output at Pin 3 remains at logic low. Pressing any key on the keypad connects two resistors from two groups—R₁ and R₂ in one

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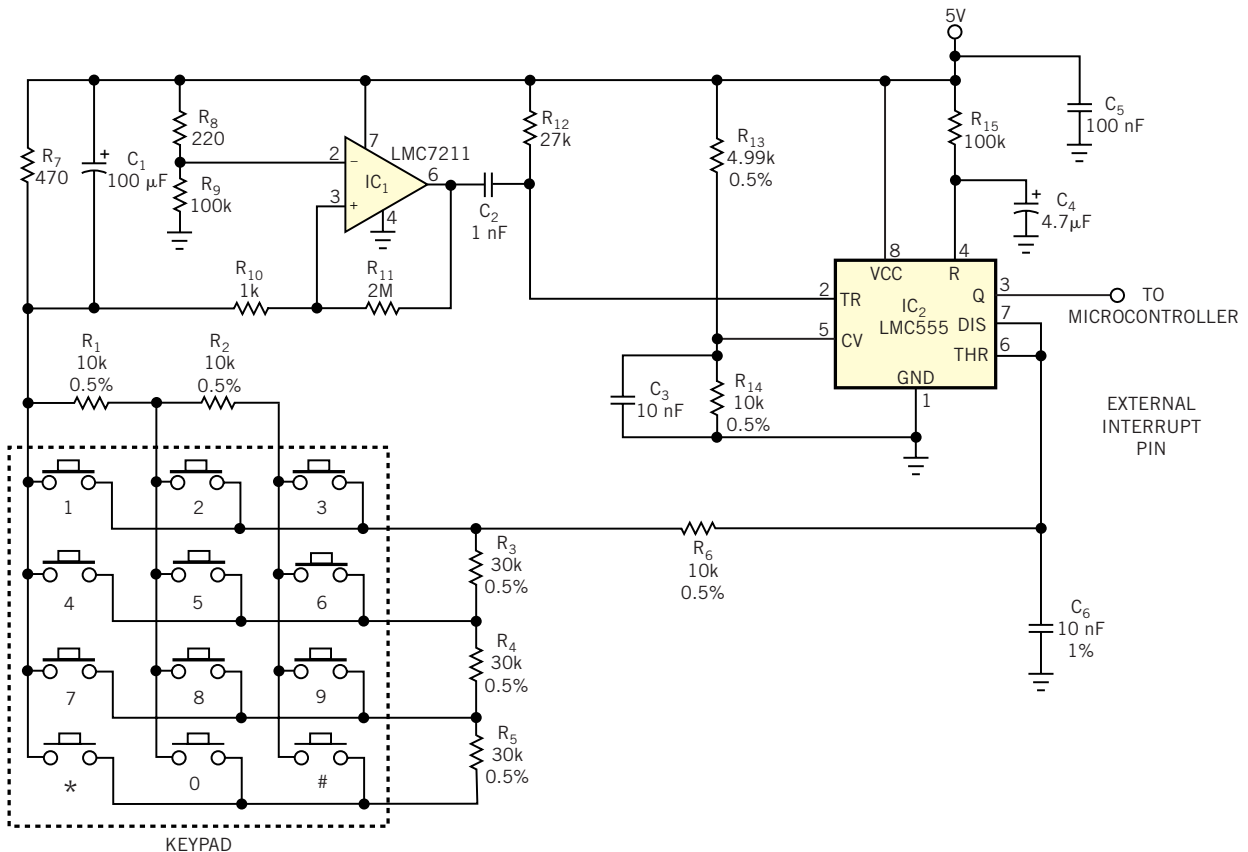


Figure 1

Two ICs form a pulse-width-modulated keypad interface that uses only one microcontroller-input pin.

group and R_3 , R_4 , and R_5 in the other—in series with R_6 . The sum of the two resistors varies in 10-k Ω increments, and the total resistance is proportional to the number of the pressed key.

Pressing any key draws current through R_6 , R_7 , and the selected keypad resistors and raises the voltage at IC₂'s Pin 7. After C_1 charges, introducing a short delay that's sufficient to eliminate keypad-switch contact-closure bounce, CMOS comparator IC₁ detects the small voltage drop established across R_7 . The output of IC₁ (Pin 6) goes from 5 to 0V, which in turn triggers Pin 2 of IC₂. Timer IC₂'s output (Pin 3) goes high and begins to charge capacitor C_6 at a time constant

that depends on the selected key. When the voltage across C_6 reaches two-thirds of V_{CC} , or 3.333V, Pin 3 goes low and discharges C_6 . The following equation calculates IC₂'s output pulse width, T : $T = 1.1 \times R_8 \times C_6$, where R_8 equals the sum of the selected keypad resistors and ranges from 10 to 120 k Ω . The pulse width spans a range of 110 to 1320 μ sec in increments of 110 μ sec.

The smallest relative change in pulse width occurs at the longest pulse ratio, 110/1320, or 8.33%. This ratio provides sufficient margin to allow use of standard $\pm 1\%$ tolerance or better components for those in **Figure 1** that are $\pm 0.5\%$ and $\pm 1\%$. Resistors R_{13} and R_{14} com-

pensate for variations in IC₂'s internal voltage dividers by forcing the voltage at Pin 5 to two-thirds of power-supply voltage V_{CC} .

The keypad circuit's output pulse drives the external interrupt input, RA₂, of a Microchip 16F630 microcontroller. **Listing 1**, available at the online version of this Design Idea at www.edn.com, presents an interrupt routine for the 16F630 that measures the pulse width, verifies that its tolerance is within $\pm 40 \mu$ sec, and returns a numerical value of 1 to 12 that corresponds to the pressed key. As a safeguard against erroneous data, the routine returns an error code if the pulse width falls outside certain limits. □

Calculator program evaluates elliptic filters

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MANY DESIGNERS consider the elliptic-transfer function to be the most useful of all analog-filtering functions, because of its steep roll-off at the band edges. You can use a Texas Instruments model V200 Voyage programmable calculator and the program in **Listing 1** at the Web version of this Design Idea at www.edn.com to evaluate a lowpass el-

liptic filter by finding its characteristic's poles and zeros. To do so, this program implements Darlington's algorithm (**Reference 1**). The program accepts as input the filter's maximum passband-attenuation ripple in decibels, its stopband and passband frequencies in radians per second, and its order, or number of poles (**Figure 1**).

As an example, calculate the zeros, poles, and stopband attenuation of an elliptic, fifth-order, analog lowpass filter with maximum gain of 0.1 dB and stopband frequency of 1.05 radians/sec. **Figure 2** illustrates the calculator's display screens during program execution. □

REFERENCE

1. Darlington, Sidney, "Simple Algorithms for Elliptic Filters and Generalizations Thereof," *IEEE Transactions on Circuits and Systems*, Volume CAS-25, No. 12, December 1978, pg 975.

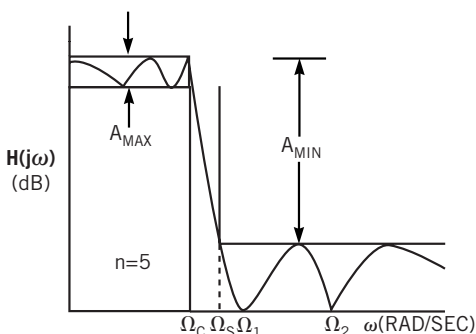


Figure 1 The characteristics of an elliptic filter's amplitude response include in-band ripple, passband-attenuation and stopband frequencies, and stopband attenuation.



Figure 2

These screens show the calculator's display from the introductory menu (a), entering filter parameters (b), calculating values for filter-response zeros (c), calculating value for out-of-band attenuation (d), and calculating values for filter-response poles (e).

Dynamic-load circuit determines a battery's internal resistance

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THE SIMPLEST MODEL of a battery comprises an ideal voltage source that connects in series with a resistance whose value—often a few milliohms—depends on the battery's electrochemical condition and construction. If you attempt to use an ordinary ac milliohmmeter containing a kilohertz-range ac excitation source to measure a battery's internal resistance, you get erroneous results due to capacitive effects, which introduce losses. A more realistic battery model includes a resistive divider that a capacitor partially shunts (Figure 1). In addition, a battery's no-load internal resistances may differ significantly from their values under a full load. Thus,

for greatest accuracy, you must measure internal resistance under full load at or near dc.

The circuit in Figure 2 meets these requirements and accurately measures internal resistance over a range of 0.001 to 1Ω at battery voltages as high as 13V. One section of an LTC6943 analog switch, IC_{2A}, alternately applies 0.110 and 0.010V derived from 2.5V voltage reference IC₃ and resistive divider R₂, R₃, and R₄ to IC₁'s input.

Amplifier IC₁, power MOSFET Q₁, and associated components form a closed-loop current sink that provides an active load for the battery under test via Q₁'s drain. Diode D₁ provides reversed-bat-

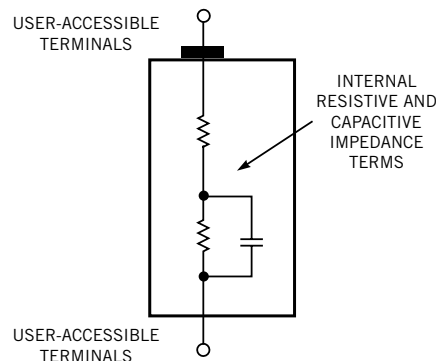


Figure 1 An elementary model of a battery's internal impedance includes resistive and capacitive elements, but the capacitive elements introduce errors in ac-based impedance measurements. For improved accuracy, analyze the battery's voltage drop at a frequency near dc.

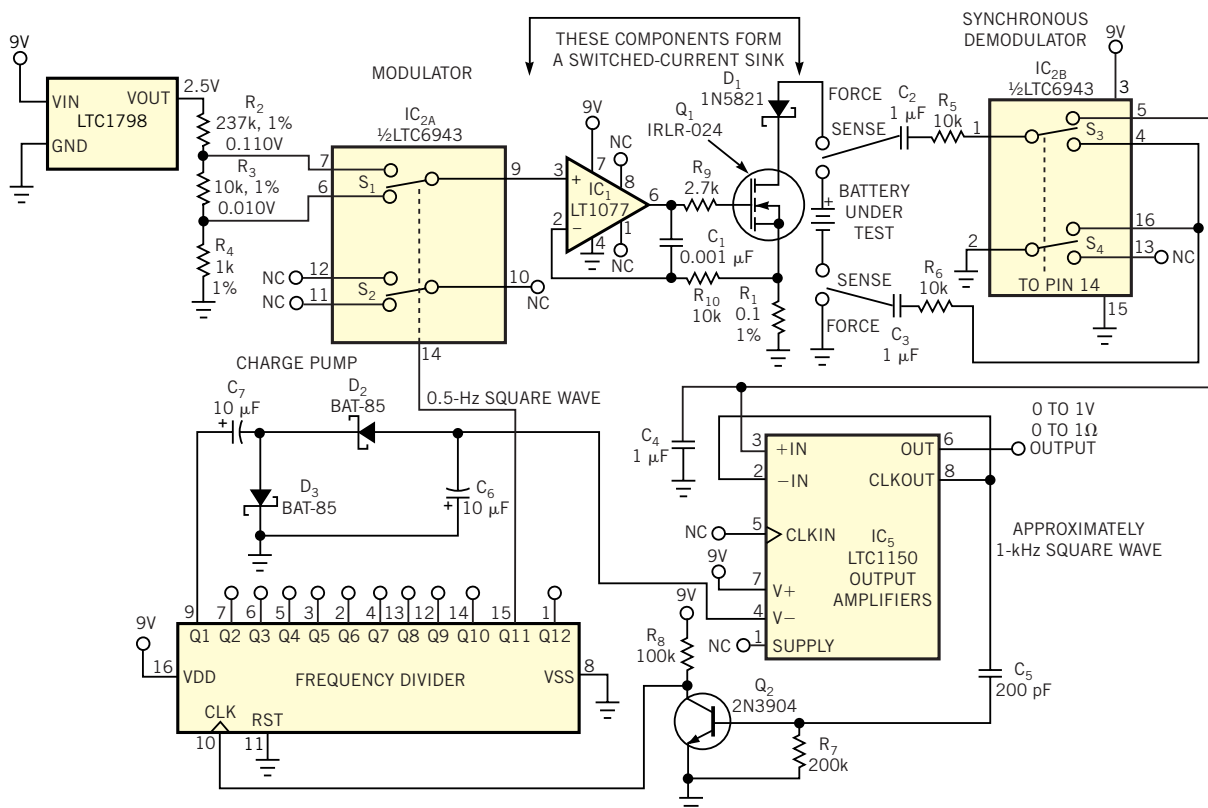


Figure 2

This circuit determines a battery's internal resistance by repetitively applying a calibrated discharge current and measuring the resultant voltage drop across the battery's terminals.

tery protection. The voltage at amplifier IC₁'s positive input and the voltage drop across R₁ determine the load applied to the battery. In operation, the circuit applies a constant-current load comprising a 1A, 0.5-Hz square wave biased at 100 mA to the battery.

The battery's internal resistance develops a 0.5-Hz amplitude-modulated square-wave signal at the Kelvin connections attached to the battery. A synchronous demodulator comprising analog switches S₂ and S₃ in IC_{2B} and chopper-

stabilized amplifier IC₅ processes the sensed signal and delivers a 0 to 1V analog output that corresponds to a battery-resistance range of 0 to 1Ω.

Via transistor Q₂, amplifier IC₅'s internal approximately 1-kHz clock drives CMOS binary divider CD4040, IC₄, which supplies a 0.5-Hz square-wave clock drive for the switches in IC₂. In addition, a 500-Hz output from IC₄ powers a charge-pump circuit that delivers approximately -7V to IC₅'s negative power-supply input and thus enables

IC₅'s output to swing to 0V.

The complete circuit consumes approximately 230 μA, allowing nearly 3000 hours of operation from a 9V alkaline-battery power supply. The circuit operates at a supply voltage as low as 4V with less than 1-mV output variation and provides an output accuracy of 3%. The circuit accommodates a battery-under-test voltage range of 0.9 to 13V, but you can easily alter discharge current and repetition rate to observe battery resistance under a variety of conditions. □

Battery automatic power-off has simpler design

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A PREVIOUS DESIGN IDEA describes a simple way to automatically turn off a battery after a preset on period to save battery life (Reference 1). This Design Idea presents a simpler way to perform the same function (Figure 1). Two gates of IC₁, a quad two-input NAND Schmitt trigger, form a modified flip-flop. When you apply a 9V battery to the circuitry, the output of IC_{1A} goes high because the initial voltage on C₁ is zero. The

output of IC_{1B} is low, which feeds back to IC_{1A} through R₂. C₃ charges up through R₃. The output of IC_{1C} goes high because R₆ is connects to ground. A P-channel MOSFET switch, Q₁, is off, and the output IC_{1D} goes high, which in turn charges C₄ through R₂.

When you push momentary switch S₁, IC_{1A}'s output goes low because both of its inputs are high, and this output forces IC_{1B}'s output high. The value of R₂ is

much smaller than R₃, so that C₃ holds a logic-level high when S₁ stays on. When S₁ goes off, C₃ discharges through R₃.

You can turn off the MOSFET switch in one of two ways. When tantalum capacitor C₂ is charged up such that the voltage on IC_{1C}'s input becomes lower than its threshold V₋, IC_{1C}'s output changes from low to high; this action turns off the MOSFET switch. C₂ and R₆ determine the duration of this automat-

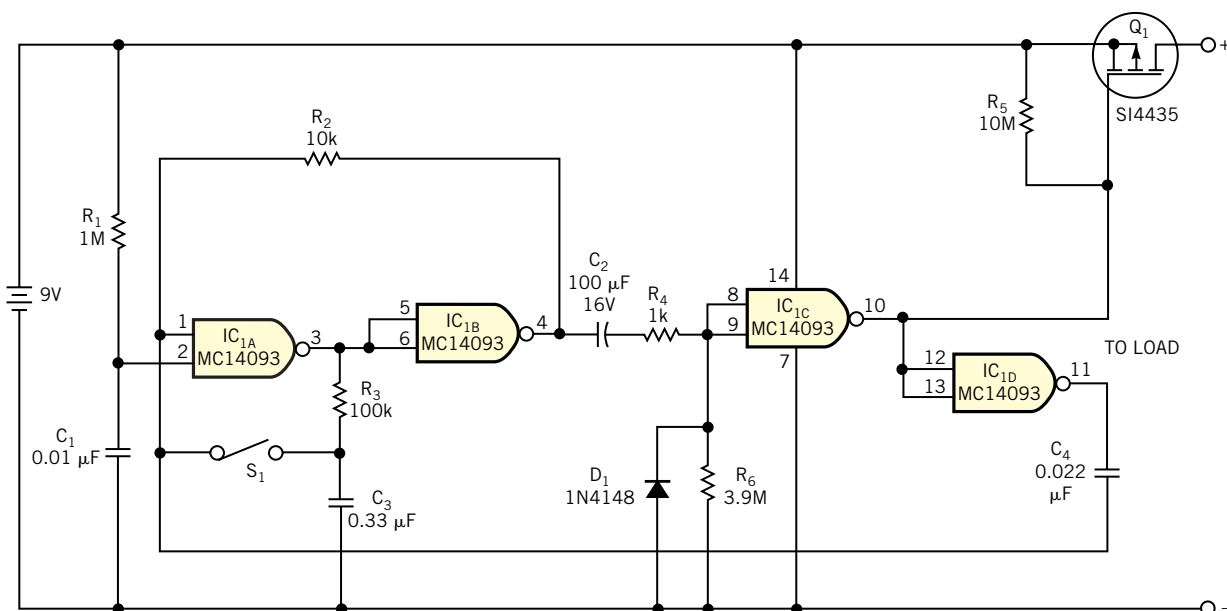


Figure 1

An improved power-off circuit automatically disconnects the battery after a preset on period.

ic turn-off. With the values shown, the turn-off takes approximately six minutes. Meanwhile, the high-to-low transition on IC_{1D}'s output forces IC_{1A} and IC_{1B} back to standby status through C₄.

Alternatively, you can manually turn off the MOSFET switch by pushing S₁. Because the voltage on C₃ is low, closing S₁ forces IC_{1A}'s outputs high and IC_{1B}'s outputs low. The high-to-low transition

on IC_{1B}'s output forces IC_{1C}'s output to be high, which turns off the MOSFET. Because the value of C₂ is fairly large, D₁ provides a quick discharge route, and R₄ limits the discharge current.

This circuitry consumes less than 0.2 μA of power during standby operation. Because the MOSFET switch has a low on-resistance, it has only a 2-mV loss when the load current is 100 mA. Add an

LED with a current-limiting resistor in series to the load side if you need a power-on indicator. □

REFERENCE

1. Gimenez, Miguel, "Scheme provides automatic power-off for batteries," *EDN*, May 13, 2004, pg 92.

Control a processor's power supply in real time

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IN BATTERY-POWERED applications in which power management is key, a microprocessor may adjust its core voltage corresponding to an increase or a decrease in clock speed, allowing full processing power when necessary but not wasting excess power when idle. The circuit of **Figure 1** shows how an embedded processor can control its own supply voltage via a simple step-down converter and

inexpensive digital potentiometer.

In this application, an embedded ADSP-BF531 Blackfin processor adjusts the wiper setting of IC₂, an AD5258 digital potentiometer, via its I²C interface. In turn, IC₂ controls the output of IC₁, an ADP3051 current-mode, PWM step-down converter that supplies as much as 500 mA at output voltages as low as 0.8V. When its output is in regulation, IC₁'s

feedback input rests at 0.8V, and IC₂ and R₂ form a voltage divider.

The ADSP-BF531 imposes several design requirements: Its core power-supply voltage must maintain its accuracy to within 25 mV and offer an adjustment resolution of 50 mV per step from 0.8 to 1.2V. Also, the processor requires 1.2V at start-up to initialize its clocks. Finally, the power controller must prevent its output

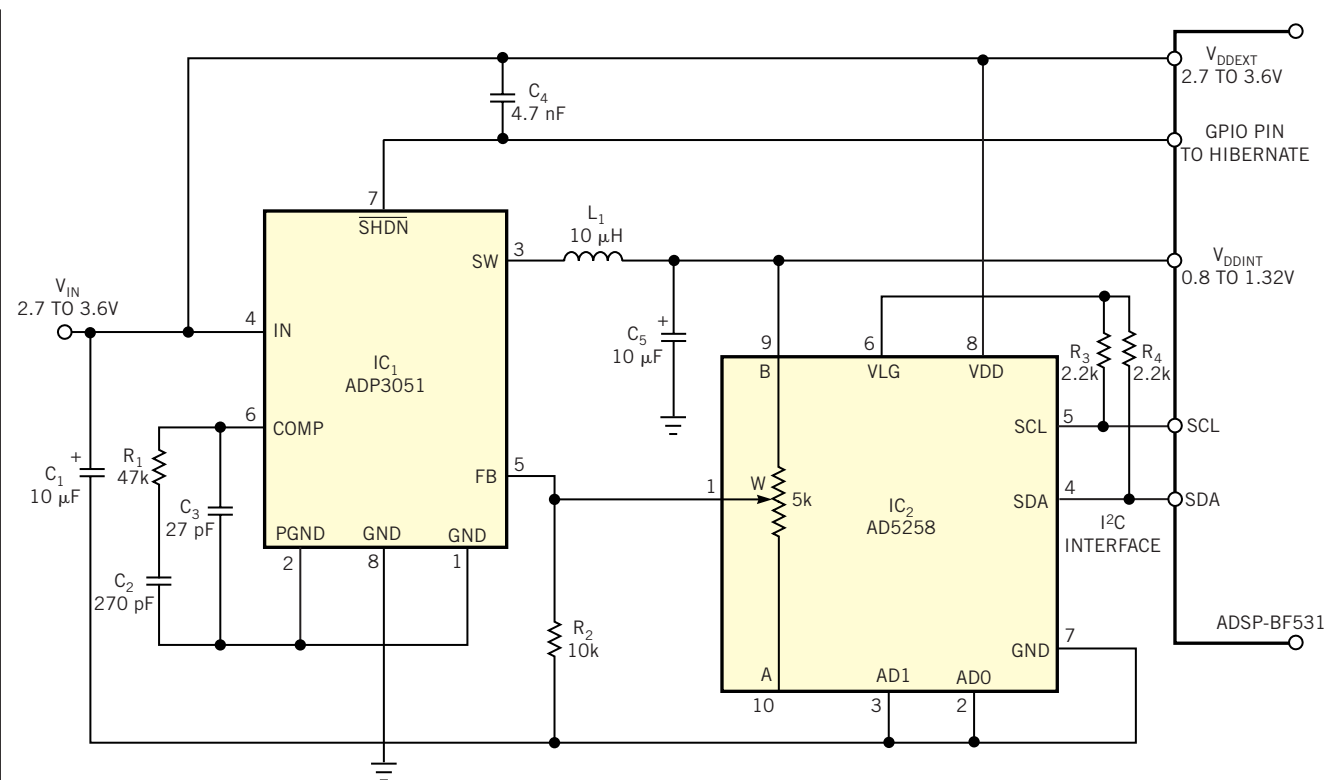


Figure 1 Under control of its host processor, digital potentiometer IC₂ adjusts the processor's core power-supply voltage.

voltage from exceeding 1.2V if a software glitch occurs.

A digital potentiometer typically presents a highly variable absolute resistance value but can accurately set its internal resistance ratio. In this design, the AD5258's internal resistor forms a voltage divider with an external resistor to set the output voltage. To improve the ADP3051's output-voltage accuracy, the ADSP-BF531 uses a simple algorithm to compute and store an appropriate maximum resistance for a given operating voltage in the AD5258's nonvolatile memory via its I²C port.

Using the AD5258 with an external resistor provides hardware protection to prevent the output voltage from going above 1.2V. If the AD5258 is set to zero resistance, the resulting output voltage is $0.8V \times (0\Omega + 10\text{ k}\Omega) / 10\text{ k}\Omega = 0.8V$. If you set it to its maximum output resistance of 5 k Ω , the resulting output voltage is

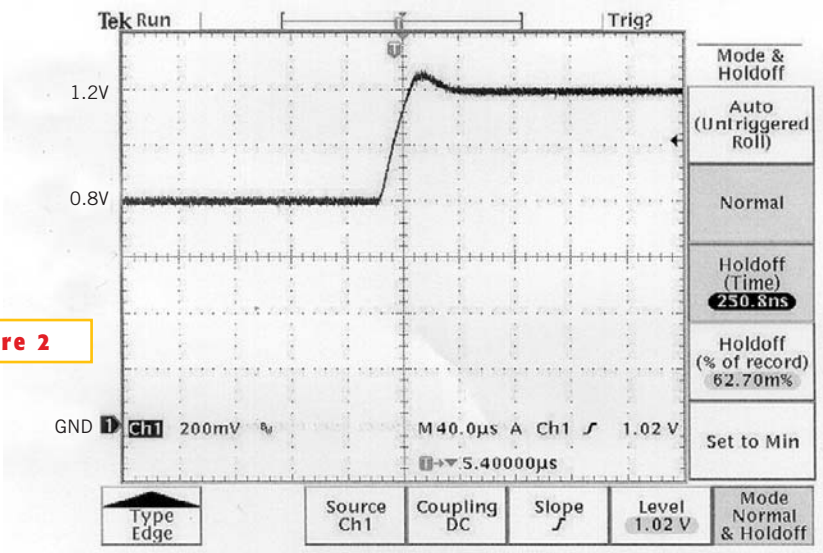


Figure 2

Applying power-supply voltage to the host processor ramps voltage from 0.8 to 1.2V with only 60-mV overshoot.

$0.8V \times (5\text{ k}\Omega + 10\text{ k}\Omega) / 10\text{ k}\Omega = 1.2V$. When the embedded processor directs the AD5258 via its I²C port to ramp the

core voltage from 0.8 to 1.2V, IC₁'s output voltage monotonically increases within 40 µsec (Figure 2). □