

**HIGH-SPEED-MEMORY DESIGNERS CAN ACHIEVE SUPERIOR SIGNAL INTEGRITY AND HIGHER SYSTEM PERFORMANCE BY USING LOW-VOLTAGE, POINT-TO-POINT INTERFACES IN A TERMINATED-TRANSMISSION-LINE ENVIRONMENT.**

# Exploring memory-interface options

IN MANY OF TODAY'S high-performance applications, system memories are the bottlenecks that limit system performance. In the 100- to 225-MHz range, the SRAM I/O-interface options for single-ended signals are HSTL (high-speed transceiver logic) and LVTTTL (low-voltage transistor-to-transistor logic). Beyond 225 MHz, HSTL has become the de-facto-standard I/O interface for synchronous SRAMs. Because faster I/O interfaces significantly improve overall system performance, HSTL is the interface of choice for high-speed-memory applications and is ideal for driving address buses to multiple memory banks.

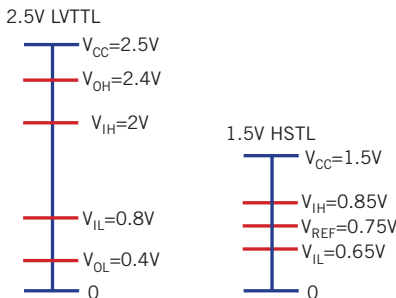
As more applications demand higher bandwidth, designers are developing new SRAM architectures that employ single- or dual-port, double-data-rate and quad-data-rate transfers. For existing SRAM architectures, such as the no-bus-latency and standard synchronous SRAMs, the path to higher performance lies in faster I/O technologies.

LVTTTL is a JEDEC (Joint Electronic De-

vices Engineering Council) standard that references the input signal to ground. The output switching range is 0.4 to 2.4V for 3.3V LVTTTL and 0.4 to 2.2V for 2.5V LVTTTL (Figure 1). Because of the large voltage swing, LVTTTL can experience ground bounce and other signal-integrity issues with wide buses when driving high capacitive loads or when operating at high frequencies.

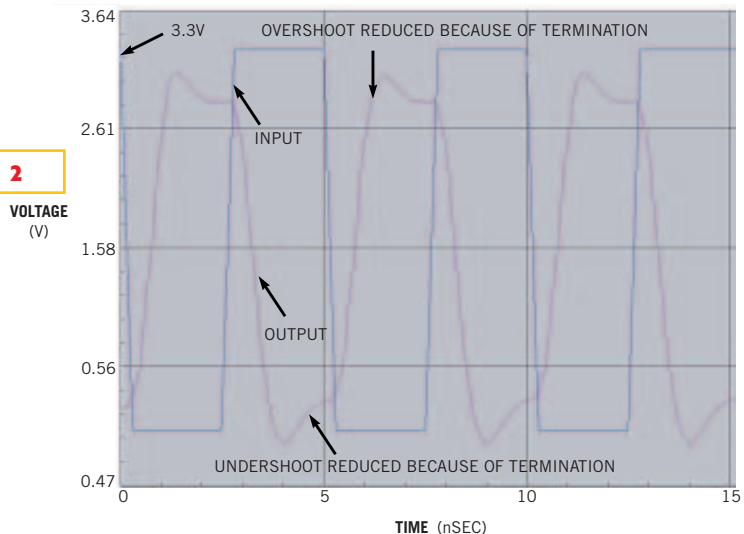
HSTL is a technology-independent interface standard for digital ICs that calibrates the input signal to a reference voltage rather than to ground. This calibration enables a smaller I/O swing and improves performance. HSTL was developed for voltage-scalable and technology-independent I/O structures. The nominal logic-switching range is 0.65 to 0.85V for 1.5V HSTL, resulting in faster outputs with reduced power-dissipation and signal-integrity issues

**Figure 1**

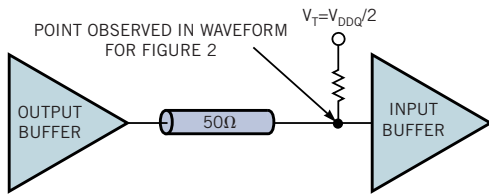


**LVTTTL I/O signals have a much larger voltage swing than do comparable HSTL devices.**

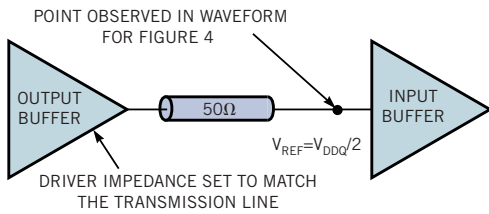
**Figure 2**



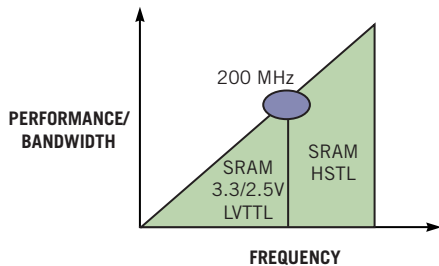
**The standard voltage swing for LVTTTL is around 3.3V.**



**Figure 3** Standard board-level conditions produce the LVTTTL waveform shown in Figure 2.



**Figure 5** These HSTL board-level conditions produce the impedance-matched waveform of Figure 4.



**Figure 6** An unterminated LVTTTL line yields excessive ringing due to impedance mismatches.

(Figure 1). The standard requires I/O structures including differential amplifier inputs and push-pull output buffers using an output power supply that may differ from the operating the device itself. You should tie one input to a user-supplied reference voltage for single-ended signals. There are four classes of HSTL output specifications depending on output-drive requirements. The major difference between the Class I and Class II HSTL outputs is the drive strength (Table 1). Most of the synchronous SRAMs are only HSTL Class I- and HSTL Class II-compatible.

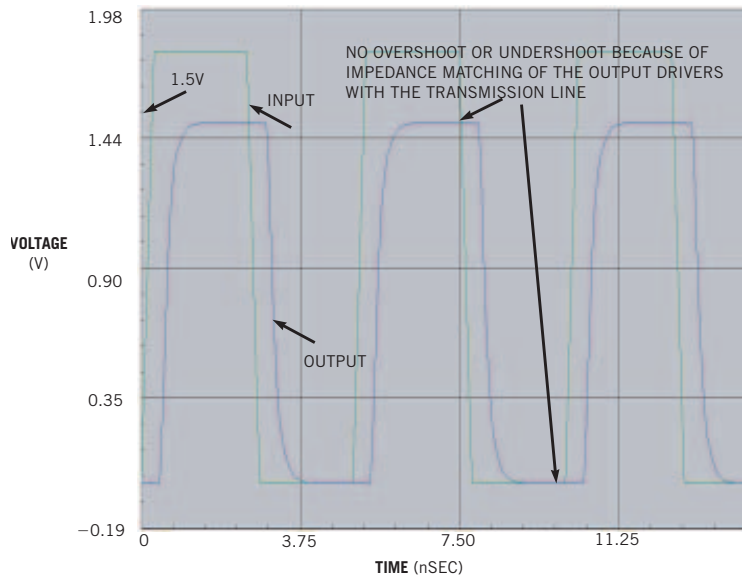
#### TRANSMISSION-LINE PROBLEMS

The limiting factors in any high-speed digital I/O circuit are the typical trans-

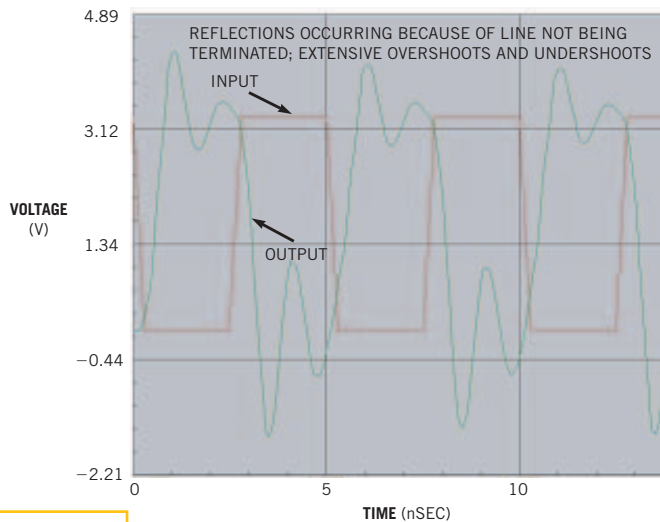
mission-line effects of ringing, reflections, crosstalk, and EMI. Reflections and crosstalk can cause major problems by latching incorrect data at the receiving end. Transmission-line reflections are the greatest constraint, so you should control them with parallel or series impedance-matching terminations.

SRAMs currently offer 3.3 and 2.5V LVTTTL levels for frequencies of 100 to 225 MHz. As networking demands have increased, so has the requirement for

faster high-performance memories. Signal characteristics, power consumption, timing, and signal-integrity parameters all contribute to the limitations or bottlenecks in LVTTTL logic. For example, the large voltage swing in LVTTTL is a major contributor, with measurable effects in power consumption, timing, noise generation, and susceptibility. Referring to figures 2 and 3, the voltage swing for LVTTTL is around 3.3V. By comparison, the voltage swing for HSTL in figures 4



**Figure 4** The voltage swing for HSTL is around 1.5V, assuming an unterminated line and no resistive load.



**Figure 7** An unterminated line results in reflections.

**TABLE 1—MAJOR DIFFERENCES BETWEEN CLASS I AND CLASS II OUTPUTS**

HSTL Class I	HSTL Class II
$V_{OH}(dc)=V_{DDQ}-0.4$	$V_{OH}(dc)=V_{DDQ}-0.4$
$I_{OH} \geq 8 \text{ mA } (V_{TI}=V_{DDQ}/2, R_I=50\Omega)$	$I_{OH} \geq 16 \text{ mA } (V_{TI}=V_{DDQ}/2, R_I=50\Omega)$
$V_{OL}(dc)=0.4$	$V_{OH}(dc)=0.4$
$I_{OI} \geq -8 \text{ mA } (V_{TI}=V_{DDQ}/2, R_I=50\Omega)$	$I_{OH} \geq -16 \text{ mA } (V_{TI}=V_{DDQ}/2, R_I=50\Omega)$

and 5 is around 1.5V, assuming an unterminated line with no resistive load.

The difference in the voltage swing gives HSTL a big advantage and leads to improvements in both power consumption and timing. The lower the voltage swing, the smaller the power required to drive the capacitive load. Keeping this fact in mind, as well as the fact that the LVTTL signal has a voltage-swing requirement that is higher than that of HSTL by a factor of two, HSTL would be a voltage level of choice.

Power =  $0.5 \cdot C_L \cdot V_{OH}^2 \cdot F$ , where  $C_L$  is the capacitive load,  $V_{OH}$  is the output swing voltage, and  $F$  is the frequency of operation. You can see from this equation that the power consumption on the LVTTL I/Os will be four times higher if you keep constant the capacitive load driven and the frequency.

**LOW-VOLTAGE TRANSITIONS**

Similarly, a smaller I/O voltage swing enables faster logic transitions. LVTTL signal transitions would take 3.3 nsec, assuming a signal rise or fall time of 1V/nsec. With HSTL, the signal swing is just 1.5V, enabling it to complete the transition in just 1.5 nsec. These transition times assume full rail-to-rail swings even though the minimum swing requirement is around 1.2V for LVTTL and 0.2V for HSTL.

In addition, high-performance buses require you to account for transmission-line effects to ensure signal integrity. LVTTL, with its large voltage swings, was not designed for high-frequency operation and is susceptible to transmission-line-type problems. HSTL's developers did not design it, on the other hand, for a high-speed transmission-line environment. It requires more design effort, with a reference supply, termination supply, line terminations, and other techniques to ensure signal integrity for high-speed I/O signals.

Some of today's HSTL I/O structures come with a termination for the inputs

and circuitry to match the output impedance of the driver to the transmission line. LVTTL I/O interfaces, on the other hand, require board designers to include additional resistors for proper termination of all lines if they are operating the interfaces at high frequencies. The built-in termination features allow HSTL to provide an easier, more reliable interface with superior signal integrity. The memory-I/O-standard transition takes into account performance and frequency (Figure 6). An unterminated line results in reflections, causing serious signal-integrity problems (Figure 7). Conversely, HSTL's designed-in matching-impedance circuitry helps provide clean signals with no overshoots and undershoots (Figure 4).

To increase system throughput, today's systems require more efficient use of system buses. Architectural changes coupled with the proper I/O interface enable applications using memories to increase the bandwidth and improve signal integrity. It is clear that, at frequencies greater than 200 MHz, HSTL is the I/O interface of choice for synchronous SRAMs. □

**AUTHOR'S BIOGRAPHY**



*Kannan Srinivasagam is a staff application engineer in Cypress Semiconductor's Memory Products Division. His responsibilities include producing reference designs, generating*

*behavioral models of key products, board-level-failure-analysis debugging, and application- system analysis. He joined Cypress in 1999 as a product engineer and has driven product-modeling-process changes. He also has been involved in debugging and qualification projects at major customer sites. Srinivasagam holds a master's degree in electrical engineering (VLSI design) from Arizona State University (Tempe).*