



The perils of input capacitance

IT IS IMPOSSIBLE TO BUILD AN OP AMP without including some input capacitance, and the op amp's pc board adds even more (**Figure 1**). All of the capacitors except for the feedback capacitor, C_F , are stray capacitances, and they influence the circuit's stability. When you set the capacitors to zero, an artificial condition, **Equation 1** gives

the loop gain (**Reference 1**). Op-amp open-loop gain, a , has magnitude and phase components, so it introduces phase shift into the Bode (logarithmic-stability) plot. The critical point on a Bode plot is the point at which the gain magnitude equals zero (gain=1); the difference between 180° and the actual phase shift is the phase margin.

$$A\beta = \frac{aR_G}{R_G + R_F} \quad (1)$$

The external components are resistive, and making $R_G=R_F$ decreases loop gain by 6 dB. This decrease further enhances stability; the vertical intercept on the Bode plot drops 6 dB, but the pole locations stay constant. **Equation 2** gives the loop gain for an inverting amplifier with real input capacitances ($C_F=0$), as **Figure 1** shows.

$$A\beta = \frac{aR_G}{R_G + R_F} \cdot \frac{1}{R_G \parallel [R_F(C_{CM} + C_D) + 1]} \quad (2)$$

The input capacitance adds a pole to loop gain, and when the parallel value of R_G and R_F is small, say 500Ω , the pole location is at $f=16.76$ MHz. The pole introduces essentially zero phase shift at one-tenth of its location frequency, so input capacitance does not affect op amps with a gain bandwidth of less than 1.676

MHz. As the op-amp gain bandwidth increases beyond 1.676 MHz, phase shift from the pole adds to the loop-gain phase shift, and, depending on its phase response, the op amp overshoots, rings, and then oscillates.

Increasing the parallel value of R_G and R_F causes the pole to decrease in frequency ($f=0.1676$ MHz at $R_F \parallel R_G=5$ k Ω); hence, the phase shift occurs sooner, exacerbating the instability problem.

AN ALTERNATIVE OPTION FOR THE INPUT-CAPACITANCE PROBLEM IS TO ADD A FEEDBACK CAPACITOR, C_F .

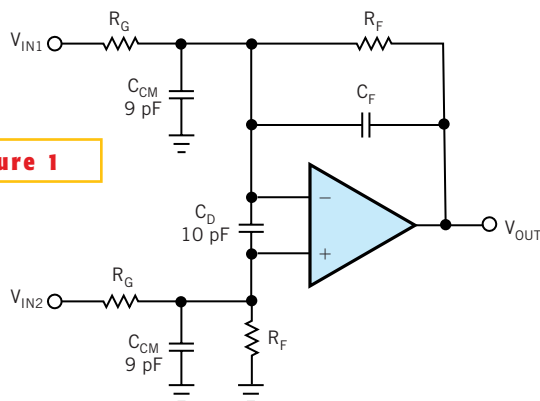
Resistors in high-frequency op-amp circuits traditionally have small values to minimize the effect of stray input capacitance. An alternative option for the input-capacitance problem is to add a feedback capacitor, C_F . **Equation 3** gives the loop gain when the circuit

has input and feedback capacitors.

$$A\beta = \frac{R_G}{R_G + R_F} \cdot \frac{R_F C_F s + 1}{\frac{R_F R_G}{R_G + R_F} ((C_F + C_G) + 1)} \quad (3)$$

The zero in **Equation 3** always precedes the pole; thus, its phase shift cancels some negative phase shift until the pole comes into play. The circuit can be independent of both capacitors by making $R_F C_F = R_G C_G$. Normally, this option is not the best for closed-loop bandwidth performance, so engineers use smaller values of C_F . You can optimize the resistor values, capacitor values, and op-amp bandwidth for the best high-frequency performance, but $2C_F = C_G$ is an excellent starting place for lab experiments.

Figure 1



Stray capacitance on the op-amp-input leads causes a pole in the Bode plot and potential instability.

REFERENCE

1. Mancini, Ron, *Op Amps for Everyone*, Newnes, March 2003.

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