

TABLE 1—LANGUAGE FEATURES

	VHDL 1993	Verilog 1995	SystemC	Verilog 2001	System Verilog 3.1	Verilog 2005	VHDL 200X
Switch-level modeling	X	X		X	X	X	X
ASIC timing	X	X		X	X	X	X
Concurrency	X	X	X	X	X	X	X
Design modularization	X	X	X	X	X	X	X
Gate-level modeling	X	X	X	X	X	X	X
Gate-level timing	X	X	X	X	X	X	X
Four-state logic	X	X	X	X	X	X	X
Event handling	X	X	X	X	X	X	X
Basic data types	X	X	X	X	X	X	X
Basic behavioral constructs	X	X	X	X	X	X	X
Dynamic generation of hardware	X				X	X	X
Configurations	X				X		X
Simple assertions	X				X	X	X
Assertions (formal methods)					X	X	X
Dynamic-memory allocation	X		X		X	X	X
Pointers	X		X		X		X
Multidimensional arrays	X		X	X	X	X	X
Records	X		X		X	X	X
Enumeration	X		X		X		X
Automatic variables	X		X	X	X	X	X
Signed numbers	X		X	X	X	X	X
User-defined logic types	X						X
User-defined resolution functions	X						X
Void type			X		X		
Union	X		X		X		X
Behavioral constructs	X		X		X	X	X
Classes with methods and inheritance			X		X		X
Sequential regular expressions	X	X	X	X	X	X	X
Temporal-property definitions					X	X	X
Scheduling for testbench and assertions					X	X	X
Semaphores	X				X		X
Stimulus generation					X	X	X
Constrained random data generator					X	X	
Coverage monitoring					X	X	X
Strings and strings operations	X				X		X
Standard C interface					X	X	X
Transaction modeling			X			X	X
Module encryption						X	