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AT CLOCK FREQUENCIES GREATER THAN 1 GHz AND INTERCONNECTS LONGER THAN 12 IN., TRANSMISSION-LINE-LOSS EFFECTS DOMINATE SIGNAL INTEGRITY. A FLEXIBLE SIMULATION TOOL HELPS YOU MAKE EARLY TRADE-OFFS TO OPTIMIZE COST AND PERFORMANCE.

What you lose from a lossy line

Electrical engineers are running on Moore's Law's relentless treadmill. Traditionally, Moore's Law says that the number of transistors per chip doubles every 18 months—thanks to advances in photolithography, which allow smaller transistors at higher yields. Its corollary is that the channel length of all gates also decreases. Because the rise time of a gate's transition is proportional to the gate's channel length, rise time, driven by the same forces that drive Moore's Law, decreases with each new generation of chips. New signal-integrity problems arise as rise times decrease, clock frequencies increase, and designs enter new bandwidth regimes. Many high-speed serial links are now entering the realm in which the transmission-line losses affect signal quality. Products may not work if designers fail to anticipate and minimize these effects to optimize each design.

THE PROBLEM WITH LOSSY LINES

An ideal lossless transmission line is the most common interconnect model in virtually all Spice and behavioral-based simulators. Such models describe the line as a characteristic impedance and a time delay and assume that, as the signal propagates down the line, it loses no energy. If a signal with 1V amplitude and 1-nsec rise time enters the line, the same 1V and 1 nsec come out the far end.

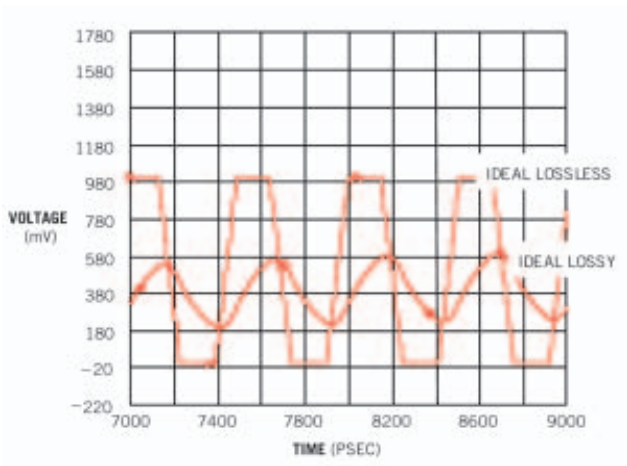

Figure 1 A 100-psec-rise-time, 2-GHz clock signal at the end of a 0.004-in.-wide, 36-in. backplane trace in FR4 material is modeled as an ideal lossless line and as an ideal lossy line (simulated with Mentor Graphics' HyperLynx).

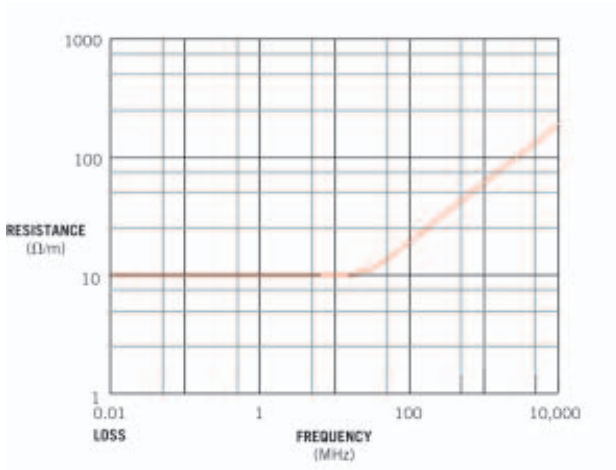

Figure 2 Because of skin-depth effects, the total resistance of a 0.004-in.-wide, 36-in.-long, ½-oz-copper trace increases with increasing frequency (simulated with Mentor Graphics' HyperLynx).

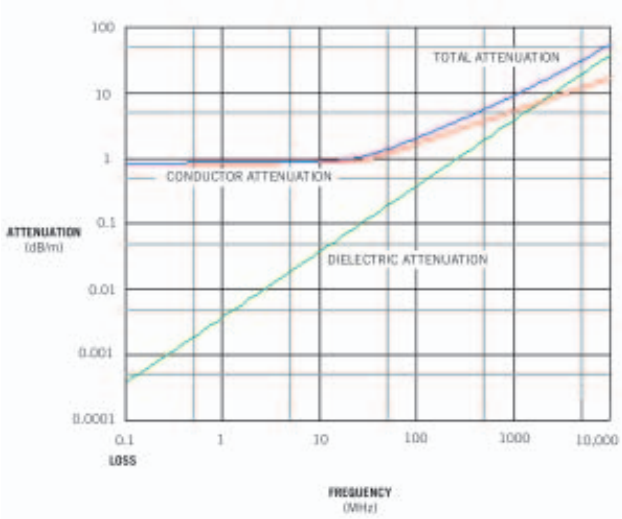

Figure 3 The total attenuation of a 36-in.-long backplane trace is the result of the combined effects of conductor loss and dielectric loss (simulated with Mentor Graphics' HyperLynx).

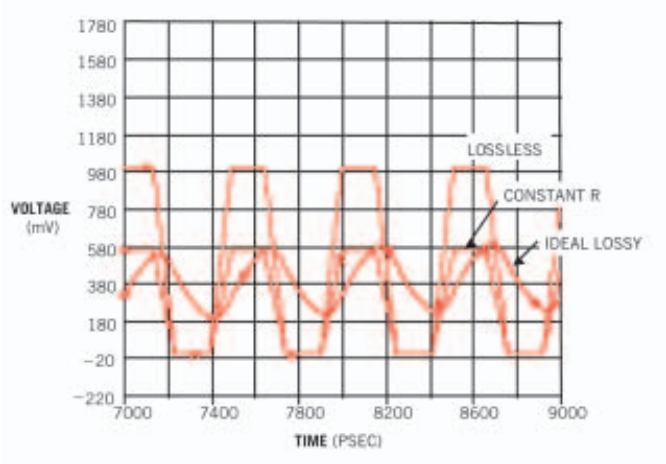

Figure 4 When you compare the response of a lossy model with that of an ideal lossless model in which you attempt to simulate losses by adding a constant 80Ω series resistance, you find that only the lossy model accounts for the rise-time degradation (simulated with Mentor Graphics' HyperLynx).

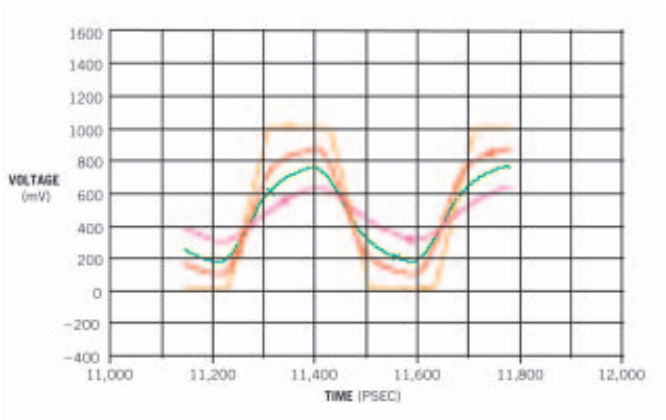

Figure 5 When you compare the rise-time degradation in 0-, 10-, 20-, and 40-in.-long traces, you find that the longer the line, the greater the rise-time degradation (simulated with Mentor Graphics' HyperLynx).

The lossless model closely approximates the behavior of interconnects when signal rise times are on the order of 1 nsec and trace lengths are as great as 10 in. However, as rise times approach 0.1 nsec and lengths approach 36 in., as they do in a backplane, the lossy effects of transmission lines begin to influence signal quality. **Figure 1** shows the simulated received signal on a typical backplane trace ignoring and including the loss effects.

The dominant problem that transmission-line losses create is degraded rise time. The degradation becomes a serious problem when the degraded rise time is comparable to the signal's bit period. Then, the received waveform's precise shape depends on the previous bit pattern, causing ISI (intersymbol interference).

Although you can use rules of thumb to approximate the rise-time degradation, this approach can produce nothing more accurate than a rough estimate. The actual transition waveforms are not even close to a Gaussian shape, which is the basis for describing them with just one "rise-time" number. Realistically, the only way to predict the impact of losses is to use a transient simulator that simulates lossy lines.

WHY IS THERE LOSS?

Describing and accurately predicting the behavior of interconnects requires a new ideal-circuit model. This model must take into account the important mechanisms that absorb energy from the signal: series resistance of the signal and the shunt leakage through the dielectric material. The series resistance of the signal and the return-path conductors increase with the square root of frequency because of skin-depth effects. At higher frequencies, the series resistance increases, as does resistive heating. **Figure 2** shows the simulated series resistance of a 0.004-in.-wide, 50Ω transmission line as a function of frequency.

All insulators have some residual dipoles that can reorient in an external electric field. As these dipoles move back and forth in a signal's ac field, they create an ac leakage current. If the dipoles respond as quickly as the field changes, the changing field's higher frequency components speed the dipoles' back-and-forth movement, increasing the shunt-ac-leakage current through the material.

The amount of leakage current, which converts the dipole motion into heating of the dielectric, depends on the number and size of the dipoles in the material and how far they move in the field. The material's dissipation factor describes this intrinsic, bulk-material property. The larger the dissipation factor, the greater the number of dipoles and the greater the shunt-leakage current.

Even with a constant dissipation factor, the leakage current increases with

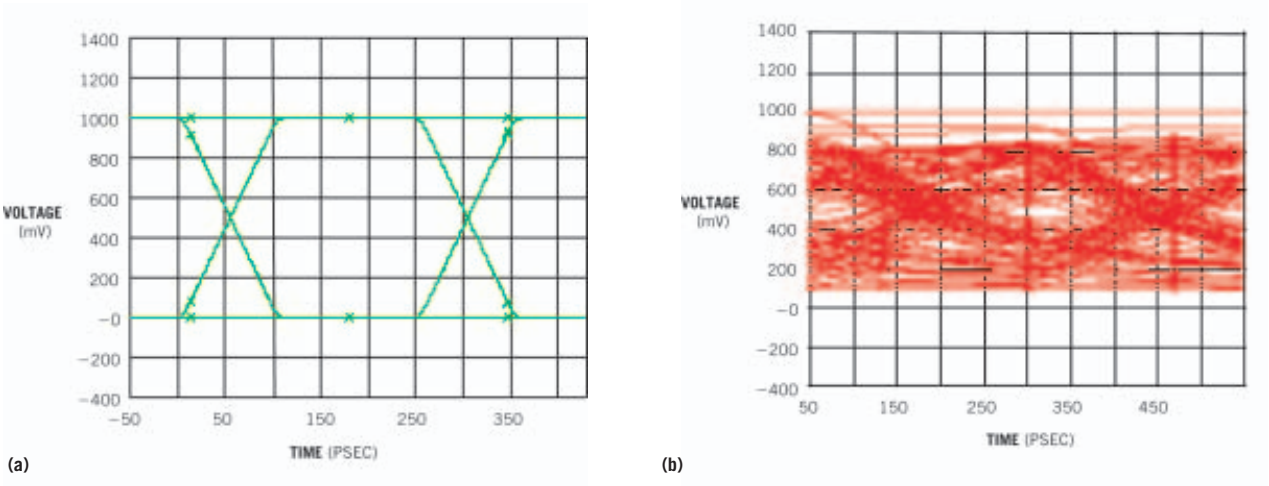

Figure 6 An eye diagram (a) shows a 2-Gbps data stream at its source with no interconnect. A second eye diagram (b) shows the same signal after it has traveled 40 in. through a 0.004-in.-wide FR4 trace. The eye is almost completely closed because of the losses (simulated with Mentor Graphics' HyperLynx).

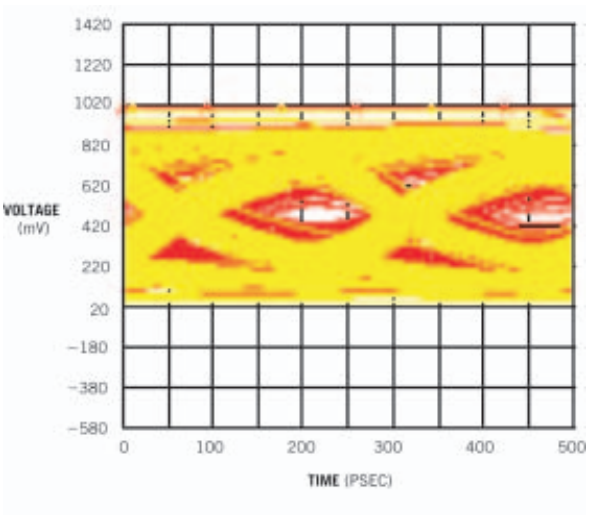

Figure 7 These eye diagrams show 2-Gbps signals that have traveled through 50Ω, 40-in. backplane traces with 0.004-in.- and 0.008-in.-wide lines in FR4 (simulated with Mentor Graphics' HyperLynx).

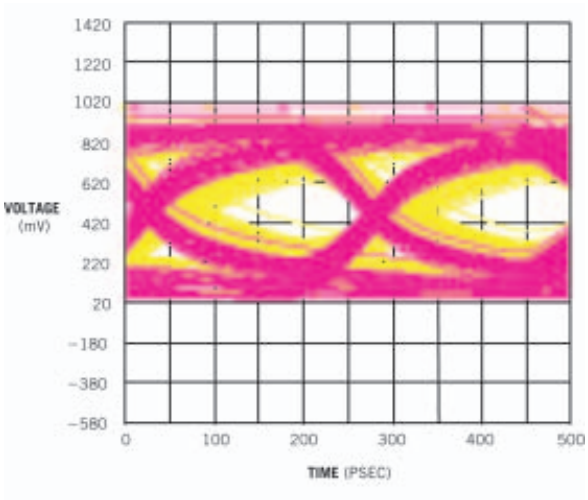

Figure 8 These eye diagrams show signals that have passed through 0.008-in.-wide, 50Ω lines with a dissipation factor of 0.02 in FR4 material and a dissipation factor of 0.004 in GML3000 material (simulated with Mentor Graphics' HyperLynx).

increasing frequency. Therefore, increasing frequency decreases the dielectric's shunt-leakage resistance and increases the material's ac-power consumption. This effect, the dielectric's conductance, is the inverse of its resistance. The power absorbed in the dielectric contributes to signal attenuation and is directly proportional to the dielectric's conductance.

These two sources of loss contribute to frequency-dependent attenuation. **Figure 3** shows the contributions from each term and the total expected attenuation. For a 0.004-in.-wide trace, dielectric loss dominates at sine-wave frequencies higher than about 2 GHz.

SIMULATING LOSSY LINES

If the losses in the line were constant with frequency, every frequency would be attenuated equally, and the spectrum of the signal entering the line would be the same as the spectrum of the signal exiting the line. Though the amplitude of the signal might be reduced, the signal's rise time would be exactly the same coming out as going in.

A simulator that fails to take into account the frequency dependence of the losses is worthless in predicting lossy lines' most important property: rise-time degradation. **Figure 4** shows an example of the simulated signal transmitted through a 36-in. backplane using an ideal lossy-line model and an ideal lossless model but with series resistance that is constant with frequency, corresponding to the resistance of the line at a 2-GHz clock frequency. An accurate transient simulator must take into account the frequency dependence of the losses from

these two sources. This tenet is the basis of the new ideal lossy-line model that Mentor Graphics' HyperLynx uses.

Because the dielectric absorbs higher frequencies more than it does low frequencies, the transmitted signals' bandwidth decreases, and their rise time increases. Longer lines and higher losses lengthen the rise time. **Figure 5** shows the signal transmitted through a typical FR4 backplane over distances of 10, 20, and 40 in. The rise-time degradation exceeds 200 psec for the 40-in. trace.

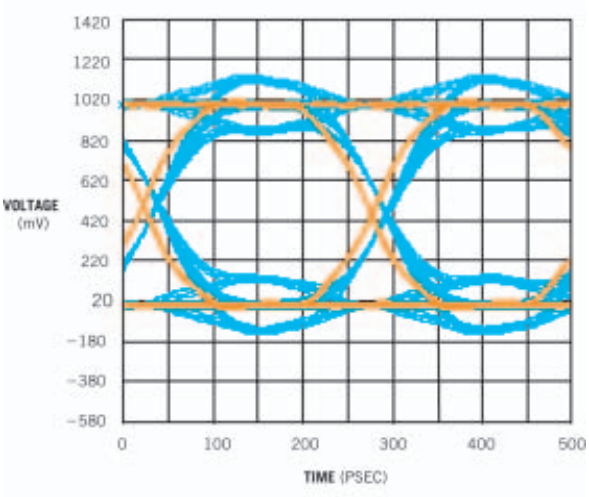

Figure 9 These eye diagrams are for 2-Gbps signals that have traveled through an ideal lossless line with four vias as nominally manufactured and that you could optimize for minimal distortion (simulated with Mentor Graphics' HyperLynx).

LOSSES' IMPACT

When the signal's rise time is comparable with the rise-time degradation, the lossy effects distort the received signal. Initially, this rise-time degradation affects timing. As the rise time further increases and becomes comparable to the bit period, the received bits' voltage waveform depends on the previous bit pattern.

You can evaluate the impact of line loss by using a long bit sequence that contains all possible pattern combinations. To shorten the simulation, the simulator generates a pseudorandom bit pattern and calculates the transmitted pattern through the lossy line. You can see the resulting signal degradation at a glance if you superimpose each successive received bit, synchronized with the generating clock as the trigger. When the voltage levels of each received bit are far enough apart to be distinguished, the resulting pattern looks like an open eye—hence, the name "eye diagram." Rise-time degradation causes the eye to close.

You can use the eye opening to characterize the performance of an interconnect in a high-speed serial link. The opening must be at least as large as the device family's noise margin and the width of the crossovers at the corners of the eye is a measure of the system's deterministic jitter, which you must account for in timing budgets.

An eye diagram shows at a glance whether an interconnect is acceptable. **Figure 6** shows the eye diagram of a signal at the output of a typical high-speed driver. The eye is open, and no ISI exists. However, when the signal propagates down a 40-in.-long, 0.004-in.-wide, 50Ω trace in FR4, the losses degrade the rise time and cause ISI; the eye closes, and jitter increases.

OPENING YOUR EYES

By using a tool that simulates lossy transmission lines and has an integrated 2-D field solver, you can explore three important design characteristics that can dramatically influence the eye opening. These characteristics are the trace width, the dielectric dissipation factor, and the impedance discontinuities from vias.

The trace width affects the series-resistance loss, which increases with the square root of frequency. Obviously, a wider line has less resistive loss and helps open the eye. Unfortunately, increasing

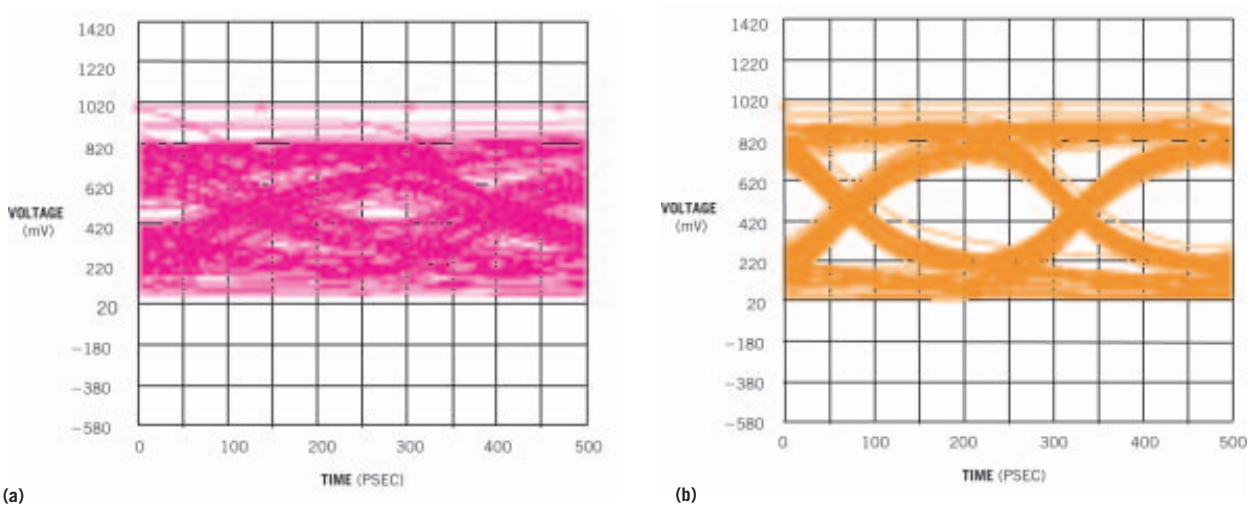

Figure 10 These eye diagrams are for a 0.004-in.-wide, 50Ω backplane trace, before (a) and after (b) optimization. With the correct simulation tool, you can optimize the board design by balancing material cost against other design issues before you commit to hardware fabrication (simulated with Mentor Graphics' HyperLynx).

the line width while maintaining the same target impedance also requires increasing the dielectric thickness and makes the board thicker.

For example, **Figure 7** shows the resulting eye diagrams for traces of two line widths, both designed as 40-in.-long, 50Ω lines in FR4. One has a line width of 0.004 in.; the other has a line width of 0.008 in. Wider lines increase the eye opening.

The laminate material's dissipation factor affects the shunt-conductance loss. A lower dissipation-factor material helps to open the eye. Unfortunately, nothing in life is free. In general, lower loss laminate materials cost more. For this reason, you should evaluate the bang for each buck. For example, **Figure 8** shows the eye diagram for a 0.008-in.-wide, 50Ω, 40-in.-long backplane trace in FR4, which has a dissipation factor of 0.02 and the same geometry using a low-loss material, such as GIL Technologies' (www.gilam.com) GML3000, which has a dissipation factor of 0.004.

Anything that causes the rise time to degrade causes the eye diagram to collapse. In addition to intrinsic losses in the transmission line, another, subtle, via-related factor can strongly influence the collapse of the eye diagram. As a simple rule of thumb, the loop inductance of a signal via and its return path is about 0.5 nH/mm. For a 0.5-mm via, a signal might see about 0.25 nH of loop inductance.

It is not so much the via itself that degrades the rise time; instead, the combination of the capacitance of the capture pad and the via barrel to the reference planes causes the problem. If you design the capture pads and clearance holes for high yields with no concern for electrical properties, the resulting capacitance can be as great as 0.25 pF per via.

The via capacitance acts as an RC filter, and the resistance comes from the line's characteristic impedance. Each via contributes to the rise-time degradation. **Figure 9** shows the impact from just four vias in an ideal lossless line using 0.25 nH and 0.25 pF for the via. The eye is distorted from the delay and impedance discontinuities.

You can dramatically reduce the impact of the vias by engineering the capture pads and clearance holes to balance the via capacitance with the via inductance for a 50Ω line.

SIMULATE...THEN FABRICATE

With a model of an ideal lossy transmission line and a simulation tool that has an integrated 2-D field solver, you can efficiently explore the three dominant features that contribute to eye-diagram collapse. Then, before committing to hardware, you can evaluate the impact of design choices on signal quality and explore your options. **Figure 10** shows the initial performance of a backplane trace compared with the results you might achieve using a better choice of line width, material selection, and via design. Though simulation does not predict the cost of a design change, it can at least point to the potential benefit.□

References

1. Bogatin, Eric, *Signal Integrity—Simplified*, Prentice Hall, NJ, 2003.

2. Additional papers on this and other signal-integrity topics are available for downloading from www.bogent.com and www.mentorg.com.

Authors' biographies

Eric Bogatin is chief technology officer at Synergetix Inc (Kansas City, KS), where he leads the development of higher performance interconnect products, such as surface-mount sockets, contactors, and connectors for high-speed digital, automotive, and medical applications. He has a bachelor's degree in science from the Massachusetts Institute of Technology (Cambridge) and a master's and a doctorate in physics from the University of Arizona (Tucson). His interests include writing popular science and technology articles and writing science fiction.

Gene Garat is technical marketing engineer for Mentor Graphics HyperLynx product line. He works with customers and signal-integrity professionals to solve board-level signal-integrity and EMI problems through the use of Mentor Graphics' simulation tools, such as HyperLynx. He has a bachelor's degree in mechanical engineering from California State Polytechnic University—Pomona. His spare-time interests include playing racquetball, skiing, motorcycle riding, and golfing.