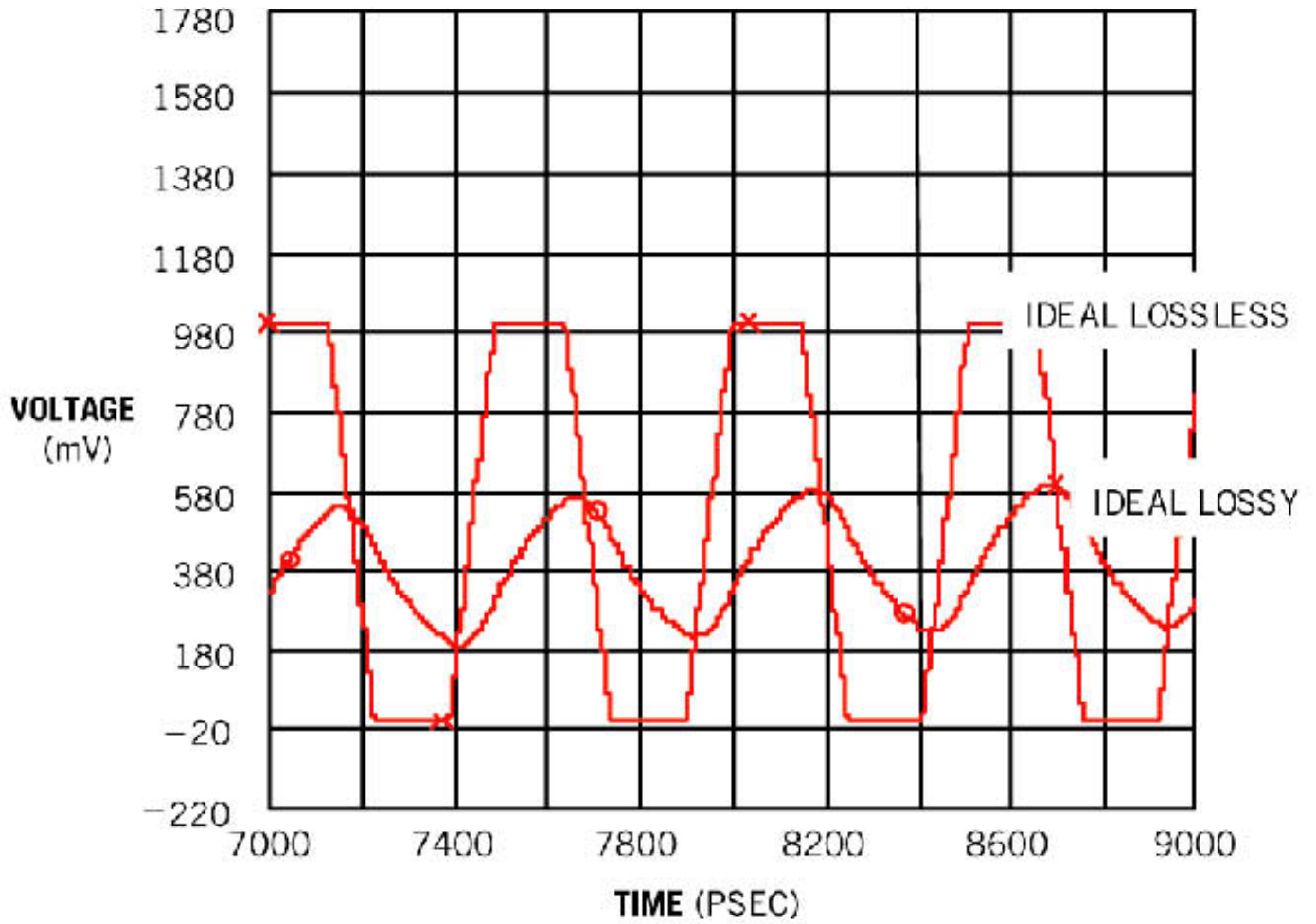


Figure 1



A 100-psec-rise-time, 2-GHz clock signal at the end of a 0.004-in.-wide, 36-in. backplane trace in FR4 material is modeled as an ideal lossless line and as an ideal lossy line (simulated with Mentor Graphics' HyperLynx).