

# leading edge

What's hot  
in the  
design  
community

Edited by  
Fran Granville



## Computerside manner

**"You're walking into a firestorm. Something has broken, and there are possible catastrophic ramifications. If you freak out... It's like a doctor walking into an operating room and saying, 'Oh my God!'"**

**—Ken Smith, co-founder of The Digiticians, a company that makes house calls to homeowners with computer-technology woes, in *The Boston Globe*, March 1, 2004**

## Light guides improve your inner and outer glow

By Bill Schweber

**M**OLDED WHITE-LED LIGHT GUIDES from Global Lighting Technologies provide the backlighting for the full-color, high-resolution displays on 3G cell phones. The MicroLens light

guides feature crisp color and brightness as high as 10,000 nits. You can attach the LEDs directly to a flex circuit and mold them into the backlight; in some cases, with this approach, you can use fewer white LEDs, thus cutting power, cost, and size.

The light guides are available in a variety of thicknesses to as little as 0.65 mm. The

vendor claims that the technology these devices use differs from that for chemical, laser-etch, or V-groove designs. The company says it thus has full control of the light guides' size, shape, depth, pitch, density, and angle of rotation. Prices depend on the parameters you specify but range from 95 cents to \$1.25 (OEM quantities) for a light



**Get the backlighting you need with less LED sourcing, using the MicroLens light guide for 3G-cell-phone-display resolution and color.**

guide with a back reflector, a frame, brightness-enhancement films, a diffuser, and a mask.

► **Global Lighting Technologies**, 1-440-922-4584, [www.glthome.com](http://www.glthome.com).

## Matched MOSFETs provide in-circuit trim

DESPITE HYPERINTEGRATION and systems on chips, many designs require bits of glue logic to complete or customize an interface. Similarly, many linear circuits use discrete transistors to implement or optimize functions, particularly within or near I/Os. Well-matched transistor pairs and quads, among the most common tools in the analog-IC designer's kit, are particularly handy for making simple and scaled current mirrors, cascodes, and discrete differential stages.

The ALD1121E and ALD1123E from Advanced Linear Devices are matched dual and quad N-channel MOSFETs, respectively, available in plastic SOIC and plastic or ceramic DIP packages. The matched MOSFETs provide for postpackage trimming, which allows



**The ALD1121E and ALD1123E matched MOSFETs provide for postpackage trimming.**

the manufacturer to dial out offsets resulting from package-induced die stress. You can trim the threshold voltage, initially  $1V \pm 10$  mV, upward to 3V in 100- $\mu$ V steps as a no-moving-parts in-circuit trim. The device's maximum long-term drift is 50  $\mu$ V in 1000 hours; typical 10-year drift is less than 2 mV.

If you use the part as the manufacturer trims it, the maximum offset is 5 mV. The on-resistance, typically 500 $\Omega$  with gate-to-source voltage 4V over the threshold, matches from device to device within a pair to 0.5%. Prices start at 75 cents (1000).—by Joshua Israelsohn

► **Advanced Linear Devices**, 1-408-747-1155, [www.aldinc.com](http://www.aldinc.com).

## Customize your scope's user interface

**T**ODAY'S DIGITAL SCOPES are replete with features. Although the myriad features add to the instruments' utility, most users take advantage of only about 20% of the capabilities. Yet, each engineer seems to want a different feature set.

This situation poses a dilemma for scope manufacturers: how to provide an array of capabilities that appeals to occasional users and power users alike without making the instruments so difficult to operate that everyone becomes dissatisfied. Tektronix believes it has the answer: Build into the scope an intuitive, graphical application

called MyScope, which enables each user to customize the interface. Removing access to unwanted features shortens the menus and makes navigation easier and more intuitive.

On the new TDS 5000B series, the scopes' 80-Gbyte hard disks store the interface-definition files so that anyone who uses one of the instru-

ments can select the interface most appropriate to the job at hand. Don't worry about colleagues' modifying your favorite interface; you can copy its definition file to a removable USB flash disk or a floppy disk and thus keep the file safe from unwanted "improvements."

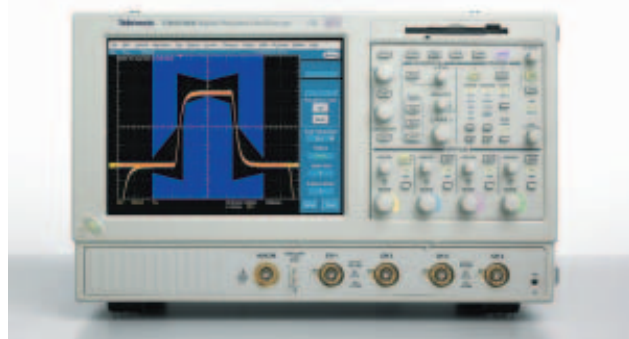
Besides MyScope, the TDS 5000B series includes many enhancements that were extra-cost options on earlier TDS 5000 units. For example, the now-standard memory depth of 2M samples/channel used to cost \$5145. On four-channel units, the memory depth becomes 4M samples/active channel when you use two channels and 8M samples in the single-channel mode. You can also purchase an option that doubles these memory depths. The now-standard advanced-analysis software used to cost \$1025; a CD-RW drive used to add \$405, as did extra processor memory.

Most TDS 5000B scopes have four channels, although the series includes two two-channel models. Bandwidths range from 350 MHz to 1 GHz, and all models but one can simultaneously take 5G samples/sec on all channels. One model has a maximum

acquisition rate of 1G sample/sec to comply with US-export restrictions on scopes that sample at higher rates. Prices range from \$7300 to \$15,990. All models incorporate Tek's DPO (digital-phosphor oscilloscope) technology, which enables the capture of 100,000 waveforms/sec.

—by Dan Strassberg

► **Tektronix Inc**, 1-800-426-2200, [www.tektronix.com](http://www.tektronix.com).



The midrange TDS 5000B family of digital scopes makes standard many features that were extra-cost options in previous versions. The new family bundles the MyScope application, which enables users to customize the instruments' graphical interface.

## DILBERT *By Scott Adams*



► Revenues for microfluidics should grow at a compound-annual-growth rate of 10.3%, from nearly \$1.7 billion in 2003, to more than \$2.7 billion in 2008, according to InStat/MDR.

### EMI FILTER PASSES ONLY GOOD VIBRATIONS

The KNA21 Series of EMI filters from AVX/Kyocera lets you suppress the noise that high-speed digital lines generate. You can tuck these multilayer, 2×1.25×0.85-mm devices into tight spaces, such as cell phones, and keep RF noise from LCD and camera lines from the sensitive RF section, for example.

Depending on model, these devices protect as many as four lines. The filters provide cutoff frequency of 400 MHz and attenuation range of 800 to 2500 MHz at 15 dB and 800 to 1000 MHz at 20 dB. Prices for this EMI filter start at 30 cents (production quantities).—by Bill Schweber

► **AVX Corp**, [www.avxcorp.com](http://www.avxcorp.com).



Keep that digital noise away from sensitive RF areas with the KNA21 series of multi-layer EMI filters.

## ZigBee radio goes IP

JENNIC HAS ANNOUNCED the availability of a suite of IP (intellectual-property) cores for ZigBee ([www.zigbee.org](http://www.zigbee.org)) wireless applications. The ZigBee Alliance, an association of companies working toward standardization of wireless-net-

work monitoring and control products, based the PHY (physical) and MAC (media-access-control) layers on the IEEE 802.15.4 wireless-personal-area-network standard. The suite includes a 2.4-GHz IEEE 802.15.4-compliant radio in 0.18-micron RF CMOS, an O-QPSK (quadrature-phase-shift-keying) modem, a baseband controller,

and a MAC-protocol stack, which companies can combine with their own IP.

The radio has a resistive, differential RF port, an integrated transmitter/receiver switch, a VCO (voltage-controlled oscillator), channel filters, and on-chip auto calibration and requires no external matching components. Current consumption

is less than 35 mA for receiving and 30 mA for transmitting; transmitting power is 1dBm, and sensitivity is -93 dBm. The modem converts 4-bit baseband symbols at 250 kbps to one of 16 quasi-orthogonal 32-bit codes for an air-chip rate of 2 million chips/sec.

The baseband controller provides hardware acceleration of several lower layer MAC functions to reduce processor overhead, including superframe and protocol timers, autoacknowledgment with retries, and CSMA/CA (carrier-sense-multiple-access/collision-avoidance) access, as well as a hardware AES (Advanced Encryption Stan-

dard) block. The protocol stack has a service-access-point interface; provides a simplified, C-callable API; and supports multiple configurations for reduced- to full-function applications. A single-chip design integrating the suite with an onboard processor, memory, and I/O systems is suitable for implementation in an 8×8-mm, 56-lead QFN package. For more technical information on IEEE 802.15.4 and ZigBee, visit the ZigBee Alliance Web Site or [www.ieee802.org/15/pub/TG4.html](http://www.ieee802.org/15/pub/TG4.html).

—by Nicholas Cravotta

►Jennic, +0114 281 2655, [www.jennic.com](http://www.jennic.com).

## Optical/electrical jitter analyzer guarantees peak-to-peak errors of less than 0.02 unit intervals

ANRITSU HAS ADDED a \$20,000 MP1590A-30 high-precision jitter-analysis option to its \$57,285-base-price MP1590A network-performance tester. The company says this option makes the tester the first instrument whose internal jitter—less than 0.02 unit intervals p-p—permits accurate measurements of the small amounts of jitter permitted under ITU (International Telecommunications Union) ultra-high-speed-communications-link specifications. Most of the links are optical, but some send electrical signals over rather long copper paths.

Low jitter isn't essential merely to please the ITU; multigigabit-per-second data streams need low jitter to keep error rates acceptably low. Without instruments that could produce and accurately measure multigigabit-per-second signals having jitter as low as 5-psec p-p, network-equipment manufacturers were flying blind; when they used different vendors' instruments to make equivalent

measurements, the results could differ by factors as large as three.

The manufacturer believes that the MP1590A/MP1590A-30 will become the gold standard for verifying specification compliance in multigigabit-per-second optical-networking equipment. Anritsu calls the combo the only test instrument that supports the phase-analysis method recommended in the revised ITU-T draft specification 0.172 (2003.11), whose adoption is expected this month.

Adding to the instrument's accuracy and repeatability, a golden transmitter guarantees the jitter that the tester's transmitter generates. You can use the golden transmitter as a reference for calibrating jitter testers because its jitter is known, is primarily deterministic (exceeding rms random jitter by almost two orders of magnitude), and exhibits low optical-power dependence from -8 to -14 dBm.—by Dan Strassberg

►Anritsu Co, 1-800-267-4878, 1-972-644-1777, [www.us.anritsu.com](http://www.us.anritsu.com).



**The MP1590A network-performance tester uses a 6U CompactPCI architecture. When outfitted with the MP1590A-30 high-precision jitter-analysis option, it is, according to its manufacturer, the only test instrument that supports the phase-analysis method recommended in the revised ITU-T draft specification 0.172 (2003.11).**

►IDC predicts that sales of digital radios will increase from 142,000 this year to 2 million in 2007, representing an increase in sales, including installation fees, from \$78 million to \$558 million.

## 10-Gigabit PHY devices hit new low

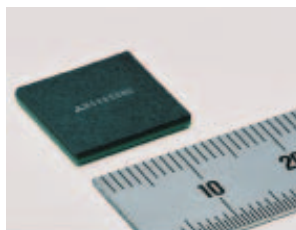
BOTH **QUAKE** Technologies and **Mitsubishi** have announced 10-Gbps PHY (physical-layer) devices. Quake's third-generation, 10-Gbps QT2022 serial-to-XAUI (10-Gigabit-attachment-unit-interface) device consumes less than 900 mW and targets applications such as 10-Gigabit Ethernet and 10-Gigabit Fibre Channel, especially those in which the 10-Gbps PHY device is migrating from a Xenpak, Xpak, or X2 module onto a system-card or mezzanine module.

The bidirectional QT2022 integrates the PMA (physical-media-attachment), PCS (physical-coding-sublayer), and XGXS (10-Gigabit-extension-sublayer) layers onto a single chip and converts four 3.125-Gbps XAUI lanes into a serial 10.3- to 10.57-Gbps data stream. This stream complies with XFI (10-Gigabit small-form-factor-interface) requirements, enabling you to connect it to an electro-optical interface or XFP (10-Gigabit small-form-factor-pluggable) module. Other features include electronic-dispersion-compensation cir-

cuitry, an integrated postamplifier with 10-mV p-p sensitivity per side, a built-in receiver equalizer running across 12 in. of FR4 pc board, an adjustable output amplitude on XAUI and serial interfaces, a JTAG interface, a standard MDIO/MDC (management-data I/O/management-data clock), and a two-wire interface with a non-volatile-register set.

The QT2022 complies with IEEE 802.3ae-2003 10GE and INCITS (International Committee for Information Technology Standards) T11 and 10-GFC (Gigabit Fibre Channel) standards and Xenpak, Xpak/X2, and XFP multi-source agreements. The QT2022 has less than 0.7 psec of rms jitter generation and includes a full suite of built-in test features, including jitter-pattern and pseudorandom-bit-sequence generators and checkers to speed development and volume-production bottlenecks by removing the need for expensive test equipment.

Running on a 1.2V supply, manufactured in a CMOS process, and available in a 12×12-mm PBGA with 1-



The M69850AWG from Mitsubishi for 10-Gigabit modules consumes only 1.2W of power (left). The QT2022 10-Gbps PHY device from Quake consumes less than 900 mW (right).



mm ball pitch, the QT2022 is available for sampling now at \$200 (sample quantities). A complete evaluation kit and an XFP-based reference board are available upon request.

Mitsubishi has also introduced a low-power, single-chip, 10-Gigabit Ethernet PHY transceiver, the M69850 AWG, consuming 1.2W for backbone fiber-optic networks, MANs (metropolitan-area networks), and LANs. The device also integrates PMA, PCS (personal communications systems), and XGXS functions and is manufactured using a 100-nm-gate-width SOI (silicon-on-insulator) CMOS process, enabling high noise immunity and a latch-up-free device. Target-

ing 10-Gbps Xenpak-, Xpak-, and X2-transceiver modules and 10-Gigabit XFP platforms, the M69850AWG complies with the latest 10-Gigabit Ethernet, 10-Gigabit Fibre Channel, and Xenpak multi-source-agreement standard requirements.

Available in a high-performance 14×14×1.7-mm BGA package conforming to X2 and Xpak space and heat requirements, the M69850-AWG is available for sampling at \$330 (sample quantities).

—by Nicholas Cravotta

► **Mitsubishi Electric and Electronics Inc USA**, [www.mitsubishichips.com](http://www.mitsubishichips.com).  
► **Quake Technologies Inc**, 1-613-270-8113, [www.quaketech.com](http://www.quaketech.com).

## Embedded encoder compresses real-time streams

**PARVUS CORP** recently unveiled the MPEG104, a PC/104-Plus form-factor encoder that captures high-quality analog-video and audio streams, encoding them in compressed MPEG-1, M-JPEG, or JPEG formats, and sending them to a host computer over a 32-bit PCI bus. The module supports as many as four composite-video inputs and one stereo-audio input at full NTSC or PAL frame rates. The card also integrates four reprogrammable, general-purpose, digital-I/O channels for system control, as well as a 2-Mbyte SDRAM frame buffer for storing single frames or snapshots of incoming video.

It encodes pictures at both QSIF (quarter-source-input format) and SIF resolutions at up to 30 frames/sec and supports single-frame sizes as large as 720×576 pixels. The MPEG104 fits live-video-encoding applications, such as remote-surveillance systems, video recorders, video servers, external MPEG-1-encoding boxes, motion detection, and traffic monitoring. The MPEG104 is in stock and sells for \$226 (100).—by Warren Webb

► **Parvus Corp**, 1-801-483-1533, [www.parvus.com](http://www.parvus.com).



The MPEG104 PC/104-Plus MPEG-1 encoder provides real-time video compression despite rugged environmental conditions or space limitations.

## Small-footprint, moderate-price scopes provide big picture

LECROY unabashedly proclaims that its new WaveSurfer series of digital scopes targets Tektronix's (www.tektronix.com) market-leading TDS3000 family. The TDS 3000s have won the hearts of many users who need compact, moderately priced scopes but who don't need and usually don't want the complexity of advanced waveform analysis. One of the Tek family's big attractions is the small footprint the lunchbox-sized units occupy on crowded lab benches.

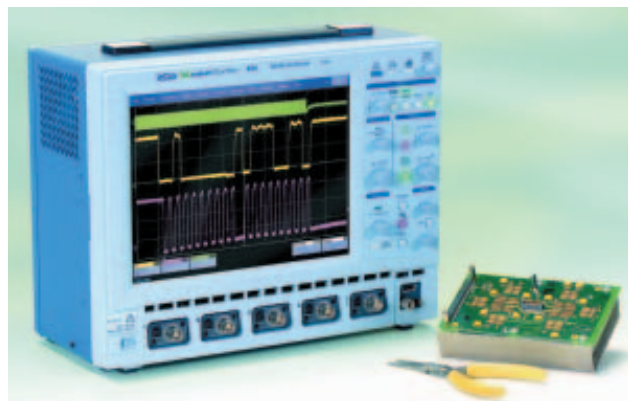
tween the scope families, another physical difference is particularly noteworthy: The WaveSurfer's case lets you attach the scope to either of two optional stands with articulated arms. One stand clamps to the edge of your work surface occupying only a few square inches but enabling you to position the scope close to your eyes and above everything on the bench, providing a true close-up view of waveform details.

A nontechnical issue guided the user-interface design.

no small feat for a product that offers such a wide array of features.

A key to simplifying the user interface was to make the big LCD touch-sensitive, although you can use a USB mouse if you prefer. Zooming in on a waveform area of interest involves nothing more than touching one corner of the area and swiping your finger to the opposite corner. When you remove your hand from the screen, the scope highlights the area you defined and automatically displays a magnified view. Despite the simple user interface, the WaveSurfers are Windows XP-based and incorporate internal hard drives. They run the full spectrum of Windows applications and incorporate multiple USB ports, enabling the use of USB printers and, for removable storage, USB CD/RW and flash drives.

Another difference between the WaveSurfers and the TDS3000s is the WaveSurfers' deep memory—optionally 2M points/channel (500k points standard) when you use no more than half of the channels—versus 10k points/channel for the TDS3000s. The WaveSurfer family comprises six models—two- and four-channel units with bandwidths of 200, 350, and 500 MHz. All units have a maximum sampling rate of 2G samples/sec with no more than half the channels in use. Base prices range from \$4190 to \$8490.—by Dan Strassberg  
► **LeCroy Corp**, 1-800-453-2769, www.lecroy.com.



**Despite a 10.4-in.-diagonal SVGA color display, Windows-XP-based WaveSurfer scopes occupy just about the same bench area as competitive scopes whose displays' area is less than 38% as large. For attachment of peripherals, including printers and storage devices, the units include three USB ports, one of which is on the front.**

LeCroy designed the WaveSurfers to use approximately the same bench area, yet, thanks to a significantly taller case, incorporated a 10.4-in.-diagonal SVGA LCD whose area is 2.64 times as great as the TDS3000s' lower resolution 6.4-in. displays. Although the huge display is but one of many differences be-

Like Tektronix with the TDS 3000s, LeCroy will sell the WaveSurfers through distributors—a first for the company, which employs a direct sales force to sell its higher priced products. Without the customer support that such a sales force can provide, however, instrument operation had to be self-explanatory—

### FREE DOWNLOAD SOLVES START-UP SHORTCOMING

Many of you have developed software for Microsoft's Pocket PC 2000/2002 and Windows Mobile 2003 operating systems or for the Windows CE operating-system versions from which Microsoft derived them. And those who have done so may have struggled with the O/S's 32-process limitation. XDA II Pocket PC Phone devices, for example, automatically launch 28 processes referenced in the start-up folder after a soft reset, thus leaving users with only four possibilities for new processes and, therefore, a limited number of programs they can concurrently run in the background.

To address that problem, Windows Mobile 2003 provides a mechanism in the services.exe directory that optionally allows Pocket PC developers to define their background applications as separate threads of one process (see [http://msdn.microsoft.com/library/default.asp?url=/library/en-us/dnppc2k3/html/ppc\\_services.asp](http://msdn.microsoft.com/library/default.asp?url=/library/en-us/dnppc2k3/html/ppc_services.asp)). Unfortunately, Pocket PC 2000 and 2002 until now lacked services.exe.

Spb Software House has developed a version of services.exe for these operating systems, and the company is offering it free. For more information on how to download and integrate Spb's services.exe with your application, see [www.pocketpcdn.com/articles/services.html](http://www.pocketpcdn.com/articles/services.html).

—by Brian Dipert

► **Spb Software House**, +7 812 324-4944, [www.softspb.com](http://www.softspb.com).

► **IDC projects digital-home-radio sales to grow from 55,000 this year to 2.3 million in 2007, representing an increase in sales from \$26 million to \$570 million.**

# FPGA adopts a revolutionary stance

**D**ARWIN FIGURED OUT that measured evolutionary steps, not abrupt revolutionary leaps, are the preferred way of the world. In your engineering-problem-solving approaches, many of you have figured it out, too. Sometimes, though, the rules of the game change, and continued evolutionary investment leads to diminishing returns; those situations require a revolutionary alternative. Xilinx ([www.xilinx.com](http://www.xilinx.com)), for example, doubled the number of four-input LUTs (look-up tables) and registers in each configurable-logic cell, or “slice,” when moving from XC4000 to Virtex FPGAs and again from Virtex to Virtex-II.

Altera has historically made comparatively minor enhancements to its own LAB (logic-array block), containing eight to 10 LE (logic-element) pairings of a four-input LUT and register, beginning with its first-generation 1992 Flex 8000 family and extending all the way through 2002’s Stratix devices (see “Congratulations to EDN’s Innovation 2002 winners,” *EDN*, May 1, 2003, pg 22). Now, however,

the company has taken the revolutionary plunge and created an ALM (adaptive-logic module) for the Stratix II family. Altera’s past logic-block conservatism had merits; fundamentally, it gave front-end synthesis and back-end placement-and-routing software a consistent, predictable silicon platform on which to perform and perfect its compilation magic.

Using a coarser grained logic element, however, also has advantages, especially in the modern era of perpetually leaky smaller-than-100-nm transistors. Increasing the amount of fast, silicon-efficient intralogic-block routing *potentially* reduces the necessity for comparatively costly and slow interblock-routing resources, along with the power-consuming configuration bits for that routing. The larger the fundamental logic block, though, the greater the importance that your design software make optimal use of that logic block’s attributes—both its internal resources and its available inputs and outputs. Otherwise, expensive silicon goes to waste.

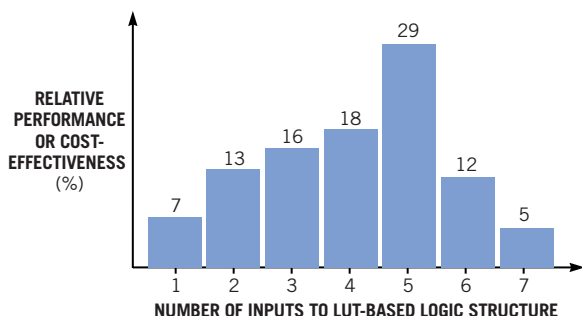
Peer inside a Stratix II ALM and you’ll find a collection of logic functions: two four-input LUTs, a three-input LUT, two registers and two three-input adders, for example. In striving to assist design software in making efficient use of the ALM, Altera has built it in such a way that its triple-LUT structure can implement a diversity of functions. Also, with efficiency aspirations in mind, Altera has doubled the number of inputs to and outputs from each ALM compared with the LE predecessor. Eight ALMs combine to form each LAB. Curiously, competitor Xilinx dropped the three-input LUT from its logic block as part of the several-year-old XC4000-to-Virtex transition, citing synthesis tools’ dearth of use for them. Altera claims that it has resolved this issue, however, in part because the HDL-friendly three-input LUT in Stratix II’s approach resides ahead of the four-input LUTs, not after them as in the past Xilinx implementation.

You won’t unfortunately be able to test Altera’s hypothesis on real chips until next quarter when the first Stratix

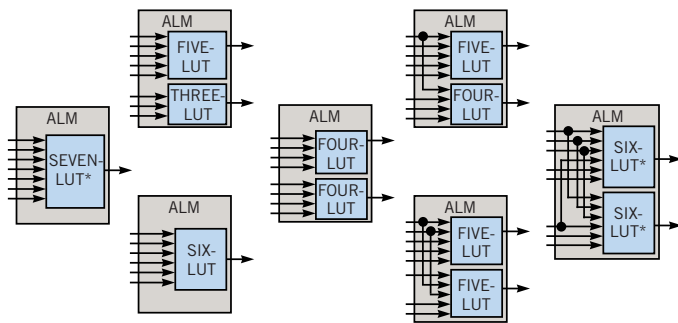
II customer samples are scheduled to begin rolling off partner TSMC’s ([www.tsmc.com](http://www.tsmc.com)) production lines based on a 90-nm, low-K, copper process. Altera’s latest generation Version 4 Quartus II design software offers preliminary device support, however, so you can now begin your development. Due to appear first, the EP2S60 (\$125, 25,000, end of 2004) contains 24,176 ALMs, 2.5 Mbits of SRAM, 144 18×18-bit multipliers, and 12 PLLs. The family of six Stratix II devices, when all members are available for sampling by year-end (with subsequent production, along with HardCopy variants, scheduled for the first half of 2005) will range from 6240 to 71,760 ALMs and contain as much as 9.3 Mbits of SRAM. All Stratix II chips also support nonvolatile, 128-bit AES security for their links to external configuration memories, along with 1-Gbps differential source-synchronous signaling and dynamic phase alignment.

—by Brian Dipert

►Altera, 1-408-544-7000, [www.altera.com](http://www.altera.com).



NOTE: ANALYSIS PERFORMED ON SUITE OF MORE THAN 150 HIGH-DENSITY CUSTOMER DESIGNS.



\*STRATIX II ALM CAN IMPLEMENT A SUBSET OF THESE FUNCTIONS.

(a) An awareness that real-life designs optimally map to a diversity of LUT structures (a) led to Stratix II’s adaptable logic element (b), which Altera believes delivers higher performance and silicon efficiency, along with lower power consumption, than what a straightforward lithography reduction of Stratix would have supplied.

# À la carte intermediate bus power

By Graham Prophet

**W**ITH ITS BCM (Bus Converter Module) concept, Vicor is proposing a modification to the power-distribution architecture usually referred to as IBA (Intermediate Bus Architecture). In IBA, you use the standard (nominally 48V) “telecom” power bus for distribution around the card cages of circuit boards. At board level, you carry out dc/dc conversion, with isolation, down to an intermediate level, usually 12V; then, at point of load, you dc/dc convert again to the final circuit voltage with multiple nonisolated converters. The problem Vicor identifies is that 12V is increasingly a less-than-ideal compromise. If you have a high power system, you can still be routing uncomfortably high currents to circuit boards; if you have heavy loads at today’s processor core volt-

ages (1 to 2V), then 12V is too far away from the final voltage for efficient conversion.

The solution? Choose the intermediate voltage to suit the system. Vicor bases its proposal on a conversion topology called an SAC (Sine Amplitude Converter), a fixed-frequency resonant converter switching at 3.5 MHz. It uses zero-voltage switching on the primary switches and both zero-voltage and -cur-

rent switching on the output synchronous rectifiers. Using a low-Q, low-profile transformer, Vicor says it achieves greater than 1-kW/in.<sup>3</sup> power density and 97% efficiency, with additional gains in noise and speed of response. Vicor’s V·I modules, which the company in turn builds into its BCMs, use this technique; you get 300W from a 32×21×6-mm package. From a 38 to 55V-dc input, you can generate an intermediate bus of 3, 4, 6, 8, 9.6, 16, 24 or 48V, according to your power-load needs. Final regulation will be with an ni-POL (nonisolated point-of-load) converter, as before. You can get 600W from a module using two such converters that still occupies the outline of a standard quarter-brick format.

—by Graham Prophet

► **Vicor**, +44 1276 678222, [www.vicr.com](http://www.vicr.com).



**You can build very-low-profile distributed power with the BCMs, which measure 6 mm high, or just 4 mm if their transformer is set into the pc board.**

## Restructure the costs of IP-based design

MUNICH-BASED MIXED-SIGNAL-IP (intellectual-property) provider Xignal is proposing a new business model, called VIC (Virtual IC), to companies with product ideas that require complex ASICs. With VIC, instead of providing its IP for a conventional licence-fee/royalty payment, Xignal aims to become involved in product definition and development earlier and more comprehensively than in a standard IP deal. Xignal, in effect, takes a view on the likely success of a product and a share in its risks and becomes involved in product development rather than just silicon IP. It forgoes upfront charges for a higher royalty-based return on each product sold. (Xignal says that the level of royalty depends on the deal but

mentions a figure of 20% on gross margin.) You get the rights to manufacture the product, Xignal retains any new IP developed, and you can launch your project having invested less upfront capital.

Xignal has specialised in complex analogue and mixed-signal IP blocks, with sales into high-speed serial-data-link products, ADSL, and other fast/high-resolution products. Functional blocks are at the level of DACs, ADCs, PLLs, and more integrated ASIP (application-specific IP) for complete signal-processing functions. Xignal’s specific expertise is in high levels of analogue integration.—by Graham Prophet

► **Xignal**, +49 17 39836282, [www.xignal.com](http://www.xignal.com).

## Embedded world sizes up ARM

IF THE PRODUCT introductions featured at this year's Embedded Systems show in Nuremberg, Germany, are any guide, the architecture to watch in the embedded space is ARM. For example, Philips announced five new chips in its LPC2000 family (ARM7-based) that will provide a smooth migration path from 8 bits to 32 bits. Features include 60-MHz clocks, 1.8V operation, as much as 256 kbytes of embedded flash, a four-channel/10-bit ADC, and an on-chip boot loader for in-system and in-application programming. Philips is using the ARM7TDMI-S core, with the "Thumb" instruction set. Noting that the series benefits from the availability of widespread support from third-party tool vendors and ARM's own development tools, Philips has also introduced a low-cost starter kit that is priced from €150. The devices are the first in 0.18-micron CMOS with flash, says the company, and the flash itself operates with "near-zero" wait states. Small package sizes are also a feature, and the chips will start at around €5 (50,000).

If you need a precision data converter alongside an ARM core, Analog Devices offers the ARM7TDMI-based AD $\mu$ C702x family. The company, which bases an ex-

isting range called MicroConverter on the 8052, also cites the market migration from 8 to 32 bits (and to a lesser extent 16 bits) as a reason for the move. (The company was already an ARM licensee.) The series of parts will pair the 32-bit core with 12-bit, fast ADCs and DACs for use in automotive, industrial, and communications applications. Analog Devices will run the core at 45 MHz in this series and include functions such as flexible ADC inputs with low-drift on-chip reference voltages, three-phase PWM outputs, and uncommitted comparators. There will also be a small area of SRAM-based programmable logic where you can implement logic functions independent of the processor, to avoid the need for small amounts of external signal-steering logic. These 32- to 80-pin parts will offer 12-bit ADCs running at 1M sample/sec; the converter itself will be a multimode device. Once again, you can turn to third-party tool support with a complete chain from Keil or IAR, and Analog Devices offers a starter kit for \$249.

A further ARM alternative is Cirrus Logic's ARM9-based family, which adds 10 new parts to the EP93xx family. At the lower end of this introduction is a less-

than-\$10 ARM9 chip with a 166-MHz core and a 66-MHz bus. It includes LAN connectivity and USB 2.0 and suits low-cost Web-enabled applications. At the other end of the scale is a \$25 processor with Cirrus' system-on-chip configuration plus a PCMCIA interface and 2-D graphics engine. The entry-level, 208-pin EP9301 contains a five-channel, 12-bit ADC and numerous peripherals; a low-cost evaluation kit is available for \$350. High-end parts have 200-MHz cores with 100-MHz external buses and also host a math co-processor. The corresponding \$2745 evaluation kit includes a TFT touchscreen and a software package with Windows CE.

The parts include Cirrus' MaverickKey, which lets you give each processor individual hardware ID codes that, in conjunction with encryption, can both secure design data and implement digital rights management.

—by Graham Prophet

► **Philips Semiconductor**, [www.semiconductors.philips.com](http://www.semiconductors.philips.com).

► **Analog Devices**, +32 11 300 635, [www.analog.com](http://www.analog.com).

► **Cirrus Logic** +44 1491 414030, [www.cirrus.com](http://www.cirrus.com).

## Multiprocessor chip wraps up the multimedia phone

CELL-PHONE DESIGNERS CAN build handsets that will extend "living-room-entertainment" functions to mobile phones, promises Texas Instruments, using the company's OMAP2 processor. Compared with TI's OMAP device for smart phones, TI says that the the OMAP2 increases the processing power available to video by four times and the processing power available to 3-D graphics by 40 times; the target applications are multimedia and games. The architecture will support 6M-pixel cameras, DVD-quality video, interactive gaming, hi-fi music with 3-D sound effects, analogue- and digital-TV broadcast reception, high-speed wireless connectivity, and LCD screens of greater than VGA resolution.

Using its 90-nm silicon process and the ARM11 architecture, TI has implemented a parallel structure, essentially fabricating a dedicated processing engine for each major function. Video- and graphics-acceleration blocks back up the ARM and a DSP. The first chips, which TI will release later this year, will contain a separate applications processor and a baseband processor. The company will release the 2410 and 2420 devices in the second half of 2004. The

2410 will include the ARM1136JS-F core, which contains ARM's hardware support for Java acceleration and a camera interface. The 2420 will add a programmable imaging and video accelerator supporting 4M-pixel still-image capture. Videoprocessing a CIF or VGA resolution will include both decode and encode compression. Future chips in the range will include further integration, bringing the base-band processor onto the same die. As you might expect with routing so much data around the chip, the architecture includes a crossbar switch fabric.

Design of a "new class of all-in-one entertainment phone" will not require a "quantum leap" in the skills of the OEM designers, TI asserts, as there is support for both full design and all the commonly used mobile operating systems. Nor has the company achieved the combined function set at the expense of power; a separate device, the TML92230 energy-management companion chip, means that power demand should be comparable with today's smart-phone figures of around 90 minutes of video viewing time.—by Graham Prophet

► **Texas Instruments**, [www.ti.com/omap2](http://www.ti.com/omap2).

## FPGA-design software includes microprocessor IP

**N**EXAR IS A SOFTWARE-DESIGN ENVIRONMENT aimed at bringing a new ease of use to working with FPGAs and exploiting the new generation of complex but affordable programmable products. It combines elements of hardware and

embedded software-design systems, IP blocks, virtual instrumentation, and a reconfigurable development board to provide a drag-and-drop approach to building processor-based systems on FPGAs. Graphical schematic-capture tools allow the interconnection of presynthesised and preverified IP (intellectual-property) components, including a range of processor cores. You can simultaneously build the circuit (translated to FPGA-configuration code by the Nexar software) and embed software virtual instruments, such as logic analysers and signal sources.

The schematic entry links to an EDIF description, where Nexar's library holds processor models with the complexity of 8051, Z80,

or PIC164 processors. There are also compatible peripherals, and the software incorporates conventional logic de-



**Altium's Nexar combines drag-and-drop hardware design with a software-development environment.**

sign where there is no off-the-shelf IP. You can combine Nexar with Altium's

board-design-product Protel to take the design through to a completed pc board. The FPGA vendor's own software handles FPGA place and route, according to your target device. (Altium says it will support all of the devices in common use.) You install this software on the design system, but Nexar calls it transparently. The environment handles writing embedded code within the same system

and understands the partitioning of each hardware and software; changes in code will

not cause the systems to re-synthesise unless you change the hardware.

With this concept, the company says it has addressed two major issues preventing average engineers from designing embedded systems on FPGAs: obtaining the IP itself (the IP in Nexar is royalty-free) and integrating it without heavily investing in tools that derive from ASIC methodologies. Also, Altium adds, current methodologies don't address the issue of integrating software development and debugging into the same environment. Altium circumvents issues of gate-level simulation and hardware/software partitioning in development by including its NanoBoard platform hardware in the system. The FPGA itself forms part of a reconfigurable development target. You prototype on the target device, and, in contrast to simulation, Altium says, your verification tells you whether the design *does* rather than *should* work. Base price for the Nexar system is €8000.

—by Graham Prophet  
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