



The nuances of op-amp integrators

AN INTEGRATOR THAT YOU configure with an op amp is a simple circuit consisting of a resistor, a capacitor, and an op amp, so how can anything go wrong?

In **Figure 1**, when Z_F is a capacitor, the closed-loop ideal-gain equation is $G = -1/R_G Cs$, where s is the Laplace complex operator. Thus, the circuit performs a pure integration. Some designers mistakenly claim that this configuration can be unstable, so you can calculate the loop gain using **Equation 1** to determine whether a potential stability problem exists.

$$A\beta = \frac{aR_G}{R_G + Z_F} = \frac{aR_G Cs}{R_G Cs + 1}, \quad (1)$$

where a is the op-amp open-loop gain.

On the well-known Bode plot, the zero contributes 90° positive phase shift starting at the lowest frequency axis, and the pole contributes -45° phase shift at the frequency at $f = 1/(2\pi R_G C)$. The total phase shift is 45° at $f = 1/(2\pi R_G C)$, and the phase shift decreases to zero at approximately $10f$. The phase shift never comes close to the -180° required for instability, so the circuit problems must be elsewhere.

Op amps contain transistors that require input currents. The input current flows from ground into the circuit if the op amp has

npn input transistors, and the current flow is opposite for pnp transistors. The inverting-input current flows from ground through R_G and C . Regardless of how small the input current is, it eventually charges the capacitor, causing the op amp to saturate at the positive rail (for pnp input transistors).

You can easily solve the saturation problem by adding a resistor in parallel with C ; the resistor supplies the bias current, and saturation

reduces to a small voltage offset. The closed-loop gain and loop-gain equations with the added series resistor follow:

$$G = -\frac{R_F Cs + 1}{R_G Cs}, \quad (4)$$

and

$$A\beta = \frac{aR_G Cs}{(R_G + R_F)Cs + 1}. \quad (5)$$

You regain the pure integration if $R_G C$ is greater than $R_F C$, and this integration lasts almost until $f = 1/(2\pi R_F C)$. The loop gain has a

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tion reduces to a small voltage offset. The closed-loop gain and loop-gain equations with the added parallel resistor follow:

$$G = -\frac{R_F}{R_G} \frac{1}{R_F Cs + 1}, \quad (2)$$

and

$$A\beta = \frac{aR_G}{R_F + R_G} \frac{R_F Cs + 1}{R_F \| R_G Cs + 1}. \quad (3)$$

You lose the pure integration with the addition of R_F . The circuit is an amplifier with an inverting gain of $-R_F/R_G$ until the input frequency approaches $f = 1/(2\pi R_F C)$. Then, it acts as an integrator for higher frequencies, or a lowpass filter. The zero in the loop gain always precedes the pole in the frequency domain; thus, this circuit is always stable. Actually, you often add a

zero, which contributes 90° positive phase shift at the low-frequency axis, so the pole usually can't cause instability. Situations might arise in which $R_G C$ is less than $R_F C$ and the circuit is unstable, but I've never seen this case.

Some final points to consider are:

- Nonrepetitive input signals require resetting the integrator by discharging C (FET in parallel with C),
- C is subject to dielectric stress that can cause a dual slope integration, and
- you must account for C 's leakage current.

Inverting integrators are well-behaved circuits, but, like all analog circuits, they require attention to detail. □

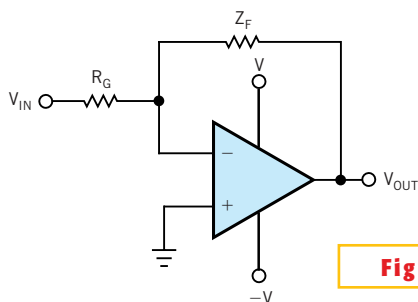


Figure 1

The basic op-amp integrator is not as simple as it looks at first glance.

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