Edited by Bill Travis

Positive feedback yields fast amplifier with precision dc offset

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Some signal-processing applications require a high-speed, low-noise, dc-coupled amplifier that incorporates a precision dc-offset adjustment. Examples include oscilloscopes, in which the offset adjustment typically acts as a “position” control), ADC-input gain blocks, and scanning-ion-beam-microscopy deflection circuitry. **Figure 1** illustrates the circuit concepts. Op amp IC$_{2A}$ is a 70-MHz, high-slew-rate device configured with a fixed gain of 3 (9.5 dB) and a ±10V precision offset adjustment. Op amp IC$_{1A}$ buffers and thereby linearizes the offset potentiometer. IC$_{1A}$ is a low-cost, low-frequency device that befits the dc circuit it occupies. But the mismatch between the frequency responses of IC$_2$ and IC$_{1A}$ creates the need for the novel topology of **Figure 1**. An obvious way to couple IC$_{1A}$ and IC$_{2A}$, which might seem to allow the addition of dc offset, would be to omit R$_1$, R$_2$, R$_5$, and C$_1$ and simply connect IC$_{1A}$ as a unity-gain buffer providing the termination for the gain-set resistor, R$_3$. Unfortunately, this scheme wouldn’t work, because the output impedance of the pokey IC$_{1A}$ starts rising at frequencies far below the capabilities of the speedy IC$_2$.

This drawback would ruin the high-frequency performance of the composite

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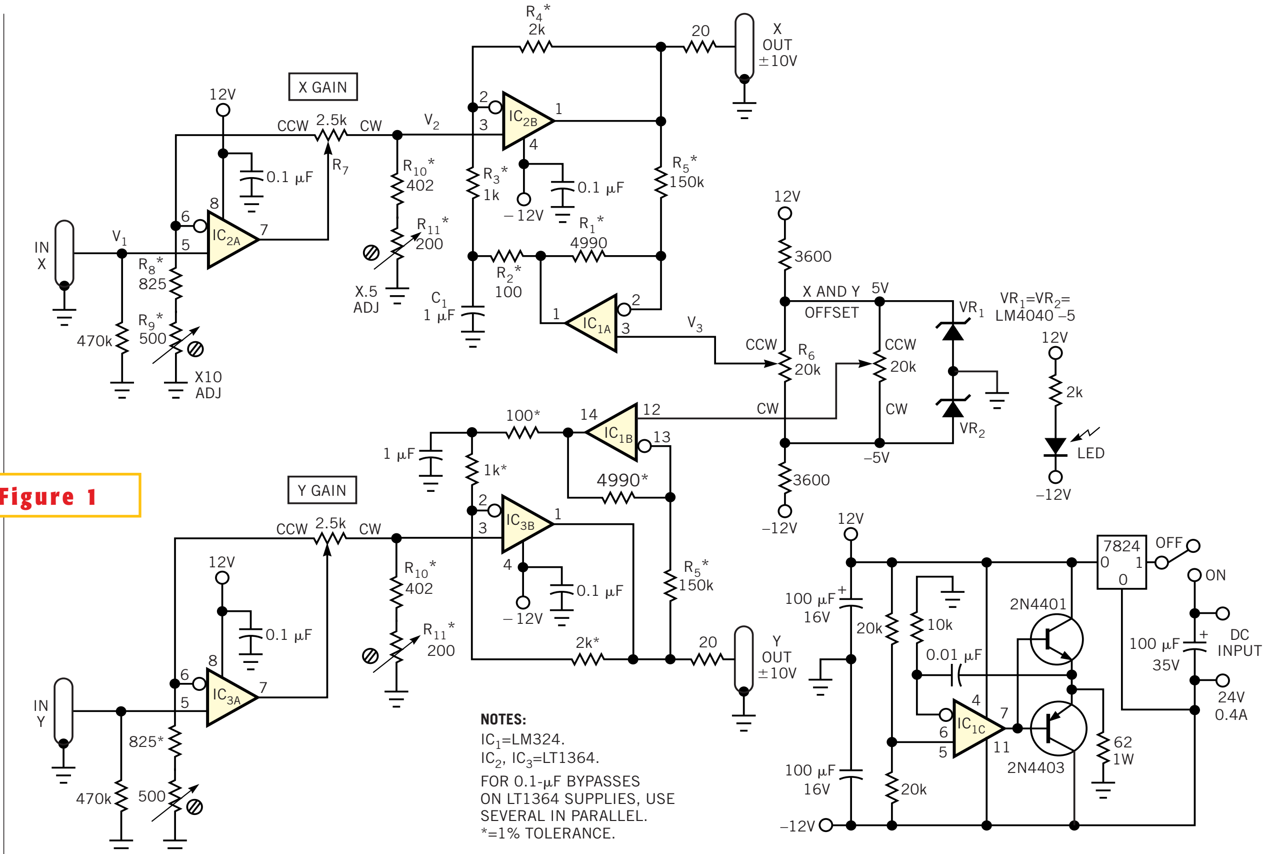

Figure 1

In this circuit, positive feedback makes it possible to obtain wide-range dc offset without compromising bandwidth.

amplifier. You could (partially) avoid this problem by using another LM1364 in place of the LM324, but the result would be a significantly noisier circuit because of the summation of IC_{1A}'s output noise with the signal at point V_2. This Design Idea offers a different approach, in which C_1 provides a robust, low-impedance termination for R_3, and the R_2C_2 time constant isolates the signal path from noise originating in either IC_{1A} or the VR_1 and VR_2 voltage references. Unfortunately, this approach creates a problem arising from R_2's dc resistance. C_1 holds down the bottom end of R_3 for ac-signal frequencies higher than 1 kHz or so. But near dc, R_2 and R_3 tend to sum, and the summing action would make the closed-loop gain of IC_2 approximately 10% less for dc-signal components than for ac. The circuit avoids this effect by using positive feedback that R_1 and R_5 provide.

The dc gain that R_1 and R_5 provide generates a compensation-voltage component that nulls the voltage drop across R_2. This action cancels the tendency of the R_3C_1 node to track IC_{2A}'s input and makes IC_2's output accurately equal to $V_{OUT}=V_2(1+R_4/R_3)-V_3(R_4/R_3)=3V_2+2V_3$. The rest of the schematic illustrates the use of the offset circuit in a dual-channel amplifier. In this amplifier, the variable-gain front ends incorporate a pseudologarithmic gain adjustment spanning gains of 0.5 to 10 (−6 to +20 dB). To achieve this wide gain-control range with a single-turn potentiometer and maintain reasonable adjustment resolution without compromising the LT1364s' 20-MHz capability, the control potentiometer, R_7, is connected such that its resistance element serves two circuit functions. The left half forms a variable-gain (1 to 3.33=0 to 10.5 dB) feedback network around IC_{2A}. The right half forms a variable-loss (1 to 0.167=0 to −15.5 dB) circuit. The net result, when you combine it with the fixed 9.5-dB gain of IC_{2A}, is an overall gain variable from (0−15.5+9.5)=−6 dB when you adjust R_7 to one extreme to (10.5−0+9.5)=20 dB when you adjust R_7 to the other extreme. IC_{1C} finishes the gain-block subsystem by generating tracking ±12V rails, by splitting the ground of the 7824 24V regulator. This regulator uses as its source an inexpensive, unregulated wall-socket power supply.□

Buck regulator forms high-power, inverting −5V supply

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Configuring a step-down switching-converter IC as an inverter yields an efficient, high-power, −5V supply that can of deliver currents as high as 4.5A at the 12V input or 3.2A at the 5V input (**Figure 1**). Conventional inverting power supplies do their switching using a p-channel MOSFET (**Figure 2**). That configuration works well at lower currents, but has limited use above approximately 2A, depending on the input and output voltage levels and the MOSFET you use. If you compare a standard buck circuit with the circuit in **Figure 1**, you can see that the converter's "output" in **Figure 1** connects to ground, and what used to be ground becomes the −5V output (**Figure 3**). Because the on-resistance of an n-channel MOSFET is lower than that of a comparably sized p-channel device, a power supply with n-channel MOSFETs usually provides more current at higher efficiency. To turn on, however, an n-channel device requires a gate voltage approximately 4V higher than the source voltage, which is usually the supply voltage.

The circuit in **Figure 1** achieves high output current and high efficiency by re-

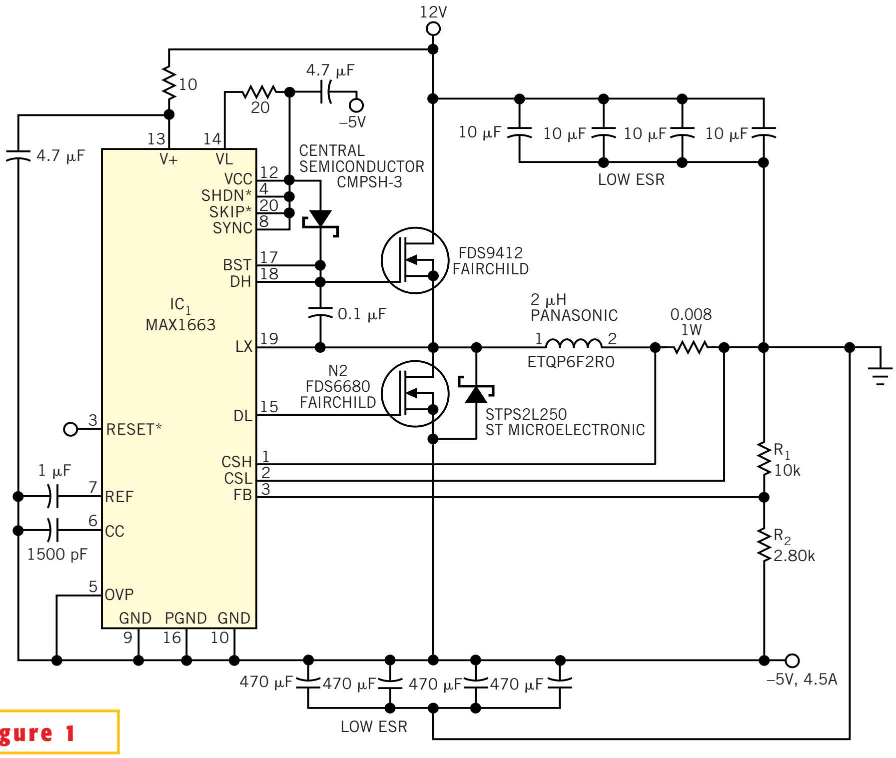
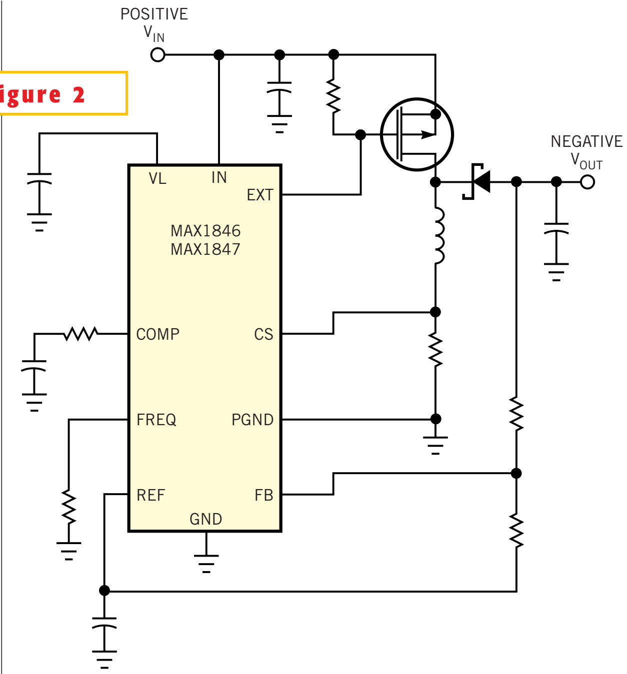


Figure 1

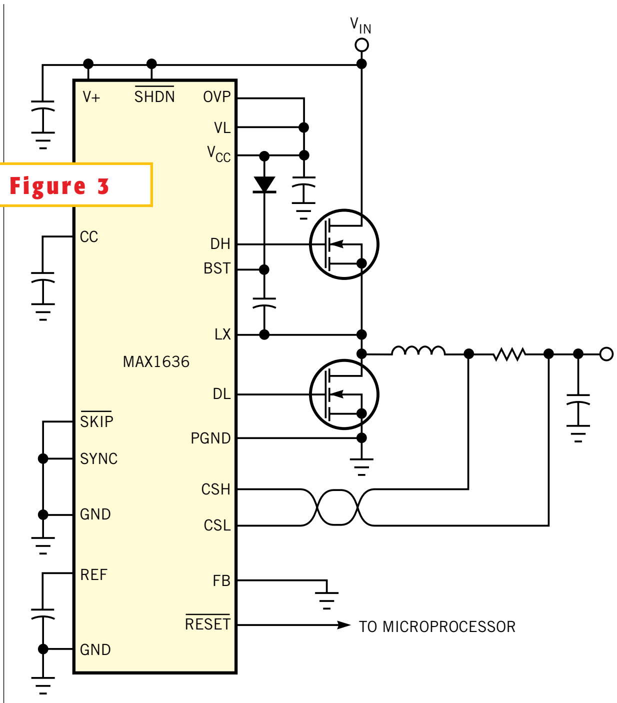
By configuring this high-power dc/dc step-down converter as an inverter, you can obtain 4.5A at −5V from a 12V input or 3.2A at −5V from a 5V input.

Figure 2



This conventional inverting power supply uses a relatively inefficient p-channel MOSFET.

Figure 3



IC_1 in Figure 1 normally operates as a high-power buck converter.

configuring a high-power buck converter, IC_1, as an inverter, thus exploiting an all-n-channel design. Efficiency is 90% with a 12.35V input, −5.02V output, and 4.7A load. The efficiency is 84% with a 4.56V input, −5.02V output, and 3.3A load. You can easily accommodate −5.2V applications by changing the values of R_1 and R_2. (Operation at −5.2V incurs a small penalty on maximum output current.) Input and output ripple voltages directly relate to the input and output capacitors' ESR (equivalent series resistance), so you should carefully select these capacitors. Circuit layout is also extremely important, as for all dc/dc converters. You may want to consider the MAX1636 evaluation kit from Maxim (www.maxim-ic.com). The kit includes a small pc board with optimized layout and all components necessary for operating the MAX1636. Because the board's layout is similar to the one required in **Figure 1**, the kit can serve as a rough layout guide for this Design Idea.□

Low-loss circuit powers solar lantern

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THE SOLAR-LANTERN CIRCUIT in **Figure 1** is a low-loss configuration that uses a 7W, four-pin CFL (compact fluorescent lamp) and a 12V, 7-Ahr, sealed, maintenance-free battery. The inverter features greater-than-85% efficiency, less-than-2-mA quiescent current, and a shunt-charge controller with deep-discharge and overcharge protection for the battery. The low quiescent current and the deep-discharge and overcharge protection ensure long life for the battery. The preheating feature in the inverter avoids the blackening of the end of the CFL, thereby ensuring long life. The circuit finds application in rural areas as a reliable, compact, portable light source and in urban areas as an emergency-lighting system. The shunt charge-controller circuit comprises IC_1, a low-current, voltage-reference 2.5V LM385, and IC_2, an LM324 comparator. IC_{2A}, with resistors R_1 through R_8 and transistor Q_1, provides protection against deep discharge of the battery.

The circuit switches off the load, including the inverter and the lamp, when the battery voltage falls below 10.8V and thus protects the battery from deep discharge. Under a no-load condition, the discharged battery voltage is approximately 12.2V. Hence, the circuit provides a deep-discharge reset level of 12.3V to avoid oscillations. Red LED_1 indicates a low-battery condition. IC_{2B} with resistors R_9 through R_{14} and transistor Q_2 provides protection against overcharging the battery. Q_2 switches on

TABLE 1—WINDING DETAILS FOR TRANSFORMER

Start pin	End pin	Wire gauge	Turns	Inductance
2	1	26	21	28 mH
3	4	26	21	28 mH
6	10	38	380	17 mH

Core: EE25/13/7

and shunts the solar array when the battery voltage exceeds 14.8V and thus protects the battery from overcharging. Q_2 turns off when the battery voltage drops below 12.5V and thus enables battery charging. D_2 is a reverse-blocking diode. It prevents the discharge of the battery through the solar cells when the cells are not generating electricity. Amber LED_2 indicates that the battery is in full-charge condition. Green LED_3, along with IC_{2C} and resistors R_{15} through R_{20}, provides an indication of charging.

TABLE 2–WINDING DETAILS FOR INDUCTOR L_2

Start pin	End pin	Wire gauge	Turns	Inductance
1	2	27	215	8.2 mH

Core: EE25/13/7

Tables 1, 2, and **3** give core and winding details for the magnetic components in the circuit. The inverter uses a Class D, push-pull, force-driven topology with MOSFETs as switching devices. IC_3, an SG3524, drives the inverter. The force-driven topology ensures trouble-free start-up in all environmental conditions. The switching frequency is approximately 26 kHz. Q_6, along with resistors R_{29}, R_{30}, and R_{31} and capacitor C_{10}, forms the preheating circuit. In addition to the 12V, 7-Ahr sealed, maintenance-free battery, the circuit uses a 10W, 12V single-crystalline-silicon solar-cell panel. The recorded backup time is approximately eight to 10 hours for a fully charged battery with a light output of 370 lumens using a 7W, four-pin CFL.□

TABLE 3–WINDING DETAILS FOR INDUCTOR L_1

Wire gauge	Turns
26	100

Core: Ferrite rod, 5-mm diameter, 25 mm long.

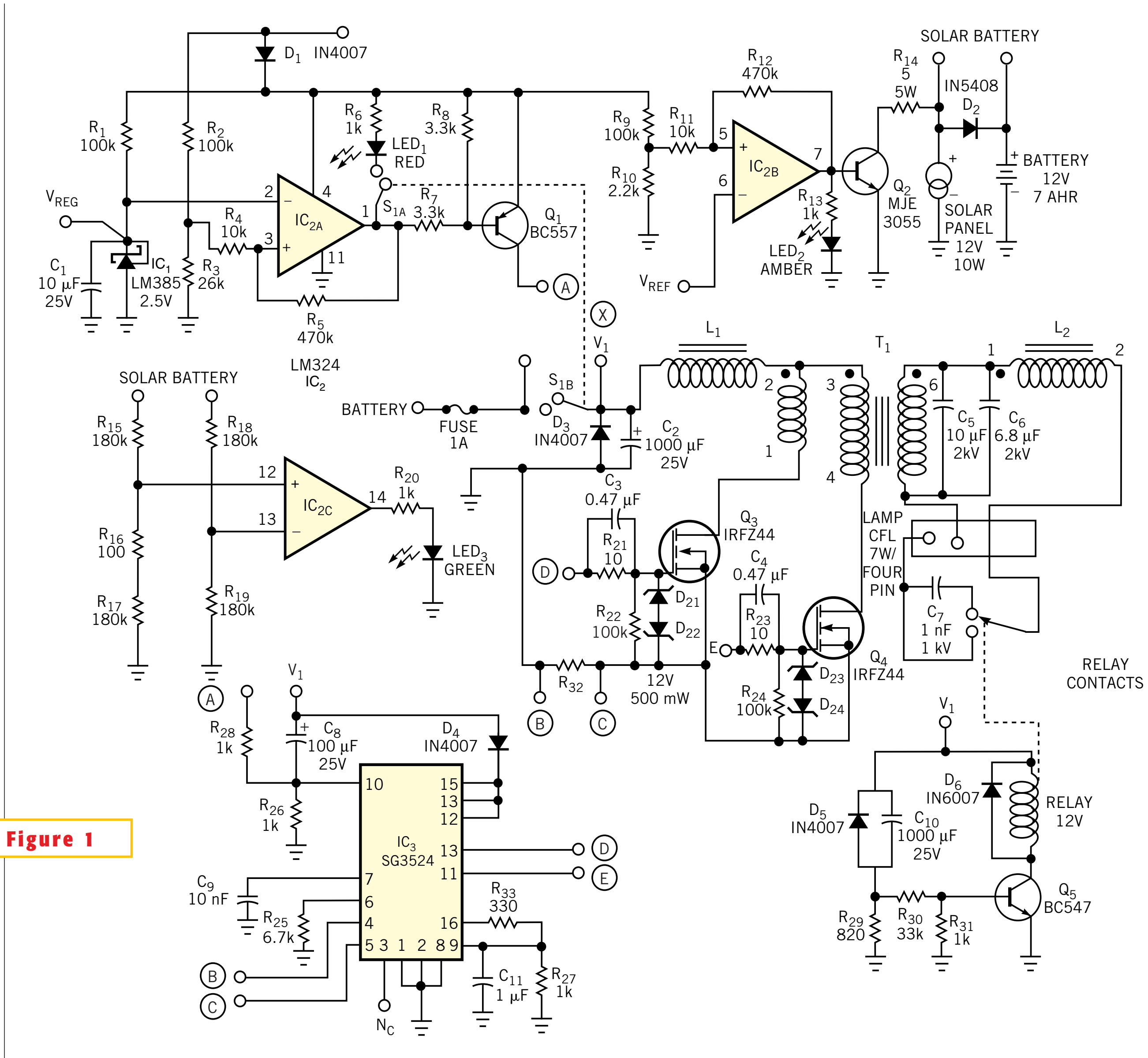


Figure 1

This solar-powered lantern driver can serve as an emergency lighting system.

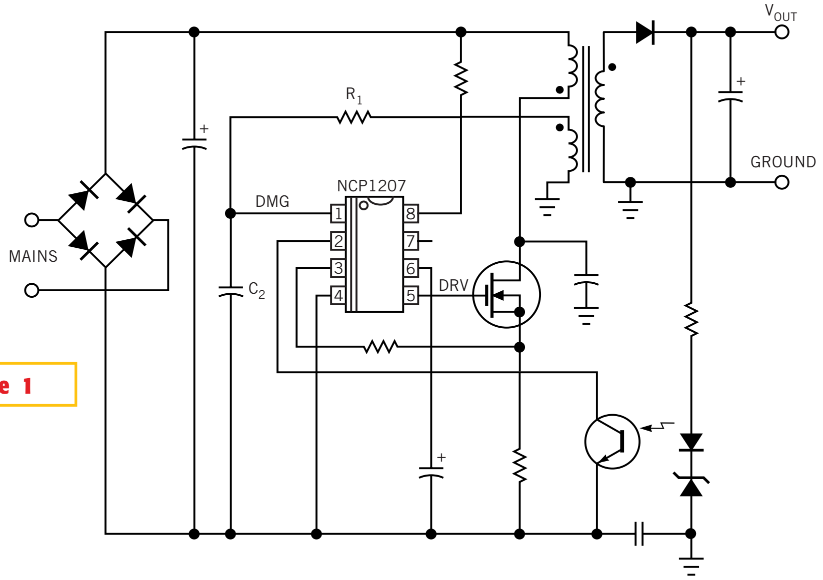
RC network quashes auxiliary winding in quasiresonant converter

Nicolas Cyr, On Semiconductor, Toulouse, France

Quasi-square-wave-resonant converters, also known as QR (quasiresonant) converters, allow the design of flyback-type SMPSs (switch-mode power supplies) with a reduced EMI (electromagnetic-interference) signature and improved efficiency. You can achieve so-called QR operation by authorizing the turn-on of the switching MOSFET when the drain voltage reaches its minimum—hence, the name valley switching operation. The circuit usually externally detects the minimum drain voltage of an auxiliary winding, which delivers a voltage image of the core's internal flux activity. The circuit in **Figure 1** offers a solution that incorporates core-reset detection with the aid of an auxiliary winding. As you can see, the auxiliary winding solely performs the function of core-reset detection. To further simplify this schematic, you can remove the auxiliary winding and use the drain signal itself to generate the demagnetization signal that Pin 1 of the NCP1207 requires. **Figure 2** shows this arrangement. Thanks to its use of high-voltage technology, On Semiconductor's (www.onsemi.com) NCP1207 QR controller can derive its power directly from the rectified mains via its "dynamic-self-supply" feature.

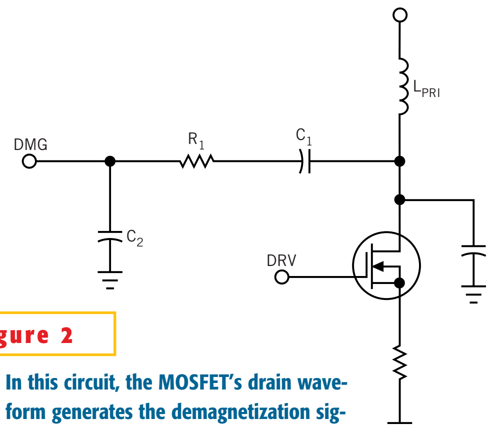
Capacitor C_1 removes the dc component of the drain signal. R_1, together with the internal resistor on the NCP1207 demagnetization pin (Pin 1), creates a resistor divider. The divider safely limits the voltage you apply on the controller when the drain swings high. C_2 delays the signal to detect exactly the drain signal valley. Compared with **Figure 1,** where R_1 and C_2 were present, the only addition is C_1 (in replacement of the auxiliary winding. Because capacitor C_1 touches the MOSFET drain, it must sustain at least the same maximum voltage: A 220-pF, 1-kV or 1-nF, 1-kV ceramic capacitor perfectly fills the bill. The internal resistance of NCP1207's demagnetization pin is 28 kΩ. The value of R_1 ranges from 1 to 2 MΩ if you want to create a 5V signal with a maximum drain voltage of 600 and 900V. The value of capacitor C_2 depends on the frequency of the resonating network comprising the primary inductance, L_{PRI}, and the total capacitance of the drain node. You adjust the values of R_1 and C_2 directly on the board to reach the best valley detection possible. Because R_1 has a relatively high value, it is essential that the component resides close to the controller's Pin 1. The **Figure 3** waveforms show the final application results. The waveforms are captured on a single-output, 30W SMPS delivering 16V. In this application, C_1=220 pF/1 kV, R_1=1.5 MΩ, and C_2=100 pF. By properly adjusting the time constants, you can obtain perfect valley switching.□

Figure 1



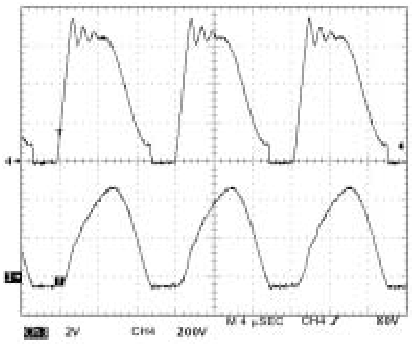
In this configuration, an auxiliary winding performs the function of core-reset detection.

Figure 2



In this circuit, the MOSFET's drain waveform generates the demagnetization signal for the controller IC.

Figure 3



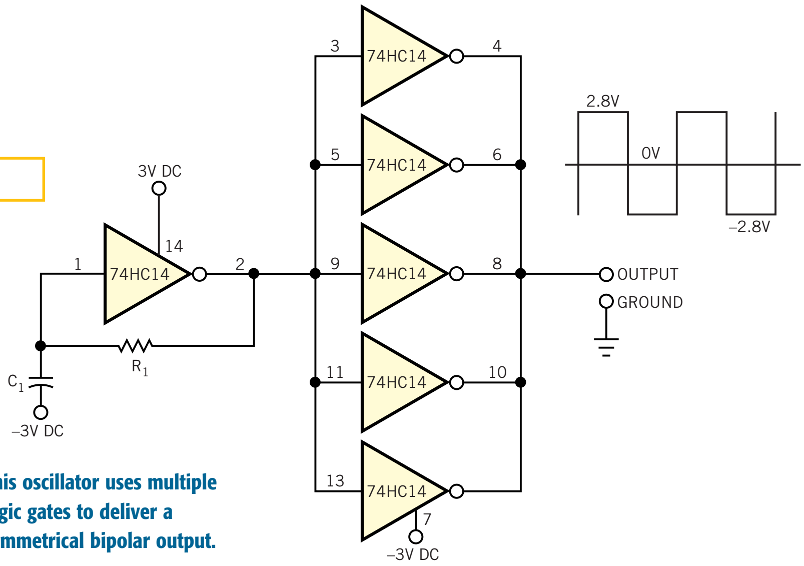
These waveforms illustrate the operation of Figure 1's circuit without the auxiliary winding.

Low-power CMOS oscillator has push-pull output

Shyam Sunder Tiwari, Sensors Technology Private Ltd, Gwalior, India

Digital oscillators often generate TTL- or CMOS-level outputs, referred to ground. Generating a symmetric bipolar output with respect to ground presents a challenge. In this design, four 1.5V flashlight cells create ±3V voltage sources, and the midpoint of cells acts as the ground reference (**Figure 1**). The oscillator at the input, based on the R_1C_1 time constant, generates a ±2.8V bipolar output. The symmetrical output waveform requires no dc-blocking capability to drive a piezoelectric buzzer or loudspeaker. The circuit works well with ±1 to ±3V sources and delivers a symmetrical output over the full range of source voltages.□

Figure 1



This oscillator uses multiple logic gates to deliver a symmetrical bipolar output.