

leading edge

What's hot
in the
design
community

Edited by
Fran Granville



EE wars

“What is it about electrical engineers? These guys just can’t get along. A group of them brings a wonderful new technology to market, and another equally brilliant band creates another way of doing the same thing.”

**—Hiawatha Bray,
on the Blu-Ray-versus-
Advanced Optical Disc
format debate,
in *The Boston Globe*,
March 22, 2004**

Float like a battery, sting like a capacitor

By Bill Schweber

A NEW BUTTON-CELL HYBRID from Evans Capacitor looks like a standard button-cell battery, and it uses the same 2325 holder as a battery, but it’s not a battery. It’s an 1800- μ F, 50V super-capacitor that targets use in aerospace, medical,

and other applications requiring a one-time or refillable jolt of energy. It offers high energy density despite weighing only 8g and measuring only 23 mm in diameter and 2.5 mm thick.

The exterior of the unit is nickel-plated for low contact resistance and houses a sintered tantalum pellet as the positive electrode with a TaO₅ (tantalum-pentoxide) dielec-

tric film, combined with a negative-electrode, conductive-metal oxide based on a RuO₂ (ruthenium-dioxide) film. The vendor says that internal resistance is one-thousandth that of electrochemical capacitors. This technology is internally complex and costs more than a standard battery, but if you need the performance and inherent ruggedness, the \$150 (one piece) is likely worth it.



Put a capacitor in a button-battery holder, and you can get the energy and voltage spikes you need but that batteries can’t provide.

► **Evans Capacitor Co,**
1-401-435-3555, www.evanscap.com.

Microcontroller adds precision analog

ANALOG DEVICES’ ADuC702x family of devices integrates a 32-bit ARM7TDMI core with 12-bit data converters targeting industrial, optical-networking, and automotive-monitoring and -control applications. The analog peripherals include a 12-bit ADC with as many as 16 channels that can support 1 million samples/sec, as many as four 12-bit DACs with a 10- μ sec settling time, and a precision bandgap reference sensitive to 10 ppm/ $^{\circ}$ C. Other peripherals include a comparator, a small programmable-logic array for glue logic, and a three-phase PWM generator.

The AduC702x devices are currently available for sampling, and production quantities will become

available in October. Prices range from \$4.55 (1000) for the 32-kbyte-flash-memory device to \$12.80 (1000) for the full-featured, 62-kbyte-flash-memory ADuC7026. Packaging options range from a 6 \times 6-mm, 40-lead CSP to an 80-pin LQFP. The 3V devices operate at -40 to +85, +105, or +125 $^{\circ}$ C. The QuickStart development system includes a power supply, cables, an evaluation board, a JTAG emulator, and software-development tools from Keil Software and IAR Systems. The QuickStart Development System sells for \$249 and is available directly from Analog Devices.—by Robert Cravotta

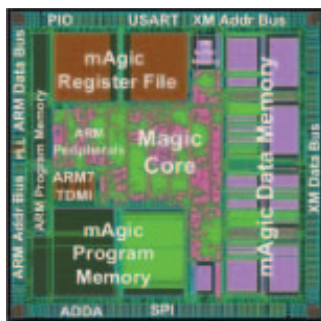
► **Analog Devices,** 1-800-262-5643, www.analog.com.

Floating-point DSP gets “RISCy”

PROCESSORS THAT INTEGRATE a DSP core with a microcontroller core on one device are becoming increasingly common. Atmel’s Diopsis

AT572D740 continues this trend by integrating a VLIW (very-long-instruction-word) mAgic DSP core with an ARM7TDMI microcontroller core. However, this integration differs from the other DSP/RISC-integration offerings because the mAgic core is a single-cycle, complex, floating-point DSP. It is becoming more feasible to consider using a floating-point DSP instead of porting floating-point algorithms to a traditional fixed-point core as process geometries continue to shrink; on-chip memory is becoming the significant user of real estate, and the cost of implementing a floating-point architecture is shrinking relative to the system cost. Diopsis, operating at 100 MHz, typically consumes 0.8W and 1.4W in the worst case.

The mAgic core’s native support for complex floating-point operations makes it a candidate for frequency-domain algorithms, time- and frequency-domain analysis, and frequency-spatial wave-



The Diopsis processor integrates a DSP core and a microprocessor.

number algorithms that would benefit from or require the extra range and precision of 40-bit floating-point data. The mAgic core targets heavy floating-point algorithms and can perform 10 floating-point and pipelined-complex-arithmetic operations per cycle. The AT572D740 includes two SPI serial ports, two USARTs, a timer/counter, watchdog timer, a parallel-I/O port, a peripheral-data controller, eight ADC and eight DAC interfaces, a clock generator, and an interrupt controller.

The control registers and memories of the mAgic DSP

map directly into the ARM memory space so that the ARM can read or write the DSP local data memories and configuration registers. In system mode, the ARM can modify the DSP-program memory by initiating a DMA transfer from the external memory or by directly writing four 32-bit words to four consecutive addresses at the appropriate program-memory location. In run mode, the ARM may access only the mAgic command register and a 1000× 40-bit, dual-port shared memory. Both processors operate their own programs, and either processor may operate as the master.

The MADE (Modular Architecture Developing Environment) supports DSP- and RISC-code development in one environment. That support includes C compilers for the ARM and mAgic cores, a macro assembler/optimizer, visual debuggers and simulators, and Light RTOS. The Diopsis AT572D740 is available now in a 352-ball PBGA industrial-temperature-range package for \$30 (1000).

—by Robert Cravotta

► **Atmel**, 1-408-441-0311, www.atmel.com.

SIMPLE DEVICE PICKS OFF LINE CURRENT

It’s sometimes the little things that make your test and monitoring task go smoothly and safely. For example, the ELS2 ac-line splitter from Wavetek Meterman plugs into a standard ac outlet and physically



Safely and easily monitor your ac-line current with the ELS2 line splitter, which has current-probe clamp-on locations for 1 and 10× ranges.

splits the conductors, so you can hook a standard current-clamp probe around one conductor and monitor the power situation with a meter or scope. The \$13.95 device offers both 1 and 10× clamp locations to ease accurately measuring low-level current if necessary.—by Bill Schweber

► **Wavetek Meterman Test Tools**, 1-425-446-5070, www.metermantesttools.com.

DILBERT By Scott Adams



► **General Motors expected to produce its 1 millionth satellite-radio car in March 2004.—The Boston Globe, March 1, 2004**

The best of both (logic) worlds?

STRUCTURED ASICs and high-density FPGAs both attempt to address chip designers' demands for devices with traditional ASIC-like high density, high speed, low per-gate cost, and low power consumption but without ASICs' increasingly high NRE (nonrecurring-engineering) charges and lengthy delays from design completion to the arrival of first chips in hand (see "Silicon segmentation," *EDN*, Sept 18, 2003, pg 57). Neither silicon extreme is ideal for all possible applications, though, and Leopard Logic officials think there's plenty of room left over for its in-between, mutually encompassing CLD (configurable-logic-device) approach.

In its initial incarnation, Leopard Logic was a provider of embedded FPGA IP (intellectual-property) building blocks to ASIC and foundry suppliers. However, the company obtained insufficient industry interest—a situation, the company claims, resulting from the sluggish financial-investment market of recent years, *not* reflecting any fundamental invalidity of the company's technology. So, Leopard decided to reinvent itself as a silicon supplier, thereby competing with its former potential customers.

The company's Gladiator devices combine HyperBlox MP (mask-programmable) and FP (field-programmable) logic modules, DLLs and

PLLs, dual-port SRAM arrays, and MAC (multiply-accumulate) circuits on a single chip, encircled by a configurable-I/O ring. FP and MP logic blocks are functionally identical, simplifying EDA tools' efforts, but, whereas SRAM elements configure the FPs when the chips are in customers' hands, a single via layer customizes the approximately 20-times smaller MP blocks during the final stages of device fabrication. Robust, hierarchical interconnect structures tie the FP and MP subsystems together and to the remaining circuits on the device.

Leopard Logic is focusing its initial ToolBlox script and library support on Synopsys' ubiquitous Design Compiler,

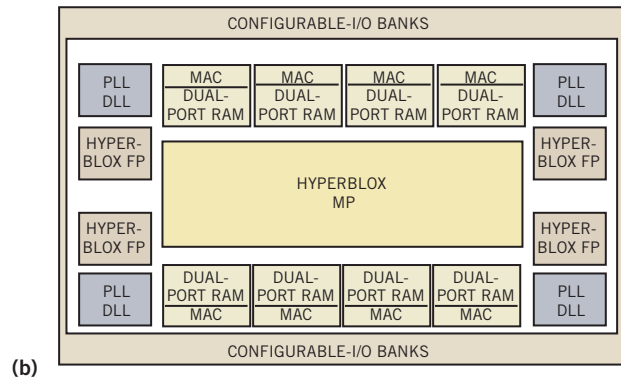
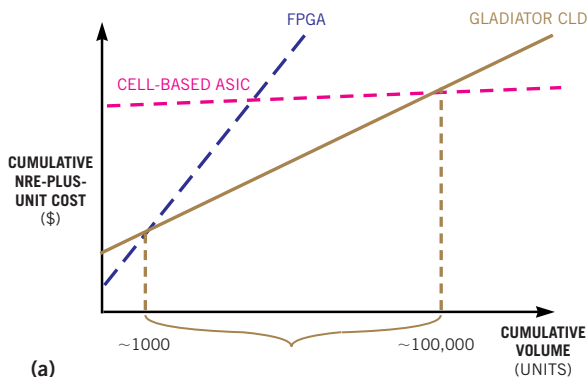
and it also anticipates offering Mentor Graphics support. The company plans to offer a range of devices with varying achievable gate counts and amounts of various on-chip resources (Table 1). The initial CLD6400 device, fabricated on TSMC's 0.13-micron process, is now available and is forecast to cost \$95 (100,000) in early 2005. Leopard Logic estimates that it can turn around product samples in less than four weeks after you ship the company \$50,000 in NRE charges and a compiled bit stream representing your design.

—by Brian Dipert

► **Leopard Logic**, 1-408-777-0905, www.leopardlogic.com.

TABLE 1—GLADIATOR CLD FAMILY MEMBERS AND THEIR ON-CHIP RESOURCES

Device	No. of system gates (millions)	No. of mask-programmable cells	No. of field-programmable cells	No. of 36-kbyte dual-port RAM arrays	No. of 18×18-bit MACs	No. of PLL DLLs
CLD1600	1.6	16,000	1000	16	16	Four
CLD3200	3.2	32,000	2000	32	32	Eight
CLD6400	6.4	64,000	4000	64	64	16
CLD12000	12.8	128,000	8000	128	128	16
CLD25000	25.6	256,000	16,000	256	256	16



Leopard Logic believes its Gladiator CLDs are the optimal silicon foundation for 1000- to 100,000-gate designs (a), and the chips encompass both fab- and field-programmable-logic blocks, along with other analog and digital circuits (b).

► The overall Ethernet-switch market grew moderately in the fourth quarter of 2003, rising nearly 7% to 55.6 million ports shipped, an increase from 52.2 million ports shipped in the third quarter, according to In-Stat/MDR.

Chip set shrinks EDGE phones to smaller than business-card size

TEXAS INSTRUMENTS has announced the TCS3500, an EDGE (enhanced-data-rates-for-GSM-evolution) chip set in a form factor one-half the size of a business card. The device comes with a hard-

ware- and software-reference design for creating EDGE-based smart phones, feature phones, and PDAs. Targeted applications include multimedia, gaming, camera functions, and video. The reference design supports leading mobile operating systems, including Symbian OS, Microsoft's Windows Mobile, Linux, and Palmsource, as well as Nokia's Series 60 terminal-software platform and multiple third-party Java plat-

forms. Support of standard real-time operating systems, such as Nucleus, offers a migration path for feature-rich GPRS (General Packet Radio Services) phones moving toward EDGE.

The EDGE protocol stack integrates the various operating systems, which carriers validate, and is Class12-capable. Future support will include extended dynamic allocation, DTM (dual-transfer mode), SAIC (single-antenna-

interference cancellation), and dual-mode UMTS/EDGE.

The reference design, which is in the pre-field-approval stage, offers three integrated modules for optional capabilities. The Version 1.2-certified Bluetooth module coexists with Wi-Fi; has active- and shutdown power consumption of 12 mA and 6 μ A, respectively; and integrates baseband, digital-RF, and an antenna switch in a 4.5 \times 4.5-mm package. The wireless-LAN module supports 802.11a/b/g, has a single 20-MHz clock, supports 2.4- and 5-GHz speeds, and requires no external memory. The programmable, cellular-modem-air-interface-independent A-GPS (assisted-Global Posi-

tioning System) module supports current and future standards and can maneuver between stand-alone, mobile-station-assisted, and mobile-station-based modes.

TI based the OMAP850 application processor on the OMAP730 with added EDGE capabilities, support for camera sensors with resolutions as high as 2 million pixels, enhanced frame-buffer-interface data rate, DDR support, and hardware-based security for e-commerce, digital-rights management, and antivirus protection. The TCS3500 sells \$35 (10,000), and samples will be available in this quarter.

—by Nicholas Cravotta

►Texas Instruments Inc, www.ti.com.

Tiny computer fits distributed-control applications

CLAIMING THE RECORD for the world's smallest single-board computer, General Micro Systems recently introduced the Spider. Measuring just 2.8 \times 1.9 in., the module offers stand-alone operation and hot-swap capability, making it suitable for a range of embedded-system applications, such as distributed-control systems, handheld computing, in-flight entertainment, and homeland security.

The Spider comes in a low-power version, the P501, based on IBM's 400-MHz 440GP, and a high-performance version, the P502, featuring IBM's 800-MHz PowerPC 440GX. Both modules come standard with two Ethernet ports, 256 kbytes of L2 cache, as

much as 256 Mbytes of DDR SDRAM, 16 Mbytes of boot flash, and 32 kbytes of user flash. They also provide two serial ports, an I²C port, a real-time clock, and a 32-bit device-bus with



No bigger than a credit card, this stand-alone, single-board computer from General Micro Systems delivers reliable computing power to remote locations.

DMA, which enables designers to add their own custom I/O without a PCI interface. To enhance stand-alone operation, the company offers a family of I/O modules that bolt directly to the Spider module in PC-104-like fashion.

Software support for Spider includes VxWorks-Tornado II and Linux. Both operating systems boot directly from the onboard flash, eliminating the need for rotating media or network booting. Modules consume 500 mA at 5 to 12V dc and operate from -40 to +85°C. Spider prices start at \$300 for the P501 and \$400 for the P502 (OEM quantities).—by Warren Webb

►General Micro Systems Inc, 1-909-980-4863, www.gms4sbc.com.

►According to InStat/MDR, sales of PICMG-based blade servers will grow to more than \$1 billion dollars by 2008, and the wireless-infrastructure segment will become the largest of that market over the next five years.