



**T**HE EDA INDUSTRY is a service industry. Its manner of growth depends on the directions and strengths of the industries it serves. The semiconductor industry has always been and will always be the primary motivator of EDA growth. Consumer applications have replaced IT (information technology) as the second most influential determinant of the type of products EDA companies develop. Both drivers have generated major changes in the requirements for EDA tools, and, as a result, the EDA industry is on the verge of a major change in the types of tools it will need to address new markets and additional requirements. Attendees at next month's 41st annual DAC (Design Automation Conference) in San Diego will be able to see the tools that are pioneering this design-paradigm shift. Princeton University professor Sharad Malik, general chairman of this year's conference, introduces many of the causes for this shift at this year's conference (see **sidebar** "What's on the horizon in EDA?").

The semiconductor industry impacts the EDA industry by providing new capabilities that support the fabrication of increasingly smaller geometries of transistors. This evolution is not new. Scientist Gordon Moore stated 40 years ago that the number of transistors on a device would double every 18 months. The industry quickly dubbed the statement "Moore's Law." Moore's prediction has so far come true, as semiconductor foundries have been able to improve fabrication technology by reaching process steps, or nodes, that manufacture increasingly smaller transistors on a wafer. Estimates of implementable processes indicate that the law may hold for at least six to eight more years. In almost all cases, semiconductor foundries have achieved the predicted doubling of transistor count by providing the ability to diffuse transistors on a die with dimensions smaller than the previous step and by occasionally increasing die dimensions. Whether the doubling of transistors will continue in the next decade is unclear and will depend on new technology, not continued refinement of current methods.

#### EVOLUTION IN THE NEW CENTURY

At the beginning of the new century, engineers could fabricate devices using optical methods, developing geometries with nominal sizes of 180 nm. Until then, the size of the required design was the most challenging obstacle to engineers. However, the larger the design you can fabricate on one die, the more complex the problems. EDA tools had to be able to handle both greater design databases and design hierarchy. Engineers use hierarchy to break the design into manageable pieces. Each piece is a unit that encompasses a function and a well-defined interface. To handle the complexity of each unit, engineers use HDLs (hardware-description lan-

**MOORE'S LAW IS NOT DEAD, AND THE EDA INDUSTRY IS CHALLENGED WITH KEEPING IT PROFITABLE. THIS TASK REQUIRES A CHANGE IN FOCUS FROM DESIGNING SILICON STRUCTURES TO PRODUCING SYSTEMS.**

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# FROM THE ASHES

# The next stage of EDA



guages) that support RTL (register-transfer-level) abstractions, such as Verilog or VHDL. Logic-synthesis tools transform that description into a netlist of gates using a library of basic logic blocks unique to the foundry chosen for the manufacturing of the device, and place-and-route tools generate the topology required to fabricate the masks to produce the device. With few exceptions, this methodology works well at the 180-nm process node.

In 2002, semiconductor technology took another step forward and began supporting 130-nm feature sizes. On the surface, this step appeared a normal evolution of the fabrication process. However, it introduced a major discontinuity that required a new approach to design and manufacturing and gave rise to many new issues. The wavelength of the optical source required to expose the circuit features on the photoresist was smaller than visible light, so manufacturers used RET (reticle-enhancement technology) and OPC (optical-proximity-correction) techniques to achieve the required feature sharpness, and EDA tools were called on to support the new

#### AT A GLANCE

- ▶ Advancements in process technology are challenging traditional ASIC-design methods.

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- ▶ Using clusters of application-processing units will shift the development burden to software.

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- ▶ ESL will become the fastest growing segment in the EDA market.

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- ▶ Designers will increase their use of FPGA and structured-ASIC devices in systems.

methods with new or improved DFM (design-for-manufacturing) tools.

Many other consequences of the smaller transistor geometries have had an even greater impact on design methodology. Two in particular have required new development tools: A logic gate is now generally smaller than the trace used to interconnect the gates, and the width of a trace is sometimes smaller than its height. In the first instance, engineers must use new tools to correctly predict

the physical and logical behavior of the circuit; in the second case, they need to be concerned with parasitic effects that can turn the trace into an antenna. EDA vendors had to develop a new suite of tools to support designers targeting processes at the 130-nm node. Physical synthesis replaced logic synthesis. Physical synthesis works with place-and-route tools to determine the topology of the circuit, because both the functional and physical characteristics of the resulting circuit impact its correctness. In 2004, leading designers have produced ICs using 90-nm processes, and semiconductor companies have shown test circuits built at 65 nm. The 65-nm technology could be available for manufacturing devices as soon as late 2005.

Since the inception of Moore's Law and until the 130-nm process node, designers needed to know only logic design to produce a working IC. Today, the need to use physical synthesis requires engineers to understand fundamental physical laws that govern the behavior of electrical circuits. Unfortunately, few designers receive adequate training in this field during college. This circumstance

## WHAT'S ON THE HORIZON IN EDA?

By Sharad Malik, Princeton University

At next month's DAC (Design Automation Conference) in San Diego, discussions will focus on how to achieve the optimal balance between cost and the complexity, performance, and power requirements of new designs as the high-tech market begins again to cautiously grow.

Possibly even more than device or manufacturing limitations, the ability to deal with the various consequences of design complexity poses the greatest challenge to the trajectory of Moore's Law. For example, the need for more efficient forms of verification is becoming a pressing issue. For more advanced semiconductors, it is not uncommon for the verification effort to consume 50 to 70% of the entire design cycle. Fortunately, manufacturers have recently made great strides in overcoming some of the limitations that

have kept formal verification—FPV (formal property verification), in particular—from mainstream adoption. Speakers and panelists will discuss encouraging advancements in this area, promising more efficient forms of verification.

DFM (design for manufacturing) is another area of great interest as semiconductor yields are coming under increasing attack by ever more complex design rules and aggressive technology scaling that makes process variation more difficult to control. The emergence of new approaches, such as statistical-timing analysis, can help bring design and manufacturing closer together, enabling designers to effectively explore trade-offs between chip performance and parametric yield. Equally interesting are the discussions starting to occur in the industry

about the need for a next-generation silicon-implementation fabric. You can expect to hear all sides of this debate at DAC, examining whether the standard-cell-based ASIC methodology has reached the point of diminishing returns and whether a next-generation fabric is required. If so, will the solution employ a structured ASIC, a traditional FPGA, or perhaps yet another approach vendors have not yet introduced?

Embedded design will be a major area of interest at DAC, at which considerable advancements and discussions will take place. Multiprocessing embedded devices are becoming commonplace, requiring designers to start adopting sophisticated techniques, such as design frameworks for structural partitioning and efficient higher level modeling. Attendees will be able to hear in-depth discussions on advanced power modeling for

embedded design. Speakers will examine creative techniques for modeling the power consumption. They promise to optimize battery performance in embedded-system applications. Also, expect to hear more about emerging embedded-system trends, such as dynamic instruction sets that accommodate on-the-fly changes in system functions. New design techniques on the horizon may help embedded-system designers deliver optimal performance for a system that will be reconfigured many times during its lifetime. And embedded security is starting to be a major concern, as consumers store more critical information on handheld devices.

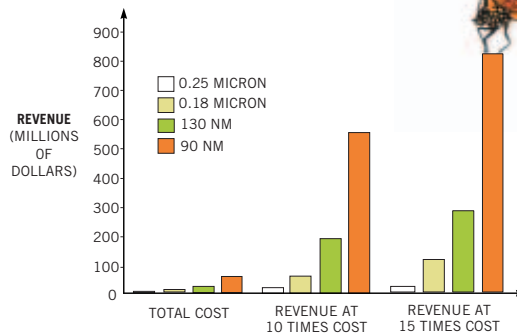
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adds a significant burden to the EDA tools, including the need to guide users toward solving problems they may not fully understand. Although EDA has invested and continues to invest significant resources to the development and improvement of new tools, the gap between the manufacturing capabilities of the semiconductor industry and the ability of designers and EDA tools to efficiently and economically develop circuits is widening. This situation contributes to the underuse of foundries and, ultimately, increased wafer costs.

Consumer products, especially communication and graphics devices, have replaced computing engines and information storage as the primary markets for system companies. These companies are the most important customers of EDA vendors, and their technical and economic requirements directly impact the welfare of the EDA industry. Consumer products differ from IT products because they have a shorter market window and are more sensitive to price competition. To be successful, a company needs to quickly develop products, normally in less than a year, and recover development cost rapidly enough to give products a chance to be profitable. Given the development costs associated with a typical IC produced with a 130-nm process, Ray Bingham, chairman and chief executive officer of Cadence Design Systems, using data provided by research company IBS ([www.internationalbusinessstrategies.com](http://www.internationalbusinessstrategies.com)), has projected that the typical product fabricated with a 90-nm technology will require an investment of \$55 million to cover NRE (non-



**Figure 1** Total development costs for advanced ICs are growing and require companies to generate large revenues in a short time to justify the product.

recurring-engineering) costs. A company looking to realize revenue equal to 10 times its investment, a normal target, would need to generate \$550 million in revenue from that product. Because the consumer market continually requires new features and new gadgets, a company must develop a large market and quickly generate revenue to cover its costs. As **Figure 1** points out, revenue equal to 15 times the investment would be \$825 million over the market life of a product. Few companies will be able to achieve the first of these goals, let alone the second, when you consider that the typical market life of a consumer product is less than 18 months.

**A NEW SOLUTION**

When the solution to a problem seems too difficult, most engineers know to try a different approach. Designers of SOC (system-on-chip) devices are increasingly using software to implement desired functions even at the 130-nm process node. IBS has calculated the average development costs for both hardware and software at various process nodes. As **Fig-**

**ure 2** shows, the percentage of software development has continued to increase as the features have shrunk, and its cost has increased proportionally. The 130-nm manufacturing process already provides operating characteristics that allow processors to sustain execution speeds fast enough to allow engineers to use software instead of hardware to implement many functions. Of course in cases in which execution speed is critical, dedicated hardware is still a better option. But these instances, once so prevalent that the requirement spawned the entire ASIC industry, are becoming less common.

When 65-nm and smaller process technologies are production-ready, their operating speed will make it possible to in most cases use application-specific processing units. Designers will be able to include a number of processing units on a single die, together with enough memory to store sophisticated application programs. To ensure maximum operating speed and appropriate bandwidth, the processing units will have to communicate over a network, because a bus would be too large and constitute a challenging physical structure to build while avoiding the associated parasitic phenomena. CODs (clusters on die) will replace SOCs. A number of APUs (application-processing units) will communicate over the network in the chip and collaborate to provide the required processing power to implement a system. **Figure 3** shows two generic examples of a COD architecture. **Figure 3a** shows a general approach, and **Figure 3b** shows a more specific architecture, in which APUs have dedicated memory or can even share a dedicated memory space.

In addition to a number of processing units and memory applications, engineers will also have at their disposal some customizable area of the chip that they can use for hardware-centric implementations. The choices of technology they use in this area will vary between classic ASIC and structured ASIC. It is unclear whether reprogrammability will be required, given the computational capabilities of the cluster already available on chip. It is highly likely that the “die” will in fact comprise at least two slices—one containing the digital logic and the other containing the analog circuits. This physical separation will be necessary to

**FOR MORE INFORMATION...**

For more information on products such as those discussed in this article, contact any of the following manufacturers directly, and please let them know you read about their products in *EDN*.

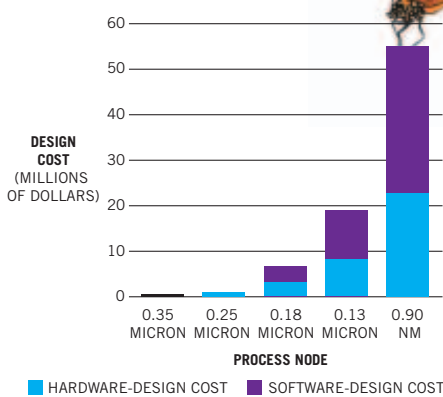
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use separate processes for digital and analog logic. This approach offers advantages: It continues to benefit from new process technology, it uses large macro blocks, and it allows users to upgrade products through reprogramming, thus decreasing costs over the market lifetime of a product family.

Companies that have traditionally been in the general-purpose-CPU business, such as Intel, AMD (www.amd.com), TI (www.ti.com), Motorola (www.motorola.com), and IBM could enter the COD market and provide powerful computing platforms that system companies could use in the way they first used mainframes, then minicomputers, and later, microprocessors. The primary task of designers would shift from generating silicon gates to designing approaches implemented mostly in software. Although at first this approach may seem revolutionary, it would, in fact, be an evolution of technologies and markets that have developed over the last few years. These areas include reconfigurable instruction processors; IP (intellectual-property) development and marketing; hardware/software co-design, also known as ESL (electronic-system-level) design; structured ASICs; and reconfigurable hardware systems.

IBM has gained valuable experience in the IP market through a distribution agreement with Xilinx that covers the PowerPC core. Although most of the feedback has come only from FPGA applications, customers have used FPGAs in ASIC applications, as well. ARM leads the processor-core field in standard cores, and Tensilica leads the field for configurable processors. CoWare also helps designers develop application-specific processors with its LisATek family of products. Tensilica has reported that a few of its customers have used as many as six configurable processors on one die, modifying the instruction set to produce application-specific processors. Synopsys is making a focused push into the IP market. Aart de Geus, Synopsys' chairman and chief executive officer, says, "System design is the systematic reuse of IP." Designers are likely to fill most of the available space in the configurable portion of a COD with IP. In this manner, they can reduce the



**Figure 2** Software development is a growing part of design costs.

development time and increase reliability by taking advantage of proven cores.

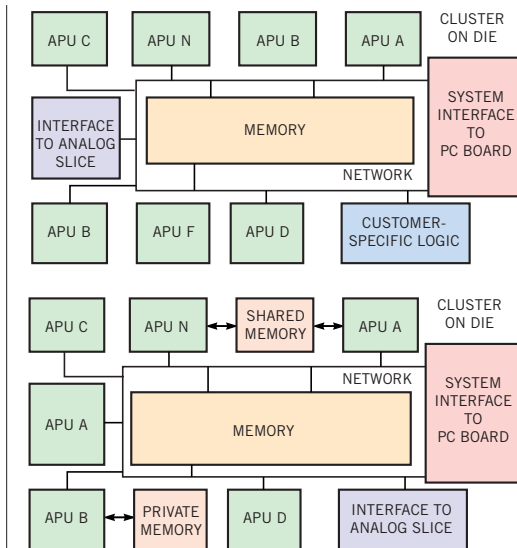
Arteris is developing network-on-chip technology that it based on a patented switch-fabric approach to managing multipurpose data packets. The company claims that its approach is compatible with a number of commercial bus protocols, including OCP and AMBA. To obtain the yield level required to make a product profitable, semiconductor foundries, EDA vendors, and end users will have to collaborate in the development of the product, because design decisions they make early in the flow will impact the degree of product manufacturability when using VDSM (very-deep-submicron) processes. Design engineers will have to become more knowledgeable in the manufacturing process, and manufacturing engineers will have to learn to

appreciate the cost of design trade-offs. As you can see, the complexities of VDSM projects will require significant investments, not only in development, but also in training and project management. Therefore, in most cases, producing programmable standard parts makes more sense than does producing ASIC devices.

### THE EVOLUTION OF ASIC DESIGN

During his speech at this year's EDAC (Electronic Design Automation Consortium), Adam Kablamian, president and chief executive officer of Virage Logic showed that, although EDA is the smallest segment of the electronics industry, all other segments depend on its capabilities for success. The advent of COD products will increase the size of the EDA market, because the need to develop software applications for these products will more than make up for the decrease in DFM-tool sales volume. Kablamian also expects that some of the revenue associated with the semiconductor sector will move to the EDA sector, as vendors in this sector enter the SIP (semiconductor-intellectual-property) market. SIP is a new term that replaces "hard macro" to describe cores that are sold only in the "ready-to-manufacture" format. The advantage of SIP is that the foundry has already proved its manufacturability; thus, system architects can integrate it into designs without worrying about yield issues. SIP vendors will need to provide behavioral models of the cores, and both TenisonEDA and Carbon Design offer tools that generate executable models that they can distribute yet still safeguard the IP value of the original design.

The major shift in the distribution of revenue that vendors generate from their products will be the growth of front-end tools at the expense of back-end tools. Gary Smith, chief analyst at Dataquest, predicted a few years ago that the ESL market was ready to expand and diversify. The increase in design complexity requires engineers to work at a level of abstraction higher than RTL, and foundries must take greater control of back-end transformations for different but just as important complexity reasons. The complexities of optimizing a design for manufacturing will require that the often-promised RTL handoff become a standard. Few



**Figure 3** A number of APUs (application-processing units) will in the coming years constitute most of the fabric ICs.




foundries are now willing to support this method, because many customers still believe that they have to participate directly in the layout of a chip. But it is becoming clear that, once designers verify the functional characteristics of a design at the abstraction level required for input to physical synthesis, engineers familiar with manufacturing issues can better handle synthesis and place-and-route functions. The foundries, not the system houses, have the best talent for this job. Structured-ASIC devices, by their own nature, require an RTL handoff.

Behavioral synthesis is also undergoing a change. First, the industry has been wrong in its use of “behavioral.” According to Merriam-Webster’s ([www.merriamwebster.com](http://www.merriamwebster.com)) online dictionary, “behavior” has three principal definitions, all involving an animated subject, either human or animal. Hardware does not behave; it operates. Vendors should call tools that transform the description of an algorithm into its hardware implementation “*algorithm*” synthesis. This area is showing great promise in the area of DSP design, using as input The MathWorks’ Matlab and Simulink models, not the traditional HDL models. For many years,

designers have used these tools to develop DSP algorithms and have then had to re-enter the design using Verilog or VHDL to synthesize the design. Accelchip pioneered the use of Matlab as the input to DSP synthesis, Catalytic followed, and Synplicity has now introduced tools that produce gate-level representations of the design directly from Matlab and Simulink descriptions.

Verification is still a major concern, in spite of advances in formal-verification technology. Jasper Design has increased the scope of formal verification by addressing the verification of the specification for a design, not its implementation. To better support functional verification, Mentor Graphics has introduced a scalable verification product that supports digital, analog, mixed-signal, and hardware/software simulation environments; Cadence offers its multilingual Incisive verification platform; and Synopsys is leading the introduction of SystemVerilog as the language of choice for electronic-system-design exploration. CoWare is trying to take advantage of its

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leading position in the SystemC market, but the language suffers from its limited ability to properly simulate asynchronous and concurrent hardware events, so engineers can use it only to develop a subset of digital designs. EDA companies will need to make a focused effort to understand the verification requirements of software engineers to take advantage of the

growing percentage of software content in system solutions. Because many of the consumer applications that are powering and will power the growth of the electronic-system market depend on unplugged connectivity, companies that specialize in RF design, such as AWR and Agilent Eesof, can play a significant role in expanding EDA revenues.

Both the FPGA and the structured-ASIC markets will increase at the expense of traditional ASICs with process geometries smaller than 90 nm. Although Xilinx is concentrating solely on FPGA development, Altera has entered the structured-ASIC market. The manufacture of FPGA is under control of the vendors, and the device structure is regular. Therefore, as soon as designers develop and verify a process, engineers can use it to produce FPGA devices. Designers will thus enjoy the benefit of having at their disposal programmable devices that offer increasing capacity and speed. Tools to develop FPGA-based systems will be as complex as those they use today to develop ASICs. Thus, it will become increasingly less desirable for FPGA vendors to develop their own proprietary tools, with the exception of place-and-route tools. Traditional EDA vendors, such as Mentor and Synplicity, have proved that this market is profitable. Synopsys is once again trying to gain a share of the market, and new entrants, such as Celoxica, Accelchip, and Catalytic, are introducing technology for FPGA designs. Although the growth of ASIC tools is slowing and will eventually reverse direction, new application areas are becoming feasible. EDA will change as will the nature of its customers but will continue to grow its overall market. □

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