



What does the ADC SNR mean?

HEAR AGAIN AND AGAIN that an ADC's ideal SNR is $6.02N+1.76$ dB (excluding delta-sigma converters). At the beginning of my career, I had to take this scenario at face value, because there were a lot of other, more im-

portant things I needed to know. But now that I am older and wiser, it's time to answer two important questions about the SNR specification: Where does this ideal formula come from, and how do you measure SNR with a real ADC?

SNR is a calculated value that represents the ratio of rms signal to rms noise. You then multiply the \log_{10} of this ratio by 20 to derive SNR in decibels. As I mention above, an ADC's ideal SNR equals $6.02N+1.76$ dB, where N is the number of bits.

You derive this formula by first defining the rms signal. Assuming that the input signal is sinusoidal, the rms signal equals the converter's full-scale range divided by $\sqrt{2}$. If the ADC has a gain of 1, you can also translate this SNR equation into bits: rms signal = $(2^{(N-1)} \times q) / \sqrt{2}$, where q is the LSB size.

All ADCs have rms noise that the quantization error generates. The noise from this error equals $q/\sqrt{12}$. This equation deserves an explanation.

The uncertainty of any ADC bit is $\pm 1/2$ LSB. Of course, this scenario is true for a perfect converter with no differential-nonlinearity errors. The trick is to determine the rms value of 1 LSB. If you assume that the response of this error is triangular across an analog-input signal, the rms value of the triangular signal equals the

magnitude of the signal divided by $\sqrt{3}$. So, if you work the math: rms noise = $\pm (\text{LSB}/2) / \sqrt{3} = q / \sqrt{12}$.

Now, combining these elements:

$$\text{SNR (dB)} = 20 \log \frac{\text{rms SIGNAL}}{\text{rms NOISE}} = 20 \log \left(\frac{2^{(N-1)} \times q / \sqrt{2}}{q / \sqrt{12}} \right) = 6.02N + 1.76 \text{ dB.}$$

Now that you know how to calculate the ideal SNR, you can work on the second question. You calcu-

late the real SNR of an ADC using the fundamental input signal and the FFT bins that contain noise. **Figure 1** shows the FFT plot of a 12-bit ADC with an input signal of 9.9 kHz. With the actual test, the noise on the sinusoidal input signal should be more than three times lower than the ADC's theoretical ideal noise. If this situation is true, the rms signal equals the signal magnitude divided by $\sqrt{2}$.

You calculate the noise from the converter using the measured magnitude of the bins in **Figure 1**. The bins that you exclude from the SNR calculation's denominator are the fundamental input signal and

YOU CALCULATE THE REAL SNR OF AN ADC USING THE FUNDAMENTAL INPUT SIGNAL AND NOISE BINS IN AN FFT PLOT.

its multiple frequencies (or harmonics), such as 19.8 kHz, 29.7 kHz, and so on. You calculate the converter's rms noise by taking the magnitude of each of these bins, squaring it, adding all of the squared bins together, and then calculating the square root of that summation, or the square root of the sum of the squares. Point C in **Figure 1** shows the data's calculated SNR from this 12-bit converter. This real-world analysis shows an SNR of 72 dB, which is close to the ideal value of 74 dB.

The above scenario sheds some light on the mysterious formula for ADC SNR. Now, you can also verify the goodness or badness of your converters in the lab. And, now that I've answered some of these questions, I am curious. What nagging problems are you interested in solving? □

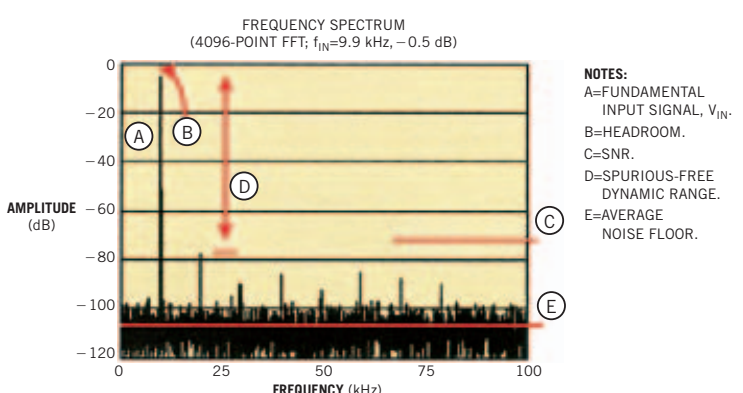


Figure 1 An FFT uses sampled data from an ADC. In this FFT plot, there are 4096 samples that the converter acquires at a data rate of 200k samples/sec. The SNR (Point C) in this plot is a calculated value.

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