Edited by Bill Travis

Circuit produces variable numbers of burst pulses

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THE ADD-ON CIRCUIT in **Figure 1** can produce one to 15 burst pulses with the same number of spaces between the bursts at a pulse width (frequency) that an external square-wave generator at the input sets. The add-on circuit produces a variable number of bursts and a variable number of spaces between the bursts by using an external square-wave generator as a source. The project in this design required a TTL burst signal, but resources did not allow for the expense of a burst generator. The circuit basically comprises two hexadecimal, divide-by-16 counters set up so that the counter on the left produces a user-selectable zero to 15 pulses and the counter on the right produces a user-selectable zero to 15 spaces. The two hexadecimal thumbwheel switches select the number of pulses and spaces.

Counter IC_1 controls the number of bursts, and counter IC_2 controls the number of spaces. The two hexadecimal thumbwheel switches, S_1 and S_2, select the count value. Each switch position is numbered zero to 15. S_1 controls the number of burst pulses, zero to 15, and S_2 controls the number of spaces, zero to 15. For either the IC_1 or the IC_2 counter to count, Pin 7 must be high. If Pin 7 is low, then the counter remains disabled. For a counter to be loaded with a desired count, Pin 9 must be low and then high. The carry output at Pin 15 is normally low until the counter reaches a count of 15, and then it goes high. When the circuit is powered on, resistor R_1 and capacitor C_1 form an RC-time-constant power-on-reset circuit at Pin 1. This feature initializes the counters to the zero state upon power-up. After that, the thumbwheel switches set the count value.

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When a clock signal arrives at the counters' Pin 2 with the desired frequency, counter IC_1 starts counting up, and counter IC_2 remains in the off-state because the low signal at IC_1's Pin 15 carry output applied to IC_2's Pin 7 disables counter IC_2. When IC_1's count reaches the end (15), it goes high and enables IC_2 to count. IC_1's carry output also goes through inverter gate IC_{3A} and then to the OR gate IC_4's Pin 1. The low signal on one input of IC_4—and the fact that, because IC_2 is now counting, its carry output at Pin 15 is also low at IC_4's Pin 2—means that a low signal appears at IC_1's Pin 7, and thus IC_1 now becomes disabled. Both IC_1 and IC_2 counters' Enable pins are cross-con-

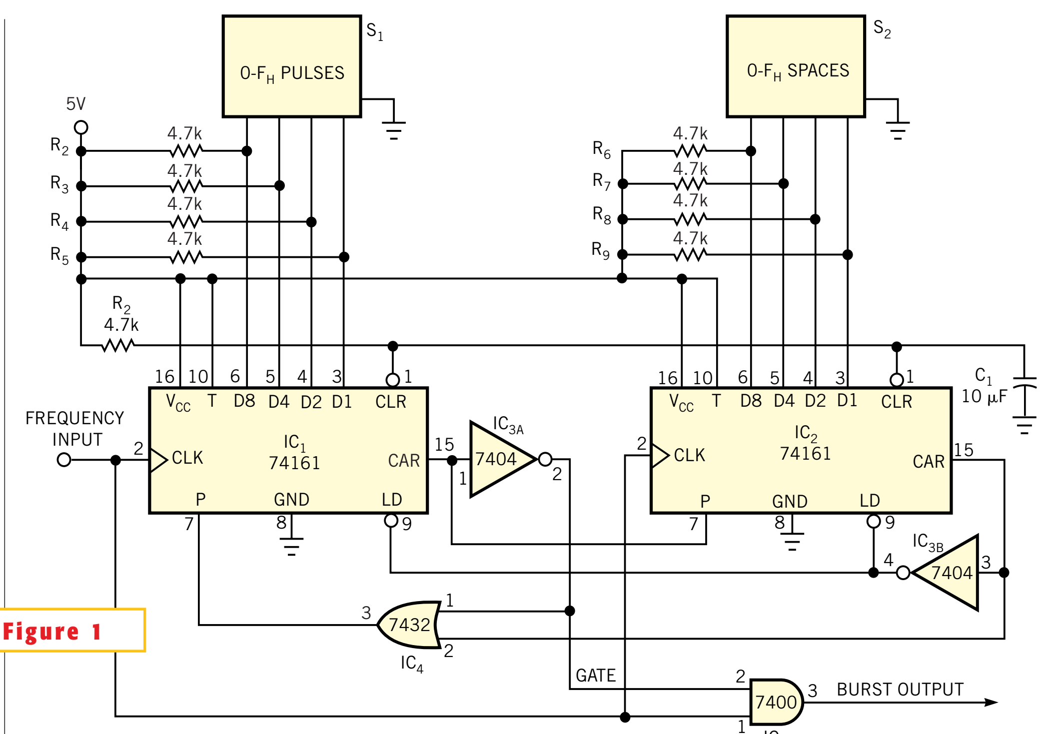

Figure 1

This circuit produces a variable number of burst pulses and spaces.

nected, so that when one counter is counting, the other counter becomes disabled. The two counters work in this way, back and forth, counting up to 15 and enabling and disabling each other. And finally for the two counters, when the carry output on IC_2 goes high, the circuit then, after it reaches a count of 15 through the inverter IC_{3B}, loads a new count or reloads the old count into the counters as set by the thumbwheel switches for the next count.

When IC_1 is counting, the output of IC_{3A} (the gate signal), assumes a high level at AND gate IC_5's Pin 2. This state allows the clock signal to pass through IC_5 unimpeded to the output. The output of IC_5 is the burst output. When IC_1 is disabled and IC_2 is counting, the gate signal from IC_{3A} asserts a low signal at IC_5's Pin 2. The output is also low and produces no bursts. You can configure this circuit to produce even more pulses or spaces by simply cascading more counter chips where needed. Also, you can replace switches S_1 and S_2 by an 8-bit write-output register, making the pulse and space counts software-controlled, or you could apply the gate signal to the control input of a CMOS switch to burst analog signals, such as sine waves at its input.□

Method provides fast, glitch-free isolation of I²C and SMBus signals

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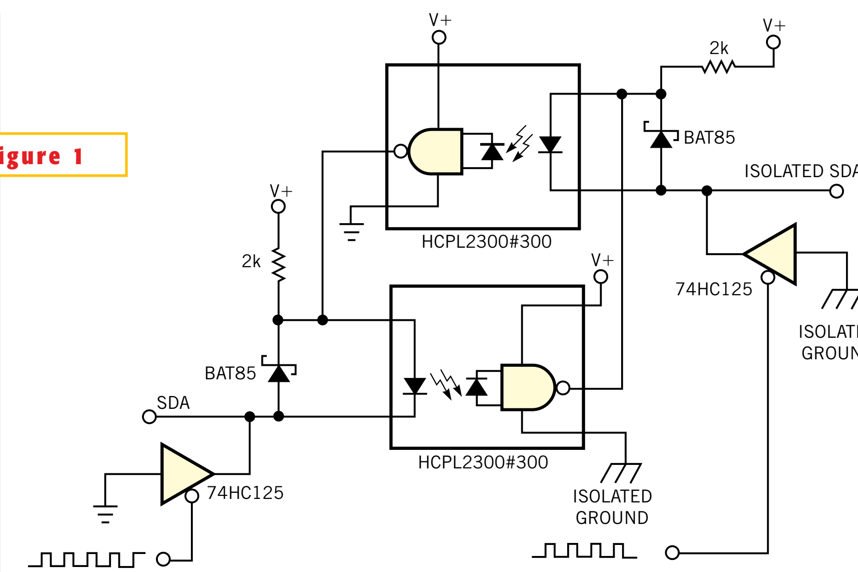
I²C IS A POPULAR SERIAL protocol for power controllers, ADCs and DACs, EEPROMs, and other devices. In certain data-acquisition and power-control situations, you must isolate the I²C master from one or more slave devices for noise, grounding, or safety issues. Also, although 128 peripherals may connect to the bus, at some point, differences in ground potential and excessive bus capacitance begin to erode noise and timing margins. This Design Idea shows how to provide fast, glitch-free optical isolation of I²C or SMBus signals by using a method that meets the requirements for the 400-kHz enhanced-I²C-bus specification. The I²C bus consists of bidirectional clock and data lines (SCL and SDA) that are pulled up with resistors or current sources. Devices connect to the bus with open-collector I/O pins. One way to isolate I²C signals is with a variation of the circuit shown in **Figure 1**, which shows only SDA; SCL operation is identical.

Figure 1



This circuit represents a simple I²C isolator.

The circuit in **Figure 1** works on the principle that a device pulling the nonisolated SDA line low turns on an optocoupler LED, pulling the isolated SDA line low and disabling the isolated side's optocoupler LED and vice versa. However, if devices on both sides of the isolation barrier are pulling their respective SDA lines low, the optocouplers are in an indeterminate state, with both LEDs partially on. When the nonisolated device releases its SDA line, the voltage on the line rises until the isolated side's LED can turn fully on. Only then will the nonisolated SDA line go low again. This situation occurs at various times during I²C communications, including clock synchronization (on the SCL line), multimaster arbitration, and SMBus interrupt arbitration (on the SDA line). **Figure 2** shows details of the operation of the circuit in **Figure 1**. The 74HC125 tristate noninverting buffers simulate the open-drain outputs of two I²C devices. A logic low on the $\overline{EN}$ line forces the output low, and a logic high puts the output in a high-impedance state. Traces 1 and 2 show the inputs to the enable lines of the SDA and isolated-SDA buffers. Traces 3 and 4 show the outputs, respectively.

This type of circuit has been published in a number of forms, often with slow optocouplers that require 5 to 10 mA of LED drive. These circuits may work in a limited set of applications, but they are slow and still produce glitches, and trying to overcome speed and drive issues with high-speed components makes the circuits almost unusable. The circuit in **Figure 1** uses fast HCPL2300 optocouplers that require only 500 μA of LED drive. If both SDA lines are held low and then released at the same time, the optocouplers fight each other and form an oscillator (**Figure 3**). The characteristics of this oscillation depend on

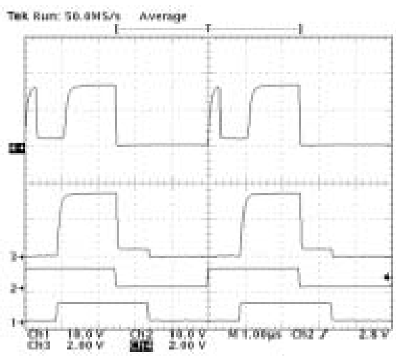


Figure 2 The simple I^{2}C isolator produces large glitches under some circumstances.

pullup resistance, supply voltage, and capacitance on the data lines. (Removing one of the 9-pF scope probes stops the oscillation, and replacing it with a 10-pF capacitor starts it up again.)

The circuit shown in **Figure 4** solves these problems by setting up three logic levels: "high" (pulled up to 5V), "pulling low," and "being pulled low." When both sides are idling high, both optocouplers are off. When one side pulls its line below 0.4V (a safe assumption for both open-collector and open-drain outputs), the comparator turns on its LED. The other side's line pulls down to approximately 0.6V, which is still interpreted as a logic low but does not result in that side's LED turning on. When both sides are pulling their lines low, both LEDs are on. In this state, if one side releases its line, it rises cleanly from the low level of the I^{2}C device's output to approximately 0.6V.

Figure 5 shows details of the operation of the circuit in **Figure 4**. The combination of the LT1719 compara-

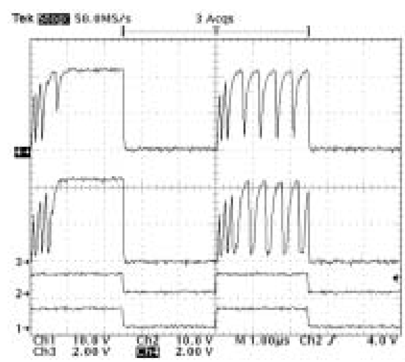


Figure 3 Using high-speed components in Figure 1's circuit causes unpredictable behavior.

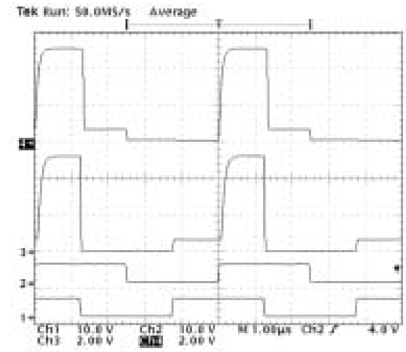


Figure 5 This scope photo shows the operation of the improved I^{2}C isolator.

tor and Agilent (www.agilent.com) HCPL2300 optoisolator meets the timing requirements of the 400-kHz enhanced I^{2}C-bus specification. Total propagation delay is approximately 100 nsec, and you can adjust the logic thresholds to suit other requirements. Although you can use this circuit for both SDA and SCL lines to support full clock synchronization, the extra circuitry is unnecessary as long as the master never tries to communicate faster than the slowest slave device. If you don't need clock synchronization, you can use a single optocoupler for SCL.□

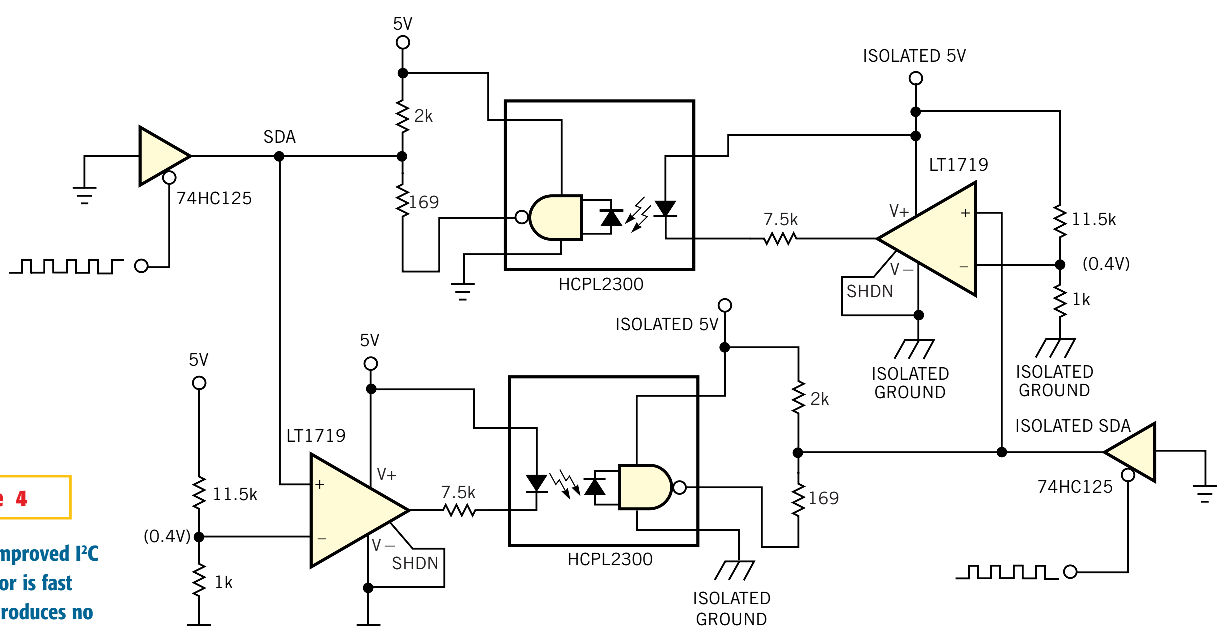


Figure 4 The improved I^{2}C isolator is fast and produces no glitches.

Simulate input-offset current for current mirrors

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Simulating the output-offset current of a current mirror is straightforward. You simply have to apply an input current, measure the output current, and calculate the difference. This output-offset current, however, is not equal to the input-offset current, especially when the circuit is not a 1-to-1 mirror. Simulating the input-offset current with high accuracy is more complicated. Suppose you're dealing with a 1-to-1 mirror and you want to know what input current is needed to obtain an output current of 10 μA. Ideally, the input current would be 10 μA, assuming that the input offset current is zero. However, because of the finite beta of bipolar transistors, finite output impedances, mismatches, and so on, the input offset current is not equal to zero. The design in **Figure 1** provides high accuracy and a low simulation time.

You use feedback to force the current of a CCCS (current-controlled current source) to equal the input-offset current. The current that flows into voltage source V_{OUT} is the difference between the output current of the mirror and the ideal output current. This current is the "error current" (I_{ERROR}). When the CCCS equals the input-offset current, then the error current is zero. The high-gain CCCS amplifies the error current, and the CCCS adds to the input current. In this way, you create a feedback loop, and the current that you measure through the CCCS is the input-offset current. The feedback loop implements a high gain that ensures a high accuracy (negligible error current). And, because you obtain the result by calculating the dc operating point, the simulation time is small.

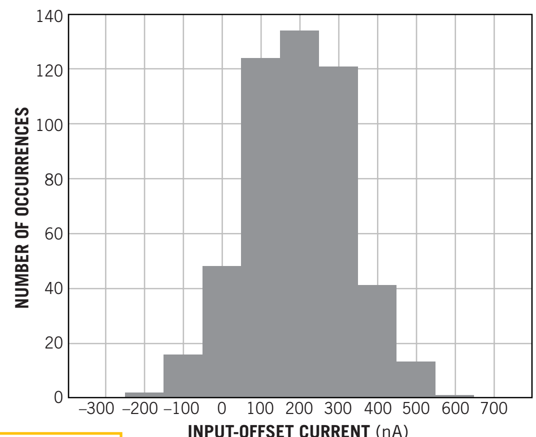

Figure 2

This bar graph shows the input offset-current distribution.

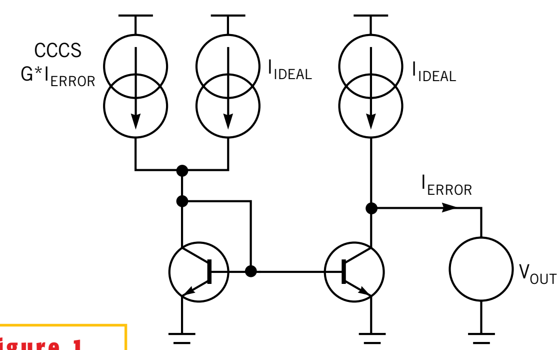

Figure 1

Use this circuit for simulation of current-mirror input-offset currents.

Figure 2 shows simulation results of 500 Monte Carlo runs for $I_{IDEAL}=10$ μA, gain G=1000, and $V_{OUT}=1V$. The npn transistors have an emitter length of 40 microns and use a 0.35-micron silicon-germanium BiCMOS process, but you can use the simulation method for all current mirrors and all types of transistors. The average of the distribution in **Figure 2** is 194 nA, and the standard deviation is 131 nA. The average is not zero because of the base-current error.□

Designing high-current chokes is easy

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Somewhat unusually, this Design Idea deals with a formula rather than a circuit. You might think that all the basic formulas of magnetic phenomena were discovered more than a century ago. In fact, they probably were, but, at the time, some were of little practical interest and were essentially disregarded and never included in books or formula tables. I developed the formula describe here because I had to design many inductive components subjected to high peak currents, such as dc filter chokes, ac reactors for resonant converters, and flyback transformers. In such cases, you have to consider two main aspects: One is the current-carrying capacity of the wire, and the other is the peak induction that the core material supports. The first point is well-known and relatively easy to deal with, but the magnetic induction is much more problematic to determine.

The traditional methods of selecting a suitable core size and air gap are generally based on tables or graphical information. Examples of such methods include Hannah curves and energy-storage-capacity graphs. I found these methods cumbersome, inflexible, and almost impossible to automate; hence, I looked for a better approach. I wanted a formula as compact and elegant as the one that is at the base of a symmetrical converter's design: $N=V/(4BFA)$, where N is the number of turns required to achieve the target induction, V is the voltage applied to the winding in volts, B is the peak magnetic induction in the core material in tesla, F is the frequency of operation in hertz, and A is the effective core area in square meters.

This formula is attractive because you need only essential parameters; you need not mess around with the permeability or the length of the magnetic path, for example. By combining and algebraically manipulating the fundamental equations of the magnetic formula, I arrived at a similarly simple equality applicable to inductors: $N=(LI)/(BA)$, where L is the inductance in henries, and I is the instantaneous peak current in amperes. Here again, you need no more parameters than the bare minimum. Using this formula, a typical design procedure is:

1. Select a core size that seems likely to suit your application (The selection information that the manufacturer provides can be useful.)
2. Use the formula and the core's data sheet to compute the number of turns required for the worst-case situation—in other words, the maximum peak current and magnetic induction below the saturation limit for the whole temperature range.
3. Check that the resulting winding does not exceed the capacity of the coil former; if it does, select the next-higher size.
4. Compute the air gap required to achieve the target inductance using the manufacturer's data or the following formula (approximate):

$$\Delta = \frac{A}{\dfrac{L}{\mu_0 N^2} - 3k\sqrt{A}},$$

where μ_0 is the permeability of a vacuum ($4\pi \times 10^{-7}$), and k is a factor that depends on the implementation of the air gap. For a single air gap, as in a potentiometer core in which the center pillar is machined, $k=2$. If, instead, you use spacers such as in a U-core, the air gap is split in two, and the factor $k=1$. If you need high accuracy for the inductance value, you should build a sample to optimize the gap. Also, for small or large gaps, the formula loses its accuracy because it assumes that the magnetic material has a negligible reluctance compared with the air gap. If the gap is small or if the core material has a low permeability, the assumption about negligible reluctance is no longer true. At the other extreme, the first-order term of the formula does not sufficiently compensate for the apparent increase in the core area that fringe fields cause. Thus, discrepancies can exist between the calculated and the measured values.

The relationship $N=(LI)/(BA)$ can also be useful in a different manner. You may want to reverse-engineer off-the-shelf components to check that they do not risk saturation at the intended peak current. (In converter circuits, the peak current can be much higher than the rms current.) To do this reverse-engineering, you can use the form $B=(LI)/(NA)$. For most general-purpose ferrites, a peak induction of 0.2 to 0.25 tesla is acceptable, whereas materials for power applications can tolerate more than 0.4 tesla. Metal-powder cores accept inductions as high as 1 tesla. If you want to know what maximum current is acceptable for a component, then the following form is convenient: $I=(BNA)/L$. At first sight, this formula looks counterintuitive or even erroneous, because it seems to imply that you can increase the current for a given induction if you also increase the number of turns. How can this situation be?

Increasing the current or the number of turns results in an increase in ampere-turns that the core sees, which should also increase the induction. The key to understanding this apparent paradox is to take into account what the formula implies: If L has to remain constant with more turns, the air gap must be wider to reduce the apparent permeability (μ) of the core, resulting in a greater current capacity, although the air gap appears nowhere in the formula. The paradox may explain why hardly anyone ever mentions this family of formulas. If you try to superficially make sense of the implications of the formulas, you have to conclude that there must be a mistake somewhere.

You can also apply the results to open-circuit magnetic components, such as cylindrical coils wound on a rod of magnetic material. In this case, the air gap becomes almost as large as the core, yielding two implications: Because the surrounding vacuum or air contributes as much as the core itself to the inductance, you can double the core area the formula uses with respect to the physical value, and, even when saturation does occur, the effect is much less brutal than in a closed magnetic circuit. Second, the simplified inductance formula is no longer valid.

To conclude, the user-friendly versions of the formulas, expressed in more convenient units are: $N=0.01(LI)/(BA)$, with L in microhenries, I in amperes, B in tesla, and A in square centimeters.

And the user-friendly expression for the air gap is

$$\Delta = \frac{A}{7.96\dfrac{L}{N^2} - 0.3k\sqrt{A}},$$

where Δ is in millimeters, A is in square centimeters, and L is in microhenries.□