

Image issue

"As long as we continue to view engineering as about widgets and not about people, we will continue to have a perception problem."

—Geoffrey Orsak, Dean, Southern Methodist University, School of Engineering, on the shortage of US engineering graduates

Programmable servo filters smooth motion control

By Warren Webb

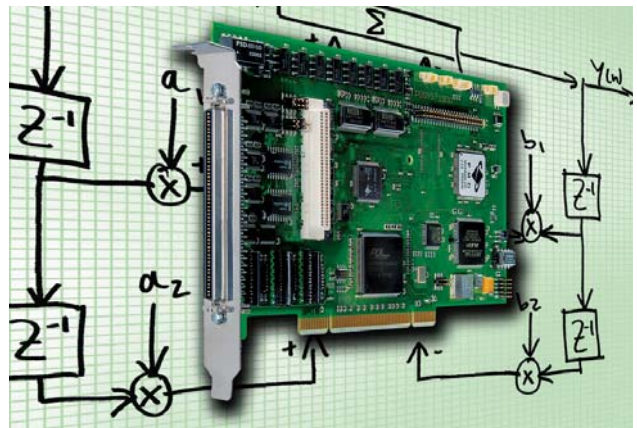
TARGETING MEDICAL, scientific, and general-automation applications, Performance Motion Devices recently announced the Magellan-PCI motion controller with dual biquad filters. Available in one-, two-, three-, and four-axis versions, the high-performance Magellan-PCI motion-control card supports dc brush, brushless, microstepping, and pulse and direction motors. The dual biquad filters can produce two polarities of lowpass output, as well as highpass, bandpass, and notch filters.

Additional features include trajectory generation, servo-loop closure, quadrature-signal input, motor-output signal generation, servo trace, on-the-fly changes, and commutation. The device supplies servo-loop rates as fast as 50

$\mu\text{sec}/\text{axis}$, a 5 million-count/sec quadrature-encoder-input rate, and pulse and direction output as fast as 5 million pulses/sec. The card accepts input parameters, such as position, velocity, acceleration,

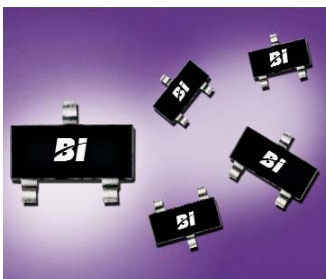
deceleration, and jerk, and automatically generates the programmed trajectory. Magellan-PCI prices start at \$638 (OEM quantities).

► **Performance Motion Devices**, www.pmdcorp.com.



With dual biquad filters at the output of the servo loop, the new Magellan-PCI motion controller delivers reduced resonance, faster transfers, and smoother motion.

Resistor array divides, so design conquers ratio needs



Get precision voltage division using a low-drift, close-tracking ratiometric resistive divider in a two-element SOT-23 or a three-element SOT-143 package.

THE VENERABLE RESISTOR DIVIDER is still a staple of high-precision analog circuits, because it enables measurement architectures that depend not on absolute component values, but only on their ratios, which are more stable. BI Technologies has put a series-connected, two-resistor divider into a three-lead SOT-23 package, forming a precision voltage divider. The ultrastable resistors of the SSI series are available in standard ratios of 1-to-1, 1-to-4, and 1-to-10. Tolerances are as tight as 0.1%, and the more critical temperature coefficient is $\pm 25 \text{ ppm}/^\circ\text{C}$ with tracking tolerance better than $\pm 5 \text{ ppm}/^\circ\text{C}$.

BI fabricated the resistors using nichrome thin-film technology on a silicon substrate. The device's size lets designers place it close to the circuit area of interest, thus "eliminating the need for the long traces and complex routing schemes required for large networks," according to Mike Torres, application engineer and product marketing manager for BI. The SSI series is also available with three resistors in a network in a four-lead SOT-143 package. Prices begin at 30 cents (10,000).

—by Bill Schweber

► **BI Technologies**, www.bitechnologies.com.

Power-industry coalition announces PMBus standard, forms SIG

A COALITION OF POWER-SUPPLY and semiconductor companies led by Artesyn Technologies has released Version 1.0 of the PMBus (Power Management Bus) specification, which defines a

protocol to manage power converters and a power system using communication over the SMBus digital-communication bus. The coalition has also announced the formation of an SIG (special interest group), the SM-IF (System Management Interface Forum), to further develop and promote the PMBus power operating system. The SM-IF comprises the PMBus Implementers Forum and the Smart Battery System Implementers Forum. SM-IF will also take over responsibility for the SMBus.

The SMBus is essentially compatible with the I²C bus, a popular two-wire bus that handles inter-IC control. "The I²C bus is a highly prevalent interface on embedded microprocessors; it's just all over the place," says Michael Stefani, director of product mar-

keting for Artesyn. "SMBus adds an alert line to I²C, making it just a short step from I²C to SMBus."

In addition to Artesyn, the initial coalition comprises Astec Power and semiconductor manufacturers Intersil, Microchip Technology, Texas Instruments, Volterra Semiconductor, Summit Microelectronics, and Zilker Labs (www.astecpower.com, www.intersil.com, www.microchip.com, www.ti.com, www.volterra.com, www.summitmicro.com, www.zilkerlabs.com).

Conspicuously absent from the SIG is Power-One (www.power-one.com), which last year launched its proprietary Z-One bus and in December announced a design, manufacturing, and marketing agreement with C&D Technologies (cdtechno.com). Ac-

ording to Dave Hage, executive vice president of Power-One, "For complex systems, PMBus does not provide a configuration-controlled, standardized programming interface like the Z-One GUI. Lack of standardization in PMBus converters could make the creation and management of a uniform PMBus GUI virtually impossible."

Hage also points out that a bus architecture is overkill and adds too great an expense for some low-end designs. "For low-complexity systems, customers have requested a configurable point-of-load supply that does not require a bus and is more cost-effective." Power-One developed its "no-bus" Z1000 supplies for these applications.

—by Margery Conner

► **Artesyn Technologies**, www.artesyn.com.

► **System Management Interface Forum**, www.power-sig.com.

► **Power Management Bus Implementers Forum**, <http://pmbus.info/specs.html>.

WI-FI CHIP ATTACHES VIA PCI EXPRESS

Broadcom has released what it claims is the first 802.11 wireless-LAN chip that supports the PCI Express bus architecture. The 802.11a/g BCM4311 baseband processor integrates a MAC (media-access controller). The chip's all-CMOS design, high integration, and small footprint provide design flexibility for wireless-enabled notebook PCs, printers, and other client devices, according to Broadcom. "This is a wireless-LAN chip set with our BroadRange technology, which allows devices to hear better in noisier environments with 2- and 5-GHz-band radios," says Brian Bedrosian, Broadcom's senior product-line manager for wireless-LAN clients.

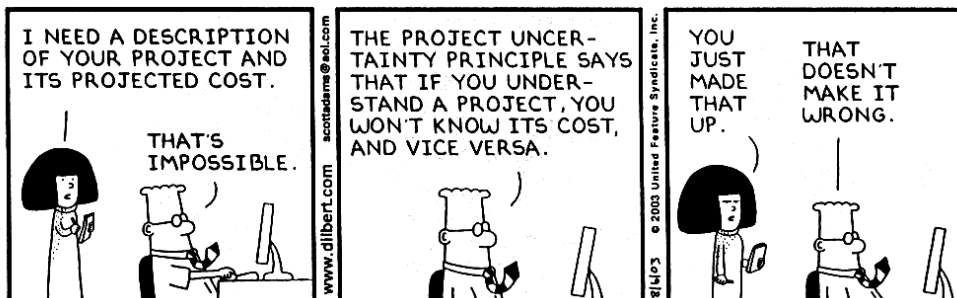
The BroadRange DSP technique allows devices to stay connected at distances as much as 50% farther from a wireless router than previous-generation technologies, according to the company. The chip's lead-free package and more efficient footprint make it a good fit for next-generation PC designs.

The device works with the company's OneDriver software, which offers various features, including SecureEasy Setup software and 125 high-speed mode, to augment the Wi-Fi (wireless-fidelity) network. The software aims to make setup and configuration user-friendly, and the high-speed mode delivers as much as 40% greater throughput than most other 802.11g and 802.11a/g systems. Broadcom's BCM4311, available now in sample quantities, costs \$10 (10,000).

—by Jeff Berman

► **Broadcom**, www.broadcom.com.

DILBERT *By Scott Adams*



► **The No. 1 thing consumers search for when they go to the Ask Jeeves search engine is the name of rival search engine "Google," according to Hitwide Inc, a researcher that analyzes the online activities of 10 million US consumers.**

Midpriced, 1.5-GHz-bandwidth DSOs provide an array of features

ACCORDING TO Boyd Shaw, product manager of Yokogawa Corp of America's Test and Measurement Division, the company's DSOs (digital storage oscilloscopes) are among the best kept secrets in the US electronics industry. Shaw says that YCA's scope sales place it fourth in the United States but that the Japan-headquartered company does far better not only in Asia, but also in Europe. Shaw believes that YCA's US DSO market share will receive a big boost from the introduction of the DL9000 series, which includes four four-channel, 1- and 1.5-GHz-bandwidth real-time-sampling scopes, whose prices start at \$10,995.

In the two-channel mode, the 1-GHz units acquire 5G samples/sec on each channel. (With all channels active, the sampling rate drops to 2.5G samples/sec on each channel.) The 1.5-GHz units can sample twice as fast. At each bandwidth, you can choose between units with maximum memory depth of 2.5 or

6.25M samples/channel.

The scopes provide an impressive array of operational and connectivity features, some of which may be unfamiliar to users of US-manufactured DSOs. For example, most US suppliers have now standardized on color grading to indicate the duty ratio of pixel illumination. YCA, however, is sticking with intensity modulation, not, as you might think, because intensity modulation is less expensive or easier to implement than color grading—in a DSO, it is not—but because many users find intensity-modulated displays more intuitive. In this regard, the DL9000s' intensity-graded displays mimic analog-scope displays in a way that many users are bound to find more informative and user-friendly than color-graded displays.

The DL9000 designs go to great lengths to rapidly acquire lots of waveforms with minimal time between acquisitions and to quickly display the acquired data in the most

meaningful ways. By segmenting memory when the record length is shorter than the full memory depth, the scopes can acquire waveforms with minimal time between acquisitions. One display mode uses the intensity-grading feature to create a single display that overlays the multiple acquisitions. However, all data from each acquisition remains in memory, and you can individually inspect each waveform to search for anomalies. If the accumulated length of all waveforms exceeds the memory depth, the unit discards the oldest acquisitions from the FIFO memory.

Other features include both front- and rear-panel USB ports, an optional 100Base-TX/10Base-T Ethernet interface, a trigger-comparator output for use with external equipment, a go/no-go output for use in production testing, an optional built-in strip-chart recorder, and two PCMCIA slots. (By installing an appropriate card in one of these slots, you can add an IEEE 488 interface.) The units have many built-in filtering and statistical functions. Unlike most Windows-based DSOs, these scopes run under a ROM-resident version of Windows CE. Shaw says that the results are faster start-up, greater operational stability, and more room for your data on the optional 20-Gbyte internal hard drive.

—by Dan Strassberg

► **Yokogawa Corp of America**, 1-770-254-0400, www.yokogawa.com/us/.

VOIP-ADAPTER DESIGN BOASTS \$6 PRICE

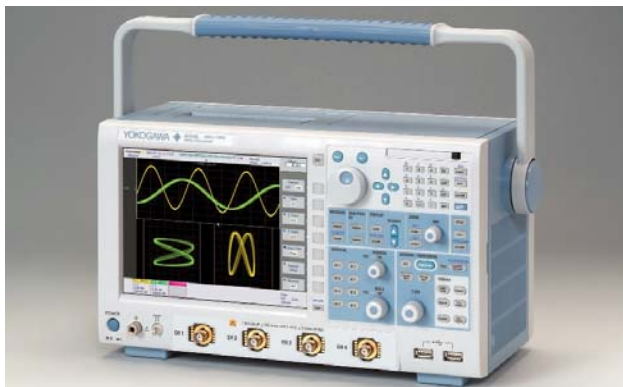
Telecommunications and networking vendor Vocal Technologies has rolled out a line of VOIP (voice-over-Internet Protocol) ATA (analog-telephone-adapter) designs, including a simple ATA with a \$6 BOM (bill-of-materials) cost and a full-motion IP video-telephone with a \$30 BOM.

The designs employ DSP resources and thereby eliminate the need for an additional RISC processor, according to the company. The adapter design offers a single PSTN (public-switched-telephone-network) port and connects to a PC via USB. The design supports two telephone lines, two Ethernet lines, and a PSTN "life-line" port for automated voice-service switching in the event of a power outage or a network disconnection.

John Blume, Vocal's chief executive officer, says that these designs reduce the number of common building blocks and components necessary for developing ATAs. "Our approach to ATA is different from many others, because we eliminate the RISC processor, which, in turn, drives down the BOM for designers," Blume says. When developing its designs, Vocal looked at alternatives using both DSPs and RISC processors and found that a recent-generation DSP is suitable for running the entire application. "The idea here is to take away most of the mystery for designers and suppliers, so that they have what they need," Blume says.

—by Jeff Berman

► **Vocal Technologies**, www.vocal.com.



DL9000 series scopes do a few things that some other DSOs can't do. For example, DL9000s can display Lissajous figures (lower half of the screen).

► According to a recent report from IBM, 76% of all e-mails in February 2005 were spam, down from a summer 2004 peak of nearly 95%.

Structured ASIC offers memory-for-logic swapping

CONFIGURABLE-CORE and structured-ASIC vendor eASIC Corp and its partner Flextronics Semiconductor have released a structured ASIC that allows users to configure the amount of logic, memory, and reprogrammable logic they need for a given design. The company's executive vice president for marketing, Ronnie Vasishtha, says that the new FlexASIC

called eCells (embedded cells), surrounded by embedded-SRAM blocks, PLLs, an 8051 microcontroller, and ROM blocks. Configurable I/O surrounds all of these blocks. The FlexASIC architecture allows users to swap eCells for extra SRAM if a design requires. For example, the biggest device in the FlexASIC family, the FA3000, boasts 3 million ASIC gates in the form of 92,000 eCells, or 194,000 LUTs, plus 2.8 million bits of embedded single-port SRAM.

Designers can configure some eCells after fabrication to reprogrammable-logic blocks. The companies program a device's eCells, RAM, and embedded RAM during fabrication using "e-beam" technology, which customizes the vias between the sixth and seventh layers of the eight-layer process. The routing customization differs from programming the logic and programmable-logic blocks. The companies use a bit stream for this programming and can reload the blocks for debugging after fabrication.

The companies also built a clock tree into the fabric, which means that users need not build it but also that they can't adjust it. The companies offer users two design flows to configure and program the devices. Using the first flow, designers feed a Verilog or VHDL netlist into Synopsys' (www.synopsys.com) Design Compiler, which creates a gate-level netlist. Users then perform chip-resource allocation, assigning memory, clocks, and I/O on the design. Then, using a proprietary eTools suite, users perform mapping, placement, and, with technol-

ogy from OEM Golden Gate Technology (www.ggtcorp.com), global routing. Users then perform final routing, finishing, and BIST (built-in self-test) with eASIC tools. They can use any vendor's tool to perform ATPG (automatic-test-pattern-generation) testing. With the second flow, users feed a Verilog or VHDL netlist into an eASIC\Flextronics-only version of Magma's (www.magma-da.com) Blast SA, which incorporates the Aplus physical-synthesis tool. The tool performs synthesis and placement and then feeds into eASIC's router, finishing tools, and BIST. As with the other flow, users can perform ATPG with any vendor's tool.

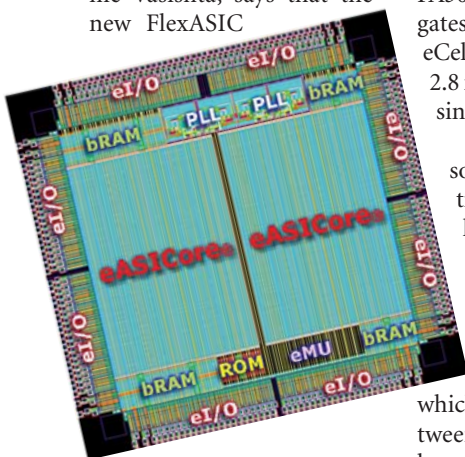
The companies currently fabricate the FlexASIC devices on STMicroelectronics' (www.st.com) 130-nm process. The companies claim that customers incur no NRE charges;

eASIC and Flextronics accommodate low-volume orders because they can implement a number of customers' designs, even if targeting a different part number of the eASIC family, on a single wafer. Vasishtha says that companies have ironed out the lithography and design-for-manufacturing issues. A debugging technology is available, but customers can receive sample silicon as early as two weeks after tape-out so they can test their designs in their systems in real time. Package support for the family ranges from 100-pin TQFPs to 896-pin FBGA packages; eASIC is currently receiving tape-outs from beta customers and expects prototyping silicon by May and production silicon by July.

—by Michael Santarini

►eASIC, www.easic.com.

►Flextronics, www.flextronics.com.



Implemented on 0.13-micron STMicroelectronics silicon, the FlexASIC architecture boasts as many as 3 million ASIC gates, as much as 1.5 Mbits of SRAM, and operation as fast as 400 MHz.

fabric gives users the best of the FPGA and the ASIC worlds: the density and speed associated with ASICs without the NRE (nonrecurring-engineering) costs and the programmability of FPGAs without the power and performance shortcomings. "FlexASIC offers a 25- to 30-times density improvement over FPGAs with power density and performance akin to cell-based design," says Vasishtha, claiming FlexASIC operates at approximately 400 MHz.

The FlexASIC architecture boasts a field of proprietary SRAM three-input LUT (lookup-table)-based logic cells,

Even jacks are getting smarter

THOUGH NOT THE FIRST jacks in audio's history with an auxiliary function, a new series from FCI USA brings the concept to the 38.5-mm-high BTX (Balanced Technology Extended) form factor, as well as to the 38.5-mm-tall jacks for the ATX (Advanced Technology Extended) form factor. The company's Smart Audio Jack series of triple-



stack connectors features an isolated switch so that associated circuitry can detect connector presence and also sense when a microphone, an audio input, or a speaker is plugged into the port. (Some designs use an electronic-circuit technique to make the same determination, but that approach can become complex because the jack must sense a completed—but highly variable and uncontrolled—signal path.)

The color-coded jacks, targeting 192-kbps, high-definition audio designs, have initial 50-mΩ contact resistance and are rated for 1A current and 1000 insertion cycles. Price is 32 cents to 68 cents (1000), depending on configuration.—by Bill Schweber

►FCI USA, www.fciconnect.com.

FPGA development kit targets designs that “race”

MERCURY COMPUTER SYSTEMS has rolled out a development kit supporting the company’s FPGA computing systems that employ its high-speed Race++ switch fabric. The FDK (FPGA Compute Node Developer’s Kit) 2.0 platform, which includes software, IP (intellectual property),

and design consultation, offers the interconnect, communications, command and control, memory, and I/O functions for flexibility and quick deployment, according to the company.

The kit supports the company’s IP cores for the ROC (Race-on-chip) high-bandwidth interconnect, a patent-

pending technology that extends the fabric inside the FPGA to access other IP cores, such as high-speed DRAM, SRAM, sensor-I/O, and system-level fabric interfaces, according to the company. The kit supports the PCI-based VantageRT FCN (FPGA-based compute node) and VME-based MCJ6 FCN

systems. Both of those products feature multimillion-gate Xilinx (www.xilinx.com) FPGAs connected to Race++, which is Mercury’s implementation of the industry-standard Raceway Interlink high-performance interconnect fabric.

Rich Jaenicke, Mercury’s director of product management, says that FDK 2.0 helps users load bit streams into their FPGA and IP, providing an FPGA interface to components such as memories, switch fabric, and I/O. “Users have data streaming from a sensor into an I/O interface and are computing and storing data in memory and sending results over the switch fabric,” Jaenicke says. “We are

providing infrastructure interfaces, which are helpful for our customers, because this approach allows them to focus on algorithms and not have to spend time on infrastructure.” Engineers will also find the kit beneficial because it includes a dual DMA master/slave switch-fabric endpoint. “Switch fabrics are all the rage now, and this IP says that we have the switch fabric and all the protocol layers directly on the chip,” Jaenicke says. FDK 2.0 is available now and costs \$23,000 for the first development seat, which includes 20 hours of development support.

—by Jeff Berman

►Mercury Computer Systems, www.mc.com.

Single-chip FM tuner enables embedded broadcast receiver

WHAT WOULD EH ARMSTRONG SAY? The FM (and super-heterodyne) pioneer never envisioned an all-CMOS, single-IC FM tuner, such as the Si470x series from Silicon Laboratories. This highly integrated, 4×4-mm digital component needs just a bypass capacitor and takes less than 20 mm² of board space overall, far less than the typical approach, which requires a 6×6-mm IC, more than 30 support components, and 150 mm² of space.

The single-chip tuner, the vendor asserts, is the industry’s first all-CMOS device. It simplifies embedding a conventional broadcast FM receiver, spanning 76 to 108 MHz, into a cell phone or an MP3 player, for example, and thus it is “easy and cost-effective to add FM radio as a standard feature to virtually any application,” according to Ed Healy, vice president at Silicon Labs. And, even if you think broadcast radio is dead, many consumers do not; it is increasingly a feature on portable wireless devices.

The Si4700 version needs no alignment. It includes the required filtering, AGC (automatic gain control), a frequency synthesizer with a VCO (voltage-controlled oscillator), a low-dropout amplifier for direct battery connec-

tion, and audio-processing functions. The Si4701 adds an integrated preprocessor for the European RDS (Radio Data System) and the US RBDS (Radio Broadcast Data System) formats at a 57-kHz offset, which adds station ID and song name along with the music and allows alternate-channel (frequency) information, which European radio provides, in which a single broadcaster uses multiple frequencies.

The Si4700 sells for \$3 (10,000), and the Si4701 sells for \$3.50. The companion evaluation board costs \$150.

—by Bill Schweber

►Silicon Laboratories Inc, www.silabs.com.



The all-digital, CMOS Si470x FM tuner does it all and in a 4×4-mm package, allowing designers to easily incorporate broadcast tuning into wireless handheld products.

►Checks accounted for 45% of all payments that were not made with cash in 2003, down from 57% in 2000, and 32% of US households used the Internet to pay bills in some fashion in 2004, according to TowerGroup.