



2004 EDN Microcontroller/Microprocessor directory

32-BIT MICROPROCESSORS

Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/ multiplication hardware support (bits)	FPU	Caching
ARC International www.arc.com	ARCTangent-A4	ARC 32-bit	156 to 183 (0.18) 179 to 247 (0.13)	32	32	1 to 5	0.4mW/MHz (0.18), 0.1mW/MHz (0.13)	Standby, sleep	16/24 and dual 16 MAC, XY memory, modulo, bit-reverse, pre/post-increment, two 32x32 options	Can add	2- to 128-kbyte instruction/data, writeback with LRU, locking, configurable for direct mapped to four-way
	ARC 600	ARCompact	160 to 200 (0.18) 200 to 300 (0.13)	32	16, 32	1 to 5	0.15mW/MHz (0.18), 0.04mW/MHz (0.13)	Standby, sleep, domain clocking	16/24 and dual 16 MAC, XY memory, modulo, bit-reverse, pre/post-increment, two 32x32 options	Can add	2- to 128-kbyte instruction/data, writeback with LRU, locking, configurable for direct mapped to four-way
	ARC 700	ARCompact	266 to 300 (0.18) 400 to 450 (0.13)	32	16, 32	1 to 5	0.-mW/MHz (0.18), 0.15mW/MHz (0.13)	Standby, sleep, domain clocking	Dual 16-bit MAC/MSUB, FFT, Viterbi, 24-bit MAC/MSUB, partial complex multiply, CRC, saturation	Can add	2- to 128-kbyte instruction/data, writeback with LRU, locking, configurable for direct mapped to four-way
	ARCTangent-A5	ARCompact	114 to 164 (0.18) 155 to 230 (0.13)	32	16, 32	1 to 5	0.5mW/MHz (0.18), 0.2mW/MHz (0.13)	Standby, sleep	Dual 16-bit MAC/MSUB, FFT, Viterbi, 24-bit MAC/MSUB, partial complex multiply, CRC, saturation	Can add	2- to 128-kbyte instruction/data, writeback with LRU, locking, configurable for direct mapped to four-way
Sharp Microelectronics of the Americas www.sharpsma.com	LH75400 LH75401 LH75410 LH75411	ARM	84	24/16, 16	16, 32	3.3/ 5 tolerant	70mA	Standby: 45mA Sleep: 4mA Stop1: 3mA Stop2: 35µA	Yes		
	LH79520	ARM	77.4	26/32	16, 32	1.8/ 3.3, 5 tolerant	55mA	Standby: 35mA Stop1: 55µA Stop2: 18µA	Yes		8-kbyte unified
	LH79524	ARM	77.4	32 data	16, 32	1.8/ 3.3, 5 tolerant	85mA	Standby: 50mA Sleep: 3.8mA Stop1: 420µA Stop2: 25µA	Yes		8-kbyte
	LH7A400	ARM	200	26/32	16, 32	1.8/ 3.3, 5 tolerant	147mA	Halt: 43mA Standby: 42µA	Yes		8/8-kbyte instruction/data
	LH7A404	ARM	200	26/32	16, 32	1.8/ 3.3, 5 tolerant	147mA	Halt: 41mA Standby: 70µA	Yes		8/8-kbyte instruction/data
	Altera www.altera.com	Excalibur: EPXA1 EPXA4 EPXA10	ARM V4T	133, 166, 200	32/32	16, 32	1.8, 2.5, 3.3	2W, FPGA dependent	Low power (EPXA1)	32x8 user-definable	Can add in FPGA

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
2- to 512-kbyte ROM, 1- to 128-kbyte XY memory	SRAM		N/A - IP core	Two 32-bit	Up to eight UART, up to eight Ethernet MAC, USB-FS OTG, USB-FS device	Up to 32		N/A (Core)	Add-on AMBA bridge, JTAG to Ethernet debug	License
2- to 512-kbyte ROM, 1- to 128-kbyte XY memory	SRAM, SDR-SDRAM, DDR-SDRAM		N/A - IP core	Two 32-bit	Up to eight UART, up to eight Ethernet MAC, USB-FS OTG, USB-FS device	Up to 32		N/A (Core)	BVCI, AMBA bridge, JTAG to Ethernet debug	License
2- to 512-kbyte ROM, 1- to 128-kbyte XY memory	SRAM, SDR-SDRAM, DDR-SDRAM	Optional	N/A - IP core	Two 32-bit	Up to eight UART, up to eight Ethernet MAC, USB-HS OTG, USB-HS device	Up to 32		N/A (Core)	BVCI, AMBA bridge, JTAG to Ethernet debug	License
2- to 512-kbyte ROM, 1- to 128-kbyte XY memory	SRAM, SDR-SDRAM, DDR-SDRAM		N/A - IP core	Two 32-bit	Up to eight UART, up to eight Ethernet MAC, USB-HS OTG, USB-HS device	Up to 32		N/A (Core)	Add-on AMBA bridge, JTAG to Ethernet debug	License
16-kbyte TCM SRAM, 16-kbyte SRAM	Flash, SRAM, ROM, four-channel DMA, asynchronous glueless interface		144 LQFP	Three 16-bit, PWM, real-time, watchdog	CAN 2.0B, three UART, SPI, Microwire, TI's SSI, 78 PIO	Seven external	Eight channel 10-bit, touchscreen controller	-40 to +85	Color or grayscale LCDC, STN, TFT, Advanced-TFT support	\$7.69 to \$9.34
32-kbyte SRAM	Flash, SRAM, ROM, SDRAM, four-channel DMA	WinCE enabled	176 LQFP	Four 16-bit, two PWM, real-time, watchdog	Three 16550 UART, SPI, Microwire, TI's SSI, 64 PIO	Six external		-40 to +85	Color or grayscale LCDC, STN, TFT, Advanced-TFT support	\$9.96
16-kbyte SRAM	SDRAM, NAND, Flash, four-channel DMA	WinCE enabled	208 CABGA	Three 16-bit with PWM, real-time, watchdog	Three 16C550-type UART, 9-bit capability, IrDA (115 kbit/s); USB 2.0 Full Speed Device	16 vectored, 16 standard (both can be FIQ or IRQ)	10-bit, touchscreen controller, brownout detector	-40 to +85	Color or grayscale LCDC, STN, TFT, Advanced-TFT support, Ten Input, NAND Flash Boot, 10/100 Ethernet	\$12.75
80-kbyte dual-port SRAM (CPU/LCDC)	SRAM, ROM, Flash, SROM, SDRAM, SFlash, 10-channel DMA	WinCE enabled	256 PBGA or CABGA	Three 16-bit, real-time, up to two PWM, watchdog	Three UART, SPI, MicroWire, SSI, AC'97, 60 PIO USB 2.0 Full Speed Device	24, four FIQ, non-vectored		0 to +70 -40 to +85	Color or grayscale LCDC, STN, TFT, Advanced-TFT support, MMC, Smart Card, CompactFlash interface, DC-DC interface	\$14.80
80-kbyte dual-port SRAM (CPU/LCDC)	SRAM, ROM, Flash, SROM, SDRAM, SFlash, 12-channel DMA	WinCE enabled	324 CABGA	Three 16-bit, real-time, up to two PWM, watchdog	Three UART, SPI, MicroWire, SSI, AC'97, device/host USB 2.0 full speed, 64 PIO	32 vectored, 32 standard (both can be FIQ or IRQ)	10 channel 10-bit, touchscreen controller, brownout detector	0 to +70 -40 to +85	Color or grayscale LCDC, STN, TFT, Advanced-TFT support, MMC/SD, Smart Card, CompactFlash interface, DC-DC interface	\$18.77
32- to 256-kbyte SRAM, 16- to 128-kbyte dual-port SRAM	SDRAM, Flash	Dual 64-entry TLB	484/672/1020 FBGA	32-bit, watchdog	Configurable number of UART, up to 170 GPIO, SPI, IDE, PCI, 10/100-Mbps Ethernet	Three modes, six sources, 31 or 63 levels		0 to +70 -40 to +85	4/16/38K FPGA logic elements; two AMBA AHB bus bridges, JTAG debug, ETM9 trace	\$40 to \$500

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ARM www.arm.com	ARM720T	ARM V4T	Up to +100 (worst case)	AHB 32	16, 32	1.2 (0.13)	0.06 to 0.2mW/MHz (0.13)	Yes	Yes		8-kbyte unified
	ARM7TDMI	ARM V4T	Up to 133 (worst case)	AHB 32 (with wrapper)	16, 32	1.2 (0.13)	0.06mW/MHz (0.13)	Yes	Yes		Can add external
	ARM7TDMI-S	ARM V4T	Up to 133 (worst case)	AHB 32 (with wrapper)	16, 32	1.2 (0.13)	0.11mW/MHz (0.13)	Yes	Yes		Can add external
	ARM920T	ARM V4T	Up to 250 (worst case)	AHB 32 (with wrapper)	16, 32	1.2 (0.13)	0.25mW/MHz (0.13)	Yes	Yes		16-kbyte instruction/data
	ARM922T	ARM V4T	Up to 250 (worst case)	AHB 32 (with wrapper)	16, 32	1.2 (0.13)	0.25mW/MHz (0.13 cache)	Yes	Yes		8-kbyte instruction/data
	ARM940T	ARM V4T	Up to 180 (worst case)	AHB 32 (with wrapper)	16, 32	1.8 (0.18)	0.8mW/MHz (0.18 cache)	Yes	Yes		4-kbyte instruction/data
	SC100	ARM V4T	80 (worst case)	32	16, 32	1.8 (0.18)	0.21mW/MHz (0.18 no cache)	Yes	Yes		
	SC110	ARM V4T	80 (worst case)	32	16, 32	1.8 (0.18)	0.32mW/MHz (0.18 cache)	Yes	Cryptography		
	ARM1020E	ARM V5TE	Up to 325 (worst case)	Dual AHB 32 or 64	16, 32	1 (0.13)	0.6mW/MHz (0.13 cache)	Yes	DSP	VFP10 co-processor	32-kbyte instruction/data
	ARM1022E	ARM V5TE	Up to 325 (worst case)	Dual AHB 32 or 64	16, 32	1 (0.13)	0.6mW/MHz (0.13 cache)	Yes	DSP	VFP10 co-processor	16-kbyte instruction/data
	ARM946E-S	ARM V5TE	Up to 215 (worst case)	AHB 32	16, 32	1.2 (0.13)	0.5mW/MHz (0.13 cache)	Yes	DSP	VFP9 co-processor	Configurable 4-kbyte to 1-Mbyte instruction/data
	ARM966E-S	ARM V5TE	Up to 250 (worst case)	Dual AHB 32	16, 32	1.2 (0.13)	0.3mW/MHz (0.13 TCM)	Yes	DSP	VFP9 co-processor	
	ARM968E-S	ARM V5TE	Up to 250 (worst case)	AHB 32	16, 32	1 to 1.2 (0.13)	0.14mW/MHz (0.13)	Yes	DSP		
	ARM1026EJ-S	ARM V5TEJ	266 to 325 (worst case)	Dual AHB 32 or 64	16, 32	1 to 1.2 (0.13)	0.6mW/MHz (0.13 cache)	Yes	DSP	VFP10 co-processor	Configurable 4- to 128-kbyte instruction/data
	ARM7EJ-S	ARM V5TEJ	Up to 133 (worst case)	AHB 32 (with wrapper)	16, 32	1.2 (0.13)	0.16mW/MHz (0.13)	Yes	DSP	Optional VFP9 co-processor	Can add external
	ARM926EJ-S	ARM V5TEJ	Up to 250 (worst case)	AHB 32	16, 32	1.2 (0.13)	0.6mW/MHz (0.13 cache)	Yes	DSP	VFP9 co-processor	Configurable 4- to 128-kbyte instruction/data
	SC200	ARM V5TEJ	110 (worst case)	32	16, 32	1.8 (0.18)	0.30mW/MHz (0.18 cache)	Yes	DSP		Optional
	SC210	ARM V5TEJ	110 (worst case)	32	16, 32	1.8 (0.18)	0.35mW/MHz (0.18 no cache)	Yes	DSP, Cryptography		Optional
	ARM1136JF-S	ARM V6	333 to 400 (worst case)	Quad AHB 64	16, 32	1 to 1.2 (0.13)	0.4mW/MHz (0.13 no cache)	Yes	DSP, SIMD	Yes	Configurable 4- to 64-kbyte instruction/data
	ARM1136J-S	ARM V6	333 to 400 (worst case)	Quad AHB 64	16, 32	1 to 1.2 (0.13)	0.4mW/MHz (0.13 no cache)	Yes	DSP, SIMD		Configurable 4- to 64-kbyte instruction/data
MPCore	ARM V6+	330 to 550 (worst case)	Dual AMBA 3.0 AXI 64	16, 32	1 to 1.2 (0.13)	1.9mW/MHz (0.13 two processor)	Yes	DSP, SIMD	Yes	Configurable: 16- to 64-kbyte per processor	
ARM1156T2F-S	ARM V6T2	330 to 550 (worst case)	Quad AMBA 3.0 AXI 64	16, 32	1 to 1.2 (0.13)	0.75mW/MHz (0.13 cache)	Yes	DSP, SIMD	Yes	Configurable 0- to 64-kbyte	

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Licensee option	Licensee option	MMU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Real-time trace	License
Licensee option	Licensee option		N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Real-time trace	License
Licensee option	Licensee option		N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Real-time trace	License
Licensee option	Licensee option	MMU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Real-time trace	License
Licensee option	Licensee option	MMU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Real-time trace	License
Licensee option	Licensee option	MPU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)		License
Licensee option	Licensee option	Secure MPU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	SecurCore security features	License
Licensee option	Licensee option	Secure MPU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	SecurCore security features	License
	Licensee option	MMU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Real-time trace	License
	Licensee option	MMU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Real-time trace	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option	MPU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Real-time trace	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option		N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Real-time trace	License
Configurable local: 0- to 4-Mbyte	Licensee option		N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Interleaved Data TCM interface	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option	MMU and MPU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Jazelle (Java), Real-time trace	License
Licensee option	Licensee option		N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Jazelle (Java), Real-time trace	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option	MMU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Jazelle (Java), Real-time trace	License
Licensee option	Licensee option	Secure MPU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	SecurCore security features	License
Licensee option	Licensee option	Secure MPU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	SecurCore security features	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option	MMU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Jazelle (Java), multimedia	License
Configurable local: 4-kbyte to 1-Mbyte	Licensee option	MMU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Jazelle (Java), multimedia	License
	Licensee option	MMU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Intelligent Energy Manager, Jazelle (Java)	License
Configurable local: 0- to 128-kbyte	Licensee option	MPU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Thumb-2, cache parity protection, ECC support for TCMs	License

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	ARM1156T2-S	ARM V6T2	330 to 550 (worst case)	Quad AMBA 3.0 AXI 64	16, 32	1 to 1.2 (0.13)	0.75mW/MHz (0.13 cache)	Yes	DSP, SIMD		Configurable 0- to 64-kbyte
	ARM1176JZF-S	ARM V6Z	330 to 550 (worst case)	Quad AMBA 3.0 AXI 64	16, 32	1 to 1.2 (0.13)	0.8mW/MHz (0.13 cache)	Yes	DSP, SIMD	Yes	Configurable 4- to 64-kbyte
	ARM1176JZ-S	ARM V6Z	330 to 550 (worst case)	Quad AMBA 3.0 AXI 64	16, 32	1 to 1.2 (0.13)	0.8mW/MHz (0.13 cache)	Yes	DSP, SIMD		Configurable 4- to 64-kbyte
Cirrus Logic www.cirrus.com	CS89712	ARM720T	74	32	16, 32	2.5/3.3	90mW	Less than 0.03mW, power management			8-kbyte unified
	EP7309	ARM720T	74	32	16, 32	2.5/3.3	90mW	Less than 0.03mW, power management			8-kbyte unified
	EP7311	ARM720T	74, 90	32	16, 32	2.5/3.3	108mW	Less than 0.03mW, power management			8-kbyte unified
	EP7312	ARM720T	74, 90	32	16, 32	2.5/3.3	108mW	Less than 0.03mW, power management			8-kbyte unified
STMicroelectronics www.st.com	STR-ARM 720	ARM720T	66	22/16	16, 32	1.8/3.3		Standby: 200uA			8-kbyte unified
Analog Devices www.analog.com	ADuC7020	ARM7TDMI	45	16	16, 32	2.7 to 3.6	150mW	90µW	Multiply instruction		
	ADuC7021	ARM7TDMI	45	16	16, 32	2.7 to 3.6	150mW	90µW	Multiply instruction		
	ADuC7022	ARM7TDMI	45	16	16, 32	2.7 to 3.6	150mW	90µW	Multiply instruction		
	ADuC7024	ARM7TDMI	45	16	16, 32	2.7 to 3.6	150mW	90µW	Multiply instruction		
	ADuC7025	ARM7TDMI	45	16	16, 32	2.7 to 3.6	150mW	90µW	Multiply instruction		
	ADuC7026	ARM7TDMI	45	16	16, 32	2.7 to 3.6	150mW	90µW	Multiply instruction		
	ADuC7027	ARM7TDMI	45	16	16, 32	2.7 to 3.6	150mW	90µW	Multiply instruction		

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Configurable local: 0- to 128-kbyte	Licensee option	MPU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Thumb-2, cache parity protection, ECC support for TCMs	License
Configurable local: 0- to 64-kbyte	Licensee option	MMU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Intelligent Energy Manager, TrustZone, Jazelle (Java)	License
Configurable local: 0- to 64-kbyte	Licensee option	MMU	N/A - IP core	Licensee option	Licensee option	Yes	Licensee option	N/A (Core)	Intelligent Energy Manager, TrustZone, Jazelle (Java)	License
48-kbyte SRAM	8-, 16-, 32-bit SRAM/Flash/ROM, 32-bit SDRAM	64-entry TLB	256 PBGA	Two 16-bit	10-Mbit Ethernet with integrated PHY, two SSI, IrDA, two UART, two PWM, 27 GPIO	22		0 to +70	LCD controller, 32-/128-bit unique MaverickKey ID, touchscreen interface, glueless digital audio, CODEC interface, JTAG	\$20.37
48-kbyte SRAM	8-, 16-, 32-bit SRAM/Flash/ROM	64-entry TLB	208 LQFP, 256 PBGA, 204 TFBGA	Two 16-bit	Two SSI, IrDA, two UART, two PWM, 27 GPIO	22		-40 to +85	LCD controller, 32-/128-bit unique MaverickKey ID, touchscreen interface, glueless digital audio, CODEC interface, JTAG	\$5.89
48-kbyte SRAM	8-, 16-, 32-bit SRAM/Flash/ROM, 32-bit SDRAM	64-entry TLB	208 LQFP, 256 PBGA, 204 TFBGA	Two 16-bit	Two SSI, IrDA, two UART, two PWM, 27 GPIO	22		-40 to +85	LCD controller, 32-/128-bit unique MaverickKey ID, touchscreen interface, JTAG	\$6.51
48-kbyte SRAM	8-, 16-, 32-bit SRAM/Flash/ROM, 32-bit SDRAM	64-entry TLB	208 LQFP, 256 PBGA, 204 TFBGA	Two 16-bit	Two SSI, IrDA, two UART, two PWM, 27 GPIO	22		-40 to +85	LCD controller, 32-/128-bit unique MaverickKey ID, touchscreen interface, glueless digital audio, CODEC interface, JTAG	\$7.13
16-kbyte RAM, up to 128-Mbyte external SDRAM	Up to 8-Mbyte external	Yes	208 PQFP	Four 16-bit	Two UART, USB, CAN, two Buffered SPI, I2C, ATAPI, DMAC	32, 16 external, 16 levels nesting	Four channel 11-bit	-40 to +85	JTAG port	\$10
62-kbyte Flash/EE, 8-kbyte SRAM	In-circuit download		40 LFCSP, 6x6mm	Four 32-bit	SPI, two I2C, UART, JTAG	24	Five channel 12-bit 1Msps; four 12-bit voltage output DACs	-40 to +85	16-element PLA, voltage comparator, temperature sensor, JTAG based debug	\$7.62
62-kbyte Flash/EE, 8-kbyte SRAM	In-circuit download		40 LFCSP, 6x6mm	Four 32-bit	SPI, two I2C, UART, JTAG	24	Eight channel 12-bit 1Msps; two 12-bit voltage output DACs	-40 to +85	16-element PLA, voltage comparator, temperature sensor, JTAG based debug	\$4.36 to \$6.39
62-kbyte Flash/EE, 8-kbyte SRAM	In-circuit download		40 LFCSP, 6x6mm	Four 32-bit	SPI, two I2C, UART, JTAG	24	10 channel 12-bit 1Msps	-40 to +85	16-element PLA, voltage comparator, temperature sensor, JTAG based debug	\$3.75 to \$5.34
62-kbyte Flash/EE, 8-kbyte SRAM	In-circuit download		64 LFCSP, 9x9mm; 64 LQFP.	Four 32-bit, three-phase PWM	SPI, two I2C, UART, JTAG	24	10 channel 12-bit 1Msps; two 12-bit voltage output DACs	-40 to +85	16-element PLA, voltage comparator, temperature sensor, JTAG based debug	\$7.62
62-kbyte Flash/EE, 8-kbyte SRAM	In-circuit download		64 LFCSP, 9x9mm	Four 32-bit, three-phase PWM	SPI, two I2C, UART, JTAG	24	12 channel 12-bit 1Msps	-40 to +85	16-element PLA, voltage comparator, temperature sensor, JTAG based debug	\$5.45 to \$6.50
62-kbyte Flash/EE, 8-kbyte SRAM	In-circuit download		80 LQFP	Four 32-bit, three-phase PWM	SPI, two I2C, UART, JTAG	24	12 channel 12-bit 1Msps; four voltage-output 12-bit DACs	-40 to +85	16-element PLA, voltage comparator, temperature sensor, JTAG based debug	\$10.60
62-kbyte Flash/EE, 8-kbyte SRAM	In-circuit download		80 LQFP	Four 32-bit, three-phase PWM	SPI, two I2C, UART, JTAG	24	16 channel 12-bit 1Msps	-40 to +85	16-element PLA, voltage comparator, temperature sensor, JTAG based debug	\$5.85 to \$6.90

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Atmel www.atmel.com	AT91M40800 AT91R40008 AT91FR4042 AT91FR40162	ARM7TDMI	Up to 70	26/16	16, 32	1.65 to 1.95/ 1.65 to 3.6	From 60mW	0.2mW, idle, individual peripheral clock enable	Yes		
	AT91M42800A AT91M55800A	ARM7TDMI	33	26/16	16, 32	2.7 to 3.6	230mW	Less than 0.003mW, idle, slow, standby, battery backup, individual peripheral clock enable,	Yes		
	AT91SAM7A1 AT91SAM7A2 AT91SAM7A3	ARM7TDMI	Up to 60	up to 24/16	16, 32	3 to 3.6	50mW	Idle, slow, standby, individual peripheral clock enable	Yes		
	AT91SAM7S32 AT91SAM7S64 AT91SAM7S128 AT91SAM7S256	ARM7TDMI	55		16, 32	3 to 3.6	50mW	Idle, slow, standby, individual peripheral clock enable	Yes		
Oki Semiconductor www.okisemi.com/us	ML671000	ARM7TDMI	24	23/16	16, 32	3.3	60mA	Halt, stop	64-bit MAC		
	ML674000	ARM7TDMI	33	24/16	16, 32	2.5/3.3	35mA	Halt, stop	64-bit MAC		
	ML674001 ML67Q4002 ML67Q4003	ARM7TDMI	33	24/16	16, 32	2.5/3.3	40mA	Halt, stop	64-bit MAC		
	ML675001 ML67Q5002 ML67Q5003	ARM7TDMI	60	24/16	16, 32	2.5/3.3	70mA	Halt, stop	64-bit MAC		8-kbyte unified, four-way set associative, write back
Philips Semiconductors www.philips.semiconductors.com	LPC2000 Family LPC21xx LPC22xx	ARM7TDMI	60	0/32	8	3 to 4		Idle, powerdown			
STMicroelectronics www.st.com	STR-ARM 71x	ARM7TDMI	66	24/16	16, 32	3.3, 1.8 regulator		Stop: 100uA, standby: 3uA			
Atmel www.atmel.com	AT91RM9200	ARM920T	180	26/32	16, 32	1.65 to 1.95/ 1.65 to 3.6	60mW	3mW, idle, slow, standby, individual peripheral clock enable	Yes		16-kbyte instruction/data
Samsung Electronics- www.samsungsemi.com	S3C2410	ARM920T	200, 266	27/32	16, 32	1.8/2/3.3	225mW (1.8V)	Sleep, idle			16-kbyte instruction/data
	S3C2440	ARM920T	300, 400, 533	27/32	16, 32	1.2/1.3/3.3 (1.8/2.5/3.3 memory)	275mW (1.2V)	Sleep, idle			16-kbyte instruction/data

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
Up to 2048-kbyte Flash, up to 256-kbyte SRAM	8- or 16-bit static memory		100 TQFP, 121 BGA	Three 16-bit, watchdog	UART, TWI, USB, SPI, I2S, 32 PIO	32, 8 levels		-40 to +85		\$4.50 to \$13
8-kbyte SRAM	8- or 16-bit static memory		144/176 BGA, 144/176 TQFP	Six 16-bit, real-time, watchdog	UART, SPI, PIO	32, 8 levels	Up to 8 channel 10-bit; two channel 10-bit DAC	-40 to +85		\$5.50 to \$7
Up to 256-kbyte Flash, 4 to 32-kbyte SRAM	8- or 16-bit static memory		100/144/176 TQFP	Nine 16-bit, watchdog, four to eight PWM	One to four CAN, UART, TWI, USB, SPI, I2S, PIO	32, 8 levels	Eight or 16 channel 10-bit	-40 to +85		\$5.50 to \$8
32 to 256-kbyte Flash, 8 to 64-kbyte SRAM			48 /64 TQFP	Three 16-bit, real-time, watchdog, four PWM	UART, TWI, USB, SPI, I2S, 32 PIO	32, 8 levels	Four or eight channel 10-bit	-40 to +85	BOD, POR, High Drive, Security bits, ISP	\$3 to \$6
4-kbyte SRAM	SRAM, DRAM, MASK ROM, Flash		128 QFP	Multifunction, PWM, watchdog	Rx/Tx UART, 16550 UART, USB 2.0 device with PHY, 64 GPIO	13, nine external		-10 to +70	DMA	\$6.50
8-kbyte SRAM, up to 4-kbyte boot ROM	SRAM, DRAM, SDRAM, EDO-RAM, MASK ROM, Flash		128 TQFP, 144 LFBGA	Multifunction, PWM, watchdog	16550 UART, RX/TX UART, 32 GPIO	18, five external	Eight channel 10-bit	-40 to +85	DMA, Selectable clock gears	From \$4
32-kbyte SRAM, up to 512-kbyte Flash, up to 4-kbyte boot ROM	SRAM, DRAM, SDRAM, EDO-RAM, MASK ROM, Flash		144 LQFP, 144 LFBGA	Multifunction, PWM, watchdog	16550 UART, RX/TX UART, SSIO, I2C, 42 GPIO	24, five external	Four channel 10-bit	-40 to +85	DMA, Selectable clock gears	From \$4
32-kbyte SRAM, up to 512-kbyte Flash, up to 4-kbyte boot ROM	SRAM, DRAM, SDRAM, EDO-RAM, MASK ROM, Flash		144 LQFP, 144 LFBGA	Multifunction, PWM, watchdog	16550 UART, RX/TX UART, SSIO, I2C, 42 GPIO	24, five external	Four channel 10-bit	-40 to +85	DMA, Selectable clock gears, PLL	From \$5
Up to 64 K RAM, 256 K Flash			LQFP48, LQFP64 and LQFP144	Up to four, real-time	I2C, two UART, up to four CAN, two SPI	Up to 25, four external	Eight channel 10-bit	-40 to +105	Zero wait state Flash	\$3.25 to \$9.25
256-kbyte Flash, 64-kbyte RAM	External		64, 144 TQFP	Five 16-bit	Two I2C, four UART, two Buffered SPI, CAN, USB, HDLC	32, 16 priority levels	Four channel 12-bit	-40 to +85	JTAG port	\$6.70
16-kbyte SRAM	SDRAM, Compact Flash, Smart Media, NAND Flash, static memory	Yes	208 PQFP, 256 BGA	Six 16-bit, real-time, watchdog	Ethernet, USB Host and Device, MCI, UART, TWI, SPI, I2S, 94 PIO	32, 8 levels		-40 to +85	Real-Time trace	\$13 to \$15
4-kbyte SRAM NAND booting	Flash, SRAM, ROM, SDRAM	Yes	272 FBGA	Four 16-bit	Three UART, two SPI, IIS, I2C, two USB host/device	24 external	Eight channel 10-bit touchscreen	0 to +70 -40 to +85	STN/TFT LCDC, SD/MMC, SMC	
4-kbyte SRAM NAND booting	Flash, SRAM, ROM, SDRAM	Yes	289 FBGA	Four 16-bit	Three UART, two SPI, IIS, I2C, AC97, two USB host/device	24 external	Eight channel 10-bit touchscreen	0 to +70 -40 to +85	STN/TFT LCDC, 4MP CAMERA I/F, SD/MMC, SMC	

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/ multiplication hardware support (bits)	FPU	Caching
Cirrus Logic www.cirrus.com	EP9301	ARM920T	166	16	16	1.8/3.3	550mW	Less than 1mW, power management			16-kbyte instruction/data
	EP9302	ARM920T	200	16	16	1.8/3.3	550mW	Less than 1mW, power management	200-MHz MaverickCrunch	200-MHz Maverick-Crunch	16-kbyte instruction/data
	EP9307	ARM920T	200	32	16, 32	1.8/3.3	550mW	Less than 1mW, power management	200-MHz MaverickCrunch	200-MHz Maverick-Crunch	16-kbyte instruction/data
	EP9312	ARM920T	200	32	16, 32	1.8/3.3	550mW	Less than 1mW, power management	200-MHz MaverickCrunch	200-MHz Maverick-Crunch	16-kbyte instruction/data
	EP9315	ARM920T	200	32	16, 32	1.8/3.3	550mW	Less than 1mW, power management	200-MHz MaverickCrunch	200-MHz Maverick-Crunch	16-kbyte instruction/data
Freescale www.freescale.com	ColdFire family MCF523x	ColdFire	80 to 150	32/24	16, 32, 48	1.5/3.3		Yes	Hardware divide, EMAC		Configurable 8-kbyte
	ColdFire family MCF527x	ColdFire	100 to 166	32/16	16, 32, 48	1.5/3.3 (2.5 DDR)		Yes	Hardware divide, EMAC		Configurable 8- or 16-kbyte
	ColdFire family MCF52xx	ColdFire	25 to 140	32/32 or 16	16, 32, 48	1.8/3.3/5	183mW (MCF5249)	Yes	Hardware divide, MAC/EMAC		Up to 4-kbyte instruction, or configurable 8-kbyte
	ColdFire family MCF5307	ColdFire	66, 90	32/32	16, 32, 48	3.3	950mW		Hardware divide, MAC		8-kbyte unified
	ColdFire family MCF5407	ColdFire	162, 220	32/32	16, 32, 48	1.8/3.3	670mW		Hardware divide, MAC		16/8-kbyte instruction/data
	ColdFire family MCF548x MCF547x	ColdFire	166, 200, 266	32/32	16, 32, 48	1.5/3.3 (2.5 DDR)		Yes	Hardware divide, EMAC	Yes	32/32-kbyte instruction/data

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
	8-, 16-bit SRAM/Flash/ROM, 16-bit SDRAM, EPROM, 12-channel DMA	64-entry TLB	208 QFP	Two 16-bit, 32-bit, 40-bit, watchdog	Two SSI, IrDA, six I2S, SPI, two UART with HDLC, two PWM, two USB 2.0 Host, AC'97, 10/100 Ethernet MAC, 24 GPIO	64	12-bit	-40 to +85	32/128-bit unique MaverickKey ID, glueless digital audio, CODEC interface	\$8.86
	8-, 16-bit SRAM/Flash/ROM, 16-bit SDRAM, EPROM, 12-channel DMA	64-entry TLB	208 QFP	Two 16-bit, 32-bit, 40-bit, watchdog	Two SSI, IrDA, six I2S, SPI, two UART with HDLC, two PWM, two USB 2.0 Host, AC'97, 10/100 Ethernet MAC, 24 GPIO	64	12-bit	-40 to +85	32/128-bit unique MaverickKey ID, glueless digital audio, CODEC interface	\$9.96
	8-, 16-, 32-bit SRAM/Flash/ROM, 32-bit SDRAM, EPROM, 12-channel DMA	64-entry TLB	272 TFBGA	Two 16-bit, 32-bit, 40-bit, watchdog	Two SSI, IrDA, six I2S, SPI, three UART with HDLC, two PWM, three USB 2.0 Host, AC'97, 10/100 Ethernet MAC, 8x8 Keypad, 65 GPIO	64	12-bit	-40 to +85	CRT/LCD/NTSC/PAL display controller, touchscreen interface, 32/128-bit unique MaverickKey ID, glueless digital audio, CODEC interface	\$12.74
	8-, 16-, 32-bit SRAM/Flash/ROM, 32-bit SDRAM, EPROM, 12-channel DMA	64-entry TLB	352 PBGA	Two 16-bit, 32-bit, 40-bit, watchdog	Two SSI, IrDA, six I2S, SPI, three UART with HDLC, two PWM, three USB 2.0 Host, AC'97, two IDE, 10/100 Ethernet MAC, 8x8 Keypad, 65 GPIO	64	12-bit	-40 to +85	CRT/LCD/NTSC/PAL display controller, touchscreen interface, 32/128-bit unique MaverickKey ID, glueless digital audio, CODEC interface	\$15.94
	8-, 16-, 32-bit SRAM/Flash/ROM, 32-bit SDRAM, EPROM, 12-channel DMA	64-entry TLB	352 PBGA	Two 16-bit, 32-bit, 40-bit, watchdog	Two SSI, IrDA, six I2S, SPI, three UART with HDLC, two PWM, three USB 2.0 Host, AC'97, two IDE, PCMCIA interface, 10/100 Ethernet MAC, 8x8 Keypad, 65 GPIO	64	12-bit	-40 to +85	CRT/LCD/NTSC/PAL display controller, touchscreen interface, 32/128-bit unique MaverickKey ID, glueless digital audio, CODEC interface	\$17.66
64-kbyte SRAM	SRAM, SDRAM		QFP, MAPBGA	Four 32-bit timers with DMA, four, 16, or 32 channel eTPU	One or two CAN, Optional 10/100 Ethernet, I2C, three UART, QSPI	Yes		-40 to +85	Optional encryption, background debug	\$10 to \$15
64-kbyte SRAM	DDR or SDR SDRAM		MAPBGA, QFP	Four 32-bit, four programmable interrupt timers, one watchdog	One or two 10/100 Ethernet, I2C, three UART, QSPI, USB	Yes		0 to +70 -40 to +85	Optional encryption, background debug	\$7.50 to \$12.25
Up to 96-kbyte SRAM	EDO, FPM, SDRAM		QFP, BGA	Two to eight 16-bit, four 32-bit, four programmable interval	FlexCAN, 10/100 Ethernet, up to two I2C, up to three UART, QSPI, USB, SPDIF, TDM	Yes	Eight to 10 channel 10 to 12-bit	0 to +70 -40 to +85	Background debug, IDE interface	\$6.99 to \$17.99
4-kbyte SRAM	EDO, FPM, SDRAM		QFP	Two 16-bit	I2C, two UART	Yes		0 to +70 -40 to +85	Background debug	\$11.35 to \$14.95
4-kbyte SRAM	EDO, FPM, SDRAM		QFP	Two 16-bit	I2C, UART, USART	Yes		0 to +70 -40 to +85	Background debug	\$18.95 to \$22.95
32-kbyte SRAM	DDR, SDR SDRAM	Yes	388 PBGA	Four 32-bit timers, two 32-bit slice timers, watchdog	I2C, DSPI, UART, USART, Four PSC, Up to two 10/100 Ethernet, Up to two CAN 2.0B, Optional USB 2.0 with integrated PHY, IrDA, modem	Yes		0 to +70 -40 to +85	Optional encryption, background debug, pin compatibility	\$16.95 to \$26.47

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/ multiplication hardware support (bits)	FPU	Caching
Hyperstone www.hyperstone.com	E1-32XS	E1-32XS (E1-16XS)	up to 115	26/32 (22/16)	Variable 16, 32, 48	2.5	50mA	Powerdown, sleep	32x32 16x16	Software instructions	128-byte instruction
	HyNet-32XS	E1-32XSR (E1-16XS)	up to 220	26/32	Variable 16, 32, 48	1.8	1.7W	Powerdown, sleep, doze	32x32 16x16	Software instructions	2-kbyte instruction/data
	E1-32XSE	E1-32XSR (E1-16XS)	up to 220	26/32	Variable 16, 32, 48	1.8		Powerdown, sleep, doze	32x32 16x16	Software instructions	128-byte instruction
	E1-32XSR	E1-32XSR (E1-16XS)	up to 220	26/32 (22/16)	Variable 16, 32, 48	1.8	40mA	Powerdown, sleep	32x32 16x16	Software instructions	128-byte instruction
Fujitsu Micro-electronics America www.fma.fujitsu.com	FR30	FR	25 to 50, 32.768 KHz	32/32, external: 24/16	16	2.3 to 5.5	270mW	Sleep, stop, sub clock mode, timer	32x32 DSP macro with barrel shifter and bit search		Up to 4-kbyte instruction
	FR50	FR	32 to 64, 32.768 KHz	32/32, external: 24/16	16	2.3 to 5.5	300mW	Sleep, stop, sub clock mode, timer	32x32 with barrel shifter and bit search		Up to 4-kbyte instruction
	FR60	FR	50 to 68, 32.768 KHz	32/32, external: 24/16	16	2.3 to 5.5	450mW	Sleep, stop, sub clock mode, timer	32x32 with barrel shifter and bit search		Up to 4-kbyte instruction
	FR60lite	FR	33	32/32, external: 24/16	16	3 to 5.5	250mW	Sleep, stop, sub clock mode, timer	32x32 with barrel shifter and bit search		Up to 4-kbyte instruction
Intel www.intel.com	80960 Cx	i960	16 to 40	32/32	32	5/5	1034mA	Wait	Yes		1- to 4-kbyte instruction, 1-kbyte data
	80960 HX	i960	25 to 80	32/32	32	3.3/5	1578mA	Halt, wait	Yes		8- or 16-kbyte instruction/data
	80960Jx 80960VH	i960	16 to +100	32/up to 32	32	3.3/5 tolerant	480 to 690mA	Halt	Yes		2- to 16-kbyte instruction, 1- to 4 kbyte data, stack frame
	80960Sx 80960Kx	i960	10 to 25	32/16 or 32	32	5/5	340 to 420mA		Yes	SB/KB only	512-byte instruction
	MCS251 8XC251Sx 8XC251Tx	MCS51	16, 24	24/8	8, 16	4.5 to 5.5 +/- 10%	85mA	Idle, powerdown	16x8		
Xilinx www.xilinx.com	MicroBlaze (soft CPU)	MicroBlaze	150	64/32 (Core Connect)	32	1 to 3.3 (FPGA usage)		Yes	556 multipliers		Fast simplex link
QuickLogic www.quicklogic.com	QL901M	MIPS	100, 133	32/32	32	1.8/3.3	Based on programmable logic usage	Nap, doze	18 MAC blocks (8x8 multiply, 16-bit carry add)	Software floating-point	16-kbyte instruction/data
	QL902M	MIPS	175, 200	32/32	32	1.8/3.3	Based on programmable logic usage	Nap, doze	18 MAC blocks (8x8 multiply, 16-bit carry add)	Software floating-point	16-kbyte instruction/data

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
16-kbyte SRAM	SDRAM, SRAM, FLASH		100/144 LQFP 144 TFBGA	32-bit., watchdog	Three GPIO	Four external		0 to +85 (case)		From \$6.50
16-kbyte RAM, 128-kbyte SRAM, 32-kbyte shared SRAM, 8-kbyte boot ROM	SDRAM, SRAM, FLASH	64-entry TLB, 32 instruction, 32 data	256 TFBGA	32-bit., watchdog, realtime	Two 10/100 Ethernet and PHY, USB 1.1 Host, CAN, up to 58 GPIO Configurable serial controller with 16 pins	Four external		0 to +85	BUS Interface PCM Interface Utopia Level	\$12.50
16-kbyte RAM	SDRAM, SRAM, FLASH		TFBGA , PBGA	32-bit., watchdog, realtime	Two RS232, SPI, I2C, AC97, USB 1.1, dual 10/1000 Ethernet	Four external		0 to +70		\$9
16-kbyte SRAM	SDRAM, SRAM, FLASH		100/144 LQFP 144 TFBGA	32-bit., watchdog	Three GPIO	Four external		0 to +85 (case)		From \$6.50
Up to 512-kbyte Flash, up to 160-kbyte SRAM	DRAM, DMAC		100/120/ 144/160 QFP/LQFP	16-bit reload, free running, PWC, timebase, PPG, PWM	SIO, CAN, UART, I2C, up to 120 PIO	Up to 24 external	Four, eight, or 16 channel 8/10-bit; three channel 8-bit DAC	0 to +70 -40 to +85	Comparator, input capture, output compare	From \$5
Up to 784-kbyte Flash, up to 36-kbyte SRAM	DMAC		120/208 QFP, LQFP	16-bit reload, free running, PWC, timebase, PPG, PWM	SIO, CAN, LIN, UART, I2C	Up to 24 external	Eight or 16 channel 8/10-bit; three channel 8-bit DAC	-40 to +85	Input capture, output compare, sound generator, Stepper motor, comparator	From \$6
Up to 512-kbyte Flash, up to 512-kbyte Font Flash, up to 160-kbyte SRAM	SDRAM, DMAC, USB, Memory stick		100/120/144/176 LQFP, QFP	16-bit reload, free running, PWC, timebase, PPG, PWM	SIO, LIN, UART, I2C	Up to 24 external	Eight or 16 channel 8/10-bit; 8-bit DAC	0 to +70 -40 to +85	Comparator, input capture, output compare, OSDC	From \$6
Up to 512-kbyte Flash, up to 16-kbyte SRAM	DMAC		100/120/144 LQFP/QFP	16-bit reload, free running, PWC, timebase, PPG, PWM	SIO,LIN-UART, I2C	Up to 24 external	Eight or 16 channel 8/10-bit; 8-bit DAC	0 to +70 -40 to +85	Comparator, input capture, output compare	From \$4.25
	Yes		168 PGA, 196 PQFP			Eight, NMI			Supervisor protection	\$27.09 to \$67.56
2-kbyte RAM	GMU		168 PGA, 208 PQFP	Two 32-bit		Eight, NMI			Supervisor protection	\$34.60 to \$106.17
1-kbyte RAM	SRAM, Flash		132 PGA/PQFP, 196/324 PBGA	Two 32-bit	I2C	Program-mable, high-speed controller			16/16 global/local 32-bit registers, high-bandwidth burst bus, JTAG	\$9.98 to \$68.17
	Yes		84 PLCC, 80 QFP, 132 PGA/PQFP			Four, direct, handshake				\$7.98 to \$39.03
8- or 16-kbyte OTP, ROM, 512- or 1024-byte RAM			44 PLCC, 40 PDIP	Three 16-bit, PCA, watchdog	One or two UART	Eight, four levels			40-byte register file	\$4.84 to \$6.87
72- to 3456-kbyte	SDRAM, DDR, SRAM, Flash, ZBT, SDARM (soft IP)		Virtex/E, SpartanII, SpartanIIE, Spartan3, VirtexII, VirtexII PRO	Watchdog, counters attached via CoreConnect bus	CoreConnect-enabled UART, I2C, GPIO, SPI, 16450/550, 10/100 EMAC, UART lite, 1 Gbit Ethernet	Soft IP		0 to +70 -40 to +85 -40 to +125	1200 I/O and 125,126 logic cells, chip scope for FPGA debugging	From \$10
16-kbyte SRAM, 82.9-kbit dual-port SRAM (128x18, 256x9, 512x4, 1024x2)	SDRAM, Flash, SRAM, EPROM	32-bit-entry TLB	680 PBGA, 1.27-mm pitch	Four 32-bit	Two serial (hardware flow control, IrDA), PCI	Seven		0 to +70 -40 to +85	2016 programmable logic cells (~75,000 ASIC gates)	\$70
16-kbyte SRAM, 82.9-kbit dual-port SRAM (128x18, 256x9, 512x4, 1024x2)	SDRAM, Flash, SRAM, EPROM	32-bit-entry TLB	544 PBGA, 1.27-mm pitch	Four 32-bit	Two serial (hardware flow control, IrDA), PCI	Seven		0 to +70 -40 to +85	2016 programmable logic cells (~75,000 ASIC gates), SVGA controller, AES encryption, IDE controller, video (de)compression	\$50

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
	QL903M	MIPS	175, 200	32/32	32	1.8/3.3	Based on programmable logic usage	Nap, doze	18 MAC blocks (8x8 multiply, 16-bit carry add)	Software floating-point	16-kbyte instruction/data
	QL904M	MIPS	175, 200	32/32	32	1.8/3.3	Based on programmable logic usage	Nap, doze	18 MAC blocks (8x8 multiply, 16-bit carry add)	Software floating-point	16-kbyte instruction/data
IDT www.idt.com	RC32332	MIPS II	100, 133, 150	23/32	32	2.5/3.3 or 3.3/3/3	0.95 or 1.7W	Wait	32x32		8/2-kbyte instruction/data, two-way set associative
	RC32333	MIPS II	100, 133, 150	23/32	32	2.5/3.3 or 3.3/3/3	0.95 or 1.7W	Wait	32x32		8/2-kbyte instruction/data, two-way set associative
	RC32334	MIPS II	100, 133, 150	26/32	32	3.3/3.3	1.7W	Wait	32x32		8/2-kbyte instruction/data, two-way set associative
	RC32336	MIPS II	180	22/32	32	2.5/3.3	2.38W	Wait	32x32		8/2-kbyte instruction/data, two-way set associative
	RC32351	MIPS II	100, 133	26/32	32	2.5/3.3	1.26W	Wait	32x32		8/2-kbyte instruction/data, two-way set associative
	RC32355	MIPS II	133, 150, 180	26/32	32	2.5/3.3	1.73W	Wait	32x32		8/2-kbyte instruction/data, two-way set associative
	RC32365	MIPS II	150, 180	22/32	32	2.5/3.3	2.38W	Wait	32x32		8/2-kbyte instruction/data, two-way set associative
Toshiba America Electronic Components www.toshiba.com	TX19 family	MIPS16	Up to 40	24/32, external: 8 or 16	16, 32	2 to 3.6	165mW (ROM)	Stop, sleep, slow	One-cycle MAC		
AMD www.amd.com	Alchemy Au1000	MIPS32	266, 400, 500	32/32	32	1.5 to 1.8/3.3	900mW	Idle, sleep	MAC		16-kbyte instruction/data

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
16-kbyte SRAM, 82.9-kbit dual-port SRAM (128x18, 256x9, 512x4, 1024x2)	SDRAM, Flash, SRAM, EPROM	32-bit-entry TLB	544 PBGA, 1.27-mm pitch	Four 32-bit	Two serial (hardware flow control, IrDA), PCI	Seven		0 to +70 -40 to +85	2016 programmable logic cells (~43,000 ASIC gates), SVGA controller, AES encryption, IDE controller, video (de)compression	\$40
16-kbyte SRAM, 82.9-kbit dual-port SRAM (128x18, 256x9, 512x4, 1024x2)	SDRAM, Flash, SRAM, EPROM	32-bit-entry TLB	544 PBGA, 1.27-mm pitch	Four 32-bit	Two serial (hardware flow control, IrDA)	Seven		0 to +70 -40 to +85	1152 programmable logic cells (~43,000 ASIC gates), SVGA controller, AES encryption, IDE controller, video (de)compression	\$35
	32-bit SDRAM, 8-, 16-, 32-bit SRAM, Flash, ROM, dual-port	32-entry TLB	208 QFP	Four 32-bit	UART (16550-compatible), v2.1 PCI 32-bits, eight PIO	Four, more via PIO		-40 to +85 0 to +70 (case)	EJTAG debug	\$10 to \$15.25
	32-bit SDRAM, 8-, 16-, 32-bit SRAM, Flash, ROM, dual-port	32-entry TLB	208 QFP	Four 32-bit	UART (16550-compatible), v2.1 PCI 32-bits, eight PIO	Four, more via PIO		-40 to +85 0 to +70 (case)	EJTAG debug	\$10 to \$15.25
	32-bit SDRAM, 8-, 16-, 32-bit SRAM, Flash, ROM, dual-port	32-entry TLB	256 PBGA	Four 32-bit	Dual UART (16550-compatible), v2.1 PCI bridge, 16 PIO	Four, more via PIO		-40 to +85 0 to +70 (case)	EJTAG debug	\$15 to \$19.25
	32-bit SDRAM, 8-, 16-, 32-bit SRAM, Flash, ROM, dual-port, six-channel DMA	16-entry TLB	256 CABGA	Three 32-bit	UART (16550-compatible), SPI, 16 GPIO, v2.2 PCI 32-bits, v2.1 PCMCIA, two 10/100 Ethernet	Four, more via PIO		0 to +70	EJTAG debug	\$15
	32-bit SDRAM, 8-, 16-, 32-bit SRAM, Flash, ROM, dual-port	16-entry TLB	208 QFP	Three 32-bit	Two UART (16550-compatible), USB 1.1, ATM (Utopia1/2), 10/100Mbps Ethernet, 32 PIO	Four, more via PIO		0 to +70	EJTAG debug	\$15 to \$15.75
	32-bit SDRAM, 8-, 16-, 32-bit SRAM, Flash, ROM, dual-port	16-entry TLB	208 QFP	Three 32-bit	Two UART (16550-compatible), USB 1.1, I2C, TDM, ATM (Utopia1/2), 10/100Mbps Ethernet, 32 PIO	Four, more via PIO		-40 to +85 0 to +70 (case)	EJTAG debug	\$17.50 to \$20.90
	32-bit SDRAM, 8-, 16-, 32-bit SRAM, Flash, ROM, dual-port, six-channel DMA	16-entry TLB	256 CABGA	Three 32-bit	UART (16550-compatible), SPI, 16 GPIO, v2.2 PCI 32-bits, v2.1 PCMCIA, two 10/100 Ethernet	Four, more via PIO		-40 to +85 0 to +70 (case)	Integrated IPsec HW Acceleration (DES, 3DES, AES), Random Number Generator, EJTAG debug	\$15 to \$16
Up to 1-Mbyte mask ROM or Flash, 40-kbyte SRAM	Eight-channel DMA		100 LQFP, 281FBGA	Four 16-bit, up to 12 8-bit, eight 32-bit input capture, real-time, watchdog	Up to eight UART, I2C, 77 PIO	Up to 29 external, NMI	Up to 24 channel 10-bit			\$8 to \$15
See cache	SRAM, SSRAM, SDRAM, Flash, EPROM	32-entry TLB, four-entry instruction TLB	324 PBGA	Programmable interval, real-time	Four UART, 32 GPIO, USB host/device, IrDA, AC97, I2S, two SSI, two Ethernet	Yes		0 to +70 -40 to +85		\$17 to \$30.17

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
	Alchemy Au1100	MIPS32	333, 400, 500	32/32	32	1.2/2.5, 3.3	400mW	Idle, sleep	MAC		16-kbyte instruction/data
	Alchemy Au1500	MIPS32	333, 400, 500	32/32	32	1.5 to 1.8/3.3	1.2W	Idle, sleep	MAC		16-kbyte instruction/data
	Alchemy Au1550	MIPS32	333, 400, 500	32/32	32	1.2/2.5, 3.3	500mW (400MHz)	Idle, sleep, hibernate	MAC		16-kbyte instruction/data
IDT www.idt.com	RC32434	MIPS32	266, 300, 350, 400	26/8	32	1.2/3.3	1.54W	Wait	32x32		8/8-kbyte instruction/data, four-way set associative
	RC32438	MIPS32	200, 233, 266	26/16	32	1.2/3.3	2.0W	Wait	32x32		16-kbyte instruction/data, four-way set associative
MIPS Technologies www.mips.com	24Kc (Pro) 24Kf (Pro)	MIPS32	400 to 550	32/64	32	Process dependent	0.5 mW/MHz	Wait	32x32	Optional, IEEE, 754-compliant	16/32/64-kbyte instruction/data
	4Kc 4Km 4Kp	MIPS32	230 to 260	32/32	32	Process dependent	0.1 to 0.3mW (0.13)	Wait	One-cycle 16x16, 32x16, two-cycle 32x32		0- to 16-kbyte instruction/data
	4KEc (Pro) 4KEm (Pro) 4KEp (Pro)	MIPS32	230 to 260	32/32	32	Process dependent	0.1 to 0.3mW (0.13)	Wait	One-cycle 16x16, 32x16, two-cycle 32x32		0- to 64-kbyte instruction/data
	4KSd	MIPS32	200 to 240	32/32	32	Process dependent	0.1 to 0.3mW (0.13)	Wait	One-cycle 16x16, 32x16, two-cycle 32x32		0- to 64-kbyte instruction/data
	M4K M4K Pro	MIPS32	200 to 240	32/32, SRAM	32	Process dependent	0.1 to 0.3mW (0.13)	Wait	One-cycle 16x16, 32x16, two-cycle 32x32		
Altera www.altera.com	Nios (soft core)	Nios	Over 125	16/16, or 32/32	16	1.5, 1.8, 2.5, 3.3, 5		User-added	250-MHz 36x36 DSP block, two-cycle 16x16, 1-bit/clock, user-definable	Can add accelerator block	Configurable 1- to 16-kbyte instruction/data, direct mapped, write-through
	Nios II/e (economy soft core)	Nios II	Over 200	32/32 (dynamic sizing)	32	1.2, 1.5		User-added	370-MHz user-definable MAC (9x9, 18x18, or 36x36)	Can add accelerator block	

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
See cache	SRAM, SSRAM, SDRAM, Flash, EPROM	32-entry TLB, four-entry instruction TLB	399 PBGA	Programmable interval, real-time	Three UART, 48 GPIO, USB host/device, IrDA, AC97, I2S, two SSI, Ethernet, two SD, LCD, PCMCIA	Yes		0 to +70		\$18.18 to \$37.50
See cache	SRAM, SSRAM, SDRAM, Flash, EPROM	32-entry TLB, four-entry instruction TLB	424 PBGA	Programmable interval, real-time	Two UART, 39 GPIO, USB host/device, AC97, two Ethernet, PCI	Yes		0 to +70 0 to +50 (500MHz)		\$18.18 to \$37.50
See cache	SRAM, SSRAM, SDRAM, Flash, EPROM, DDR	32-entry TLB, four-entry instruction TLB	483 BGA	Programmable interval, real-time	Three UART, 43 GPIO, USB host/device, PCI, two Ethernet, PCMCIA, and four programmable serial controllers for AC97, I2S, SPI, SMBus, SSI	Yes		0 to +85 -40 to +100	SafeNet's embedded security engine	\$20.62 to \$32.74
	16-bit DDR, 8-bit SRAM, ROM, Flash, dual-port	16-dual-entry TLB	256 CABGA	Three 32-bit	UART (16550-compatible), I2C, SPI, 10/100 Ethernet, v2.2 PCI 32-bit, 14 GPIO	Four, more via PIO		-40 to +85 0 to +70 (case)	Enhanced JTAG and ICE interfaces. Integrated authentication unit with NVRAM.	\$15.50 to \$23
	16-, 32-bit DDR, 8-, 16-bit SRAM, ROM, Flash, dual-port	16-dual-entry TLB	416 BGA	Three 32-bit	Dual UART (16550-compatible), I2C, SPI, Two 10/100 Ethernet, v2.2 PCI 32-bit, 32 GPIO	Four, more via PIO		-40 to +85 0 to +70 (case)	Enhanced JTAG and ICE interfaces. On-chip bus-monitor logic	\$25 to \$35
Configurable	Optional	16, 32, 64-entry jTLB with variable page size, optional FMT	N/A - IP core					N/A (Core)	Synthesizable core, OCP interface, CorExtend user defined instructions	License
Configurable	Optional	16 dual-entry jTLB with variable page size or FMT mechanism	N/A - IP core	Optional				N/A (Core)	Synthesizable core	License
Configurable	Optional	16 dual-entry jTLB with variable page size or FMT mechanism	N/A - IP core					N/A (Core)	Synthesizable core, CorExtend user-instructions	License
Configurable	Optional	16 dual-entry jTLB with variable page size or FMT mechanism	N/A - IP core					N/A (Core)	Synthesizable core, code compression, SmartMIPS ASE, crypto-acceleration, CorExtend user-instructions	License
Configurable	Optional	16 dual-entry jTLB with variable page size or FMT mechanism	N/A - IP core					N/A (Core)	Synthesizable core, cacheless design for multiprocessor designs	License
Up to 12 64-kbyte RAM blocks, multiple configuration register file	SRAM, SSRAM, SDRAM, Flash		N/A - IP core	32-bit, watchdog, PWM, configurable	Configurable, RS232, SPI, GPIO, IDE, PCI, Ethernet	Up to 64, configurable		N/A (Core)	Custom instructions, hardware accelerators, simultaneous multiple master bus	Royalty-free license in Altera PLDs; ASIC license
Up to nine 64-kbyte RAM blocks	SRAM, SSRAM, SDRAM, CFI flash		N/A - IP core	32-bit, watchdog, PWM, configurable	RS232, SPI, GPIO, IDE, PCI, JTAG, Ethernet, DMA	32		N/A (Core)	Over 30 DMIPs, 256 custom instructions, unlimited hardware accelerators, over 60 available peripherals	From 35 cents; royalty-free in Altera FPGAs; ASIC license

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
	Nios II/f (fast soft core)	Nios II	Over 180	32/32 (dynamic sizing)	32	1.2, 1.5		User-added	370-MHz user-definable MAC (9x9, 18x18, or 36x36)	Can add accelerator block	Configurable up to 64-kbyte instruction/data
	Nios II/s (standard soft core)	Nios II	Over 160	32/32 (dynamic sizing)	32	1.2, 1.5		User-added	370-MHz user-definable MAC (9x9, 18x18, or 36x36)	Can add accelerator block	Configurable up to 64-kbyte instruction/data
AMCC www.amcc.com	PowerPC 405EP	PowerPC	333	32	16	1.8/3.3	1.2W		16x16 MAC		
	PowerPC 405GP/CR	PowerPC	266	32	16	2.5/3.3	1.5W (GP) 0.8W (CR)		16x16 MAC		16-kbyte/8-kbyte
	PowerPC 405GPr	PowerPC	400	32	16	1.8/3.3	0.72W		16x16 MAC		16-kbyte/16-kbyte
	PowerPC 440EP	PowerPC	533	32	32	1.5/2.5, 3.3	3W		16x16 MAC	Double precision	32-kbyte/32K-kbyte
	PowerPC 440GP	PowerPC	500	32/64	32	1.85/2.5, 3.3	Less than 4W		16x16 MAC		32-kbyte/32K-kbyte
	PowerPC 440GX	PowerPC	800	32/64	32	1.5/2.5, 3.3	4.5W		16x16 MAC		32-kbyte/32K-kbyte
	PowerPC 440SP	PowerPC	667	32/64	32	1.5/2.5, 3.3	6W		16x16 MAC		32-kbyte/32K-kbyte
	PowerPC NPe405L/H	PowerPC	266	32	16	2.5/3.3	1.7W to 2.4W		16x16 MAC		16-kbyte/8-kbyte
Freescale www.freescale.com	MP8540 PowerQUICC III	PowerPC	667 to 1GHz	64/64 (Local Bus PCI/PCI-X), 8 (RapidIO)	32	1.2	6.9W			Yes	32/32-kbyte instruction/data, L2: 256-kbyte unified
	MP8541 PowerQUICC III	PowerPC	533 to 833	32 (Local Bus PCI), 32/64 (PCI)	32	1.2	5.4W			Yes	32/32-kbyte instruction/data, L2: 256-kbyte unified

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
Up to nine 64-kbyte RAM blocks	SRAM, SSRAM, SDRAM, CFI flash		N/A - IP core	32-bit, watchdog, PWM, configurable	RS232, SPI, GPIO, IDE, PCI, JTAG, Ethernet, DMA	32		N/A (Core)	Over 200 DMIPs, 256 custom instructions, unlimited hardware accelerators, over 60 available peripherals	From \$1.12; royalty-free in Altera FPGAs; ASIC license
Up to nine 64-kbyte RAM blocks	SRAM, SSRAM, SDRAM, CFI flash		N/A - IP core	32-bit, watchdog, PWM, configurable	RS232, SPI, GPIO, IDE, PCI, JTAG, Ethernet, DMA	32		N/A (Core)	Over 125 DMIPs, 256 custom instructions, unlimited hardware accelerators, over 60 available peripherals	From 78 cents; royalty-free in Altera FPGAs; ASIC license
4-kbyte		Yes	385 PBGA	Yes	Two UART, I2C, GPIO, UI2C, two 10/100 Ethernet	7 external, 19 internal		-40 to +85		\$17
4-kbyte (GP)	SRAM, SDRAM	Yes	316/413/456 PBGA	Yes	10/100 Ethernet, two UART, I2C, GPIO, UIC, CodePack	7 external, 19 internal		-40 to +85	On-chip SRAM with single-cycle access	\$15
4-kbyte	SRAM, SDRAM	Yes	456 PBGA	Yes	10/100 Ethernet, two UART, I2C, GPIO, UIC, CodePack	13 external, 19 internal		-40 to +85	On-chip SRAM with single-cycle access	\$27
	DDR	Yes	456 PBGA	Yes	Two 10/100 Ethernet, DMA, SPI, USB, UIC, two I2C, four UART, GPIO	10 external, 63 internal		-40 to +85		\$25
8-kbyte	DDR SRAM	Yes	552 CBGA	Yes	Two 10/100 Ethernet, two UART, two I2C, GPIO, UIC, GPT	13 external, 63 internal		-40 to +85	PCI-X	\$75
256-kbyte	DDR SDRAM	Yes	552 CBGA	Yes	Two 10/100 Ethernet, DMA, two 10/100/1000 Ethernet, two I2C, two UART, GPIO, GPT, UIC	18 external, 63 internal		-40 to +85	PCI-X	\$68
256-kbyte	Dual-ported 32/64-bit SDRAM	Yes	783 PBGA	Yes	10/100/1000 Ethernet, three UART, two I2C, GPIO, UIC, GPT, I20, XOR	18 external, 63 internal		-40 to +85	PCI-X	\$100
4-kbyte	SDRAM	Yes	324 PBGA, 580 PBGA	Yes	Four 10/100 Ethernet, DMA, I2C, two UART, GPIO, UIC, 32-channel HDLC, 8-port HDLC	7 external, 19 internal		-40 to +85		\$19
64-kbyte DPRAM	DDR-1 SDRAM, SDRAM, DRAM, SRAM, Flash	64-entry, four-way set-associative TLB, L2: 16-entry, fully associative TLB, 256-entry, two-way set-associative TLB	783 FCBGA	Four 16-bit or two 32-bit	Two 10/100/1000 Ethernet, DUART, I2C, PCI/PCI-X, local bus, GPIO, 10/100 Ethernet, RapidIO	16 programmable, 16 levels, 12 external, four message, 22 other internal sources		-40 to +110 junction temperature	e500 PowerPC core, hardware coherency, 130nm	\$88 to \$110
64-kbyte DPRAM	DDR-1 SDRAM, SDRAM, DRAM, SRAM, Flash	64-entry, four-way set-associative TLB, L2: 16-entry, fully associative TLB, 256-entry, two-way set-associative TLB	783 FCBGA	Four 16-bit or two 32-bit, realtime	Two 10/100 and two 10/100/1000 Ethernet, ATM, transparent; QMCI; three serial controllers for Ethernet, HDLC, UART, BISYNC, transparent; two serial channels for UART; I2C, SPI, USB	16 programmable, 16 levels, 12 external, four message, 22 other internal sources		-40 to +110 junction temperature	e500 core, hardware coherency, integrated security engine (IPsec, SSL, etc.), time slot assigner, three TDM interfaces, four baud rate generators, debug interface, 130nm	\$75 to \$115

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
	MP8555 PowerQUICC III	PowerPC	533 to 833 (333 with Communications Processor Module)	32 (Local Bus PCI), 32/64 (PCI)	32	1.2	5.4W			Yes	32/32-kbyte instruction/data, L2: 256-kbyte unified
	MP8560 PowerQUICC III	PowerPC	667 to 1GHz (333 with Communications Processor Module)	64/64 (Local Bus PCI/PCI-X), 8 (RapidIO)	32	1.2	7.4W			Yes	32/32-kbyte instruction/data, L2: 256-kbyte unified
	MPC603	PowerPC	200, 266, 300	32/64	64	2.5/3.3	4.0W/6.1W (300MHz)	Doze, stop		Yes	16/16-kbyte instruction/data, four-way set-associative
	MPC7410	PowerPC	400, 450, 500	32/64	64	1.8/2.5	5.3W/11.9W (500MHz)	Nap, sleep, deep sleep		Yes	32/32-kbyte instruction/data, eight-way set-associative
	MPC7445	PowerPC	600, 733, 800, 867, 933, +1000	36/64	64	1.3/2.5	15W/22W (1000MHz)	Nap, sleep, deep sleep		Yes	32/32-kbyte instruction/data, eight-way set-associative
	MPC7447	PowerPC	600, 733, 867, +1000, 1200, 1267	36/64	64	1.1/2.5	18W/25W (1267MHz), 8.3W/11.5W (1GHz)	Nap, sleep, deep sleep		Yes	32/32-kbyte instruction/data, eight-way set-associative
	MPC7447A	PowerPC	733, 867, +1000, 1167, 1267, 1333, 1420	36/65	64	1.3/2.5	21W/30W (1420MHz)	Nap, sleep, deep sleep		Yes	32/32-kbyte instruction/data, eight-way set-associative
	MPC745	PowerPC	300, 350	32/64	64	2/3.3	4.0W/5.7W (350MHz)	Doze, stop		Yes	32/32-kbyte instruction/data, eight-way set-associative
	MPC7455	PowerPC	600, 733, 800, 867, 933, +1000	36/64	64	1.3/2.5	15W/22W (1000MHz)	Nap, sleep, deep sleep		Yes	32/32-kbyte instruction/data, eight-way set-associative
	MPC7457	PowerPC	600, 733, 867, +1000, 1200, 1267	36/64	64	1.1/2.5	18W/25W (1267MHz), 8.3W/11.5W (1GHz)	Nap, sleep, deep sleep		Yes	32/32-kbyte instruction/data, eight-way set-associative
	MPC755	PowerPC	300, 350, 400	32/64	64	2/3.3	4.0W/6.0W (400MHz)	Doze, stop		Yes	32/32-kbyte instruction/data, eight-way set-associative
	MPC8241	PowerPC	166, 200, 266	64	32	1.8/2	2.1	Doze, stop		Yes	16/16-kbyte instruction/data, four-way set-associative
	MPC8245	PowerPC	266, 300, 333, 350, 400	64	32	1.8/2	2.8	Doze, stop		Yes	16/16-kbyte instruction/data, four-way set-associative

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
64-kbyte DPRAM	DDR-1 SDRAM, SDRAM, DRAM, SRAM, Flash	64-entry, four-way set-associative TLB, L2: 16-entry, fully associative TLB, 256-entry, two-way set-associative TLB	783 FCBGA	Four 16-bit or two 32-bit, realtime	Two 10/100 and two 10/100/1000 Ethernet, ATM, transparent; QMCI; three serial controllers for Ethernet, HDLC, UART, BISYNC, transparent; two serial channels for UART; I2C, SPI, USB	16 programmable, 16 levels, 12 external, four message, 22 other internal sources		-40 to +110 junction temperature	e500 core, hardware coherency, integrated security engine (IPsec, SSL, etc.), time slot assigner, three TDM interfaces, four baud rate generators, debug interface, 130nm	\$88 to \$126
64-kbyte DPRAM	DDR-1 SDRAM, SDRAM, DRAM, SRAM, Flash	64-entry, four-way set-associative TLB, L2: 16-entry, fully associative TLB, 256-entry, two-way set-associative TLB	783 FCBGA	Four 16-bit or two 32-bit, realtime	Two 10/100/1000 and three 10/100 Ethernet, ATM, transparent; two 128 channels of HDLC or transparent; four serial controllers for Ethernet, HDLC, UART, BISYNC, transparent; I2C, SPI, PCI/PCI-X, local bus, RapidIO	16 programmable, 16 levels, 12 external, four message, 22 other internal sources		-40 to +110 junction temperature	e500 PowerPC core, hardware coherency, time slot assigner, eight TDM interfaces, transmission convergence layer for ATM, IMA, four baud rate generators, debug interface, 130nm	\$115 to \$144
		64-entry TLB, two-way set associative	CBGA, PBGA					0 to +105		\$45
		128-entry TLB, two-way set associative	FCCBGA, HiCTE					0 to +105	Altivec	\$81
256-kbyte L2		128-entry TLB, two-way set associative	FCCBGA, HiCTE					0 to +105	Altivec	\$214
512-kbyte L2		128-entry TLB, two-way set associative	FCCBGA, HiCTE					0 to +105	Altivec	\$203
512-kbyte L2		128-entry TLB, two-way set associative	HiTCE					0 to +105	Altivec	\$245
		128-entry TLB, two-way set associative	FCPBGA					0 to +105		\$44
256-kbyte L2		128-entry TLB, two-way set associative	FCCBGA, HiCTE					0 to +105	Altivec	\$252
512-kbyte L2		128-entry TLB, two-way set associative	FCCBGA, HiCTE					0 to +105	Altivec	\$233
		128-entry TLB, two-way set associative	FCCBGA, FCPBGA					0 to +105		\$67
	EPROM, FLASH, DRAM, SDRAM, SRAM	64-entry TLB, two-way set associative	357 PBGA	Four 16-bit or two 32-bit	I2C, SPI, PCI, local bus			0 to +105 junction -40 to 105 junction		\$12 to 25
	EPROM, FLASH, DRAM, SDRAM, SRAM	64-entry TLB, two-way set associative	352 TBGA	Four 16-bit or two 32-bit	I2C, SPI, PCI, local bus			0 to +105 junction -40 to 105 junction		\$15 to 60

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
	MPC8260 PowerQUICC II Family (MPC8260, 8250, 8255, 8264, 8265, 8266)	PowerPC	266, 300	64	32	1.8 to 2.2	3	Doze, stop		Yes	16/16-kbyte instruction/data, four-way set-associative
	MPC8272 PowerQUICC II Family (MPC8272, 8271, 8248, 8247)	PowerPC	266, 300, 400	64	32	1.5	1.2W	Doze, stop		Yes	16/16-kbyte instruction/data, four-way set-associative
	MPC8280 PowerQUICC II Family (MPC8280, 8275, 8270)	PowerPC	266, 333, 450	64	32	1.5	2	Doze, stop		Yes	16/16-kbyte instruction/data, four-way set-associative
	MPC8349E PowerQUICC II Pro Family (MPC8349E, 8347E, 8343E)	PowerPC	266, 400, 533, 667	64	32	1.2	1.3W	Nap, doze, sleep		Yes	32/32-kbyte instruction/data, eight-way set-associative with parity
	MPC860 PowerQUICC I Family (MPC860, 860P, 855T, 862T, 862P, 857T, 857DSL)	PowerPC	50, 66, 80, +100	32	32	3.3	1.35	Sleep, doze, power-down	16x16 MAC		4- to 16-kbyte instruction, 4- to 8 kbyte data, two-way set-associative
	MPC866 PowerQUICC I Family (MPC866, 852T, 859T, 859DSL)	PowerPC	50, 66, 80, +100, 133	32	32	1.8	0.26	Normal low	16x16 MAC		4- to 16-kbyte instruction, 4- to 8 kbyte data, two-way set-associative

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
32-kbyte DPRAM	EDO, EPROM, FLASH, DRAM, SDRAM, SRAM	64-entry TLB, two-way set associative	480 TBGA	Four 16-bit or two 32-bit, realtime	Three controllers for ATM, 10/100 Ethernet, or transparent; I2C, two 128-channel transparent or HDLC controllers; four controllers for Ethernet, UTOPIA, HDLC, UART, transparent, or BiSync; two UART or transparent channels, SPI, PCI, local bus	Eight IRQ, 24 external sources		0 to +105 junction -40 to 105 junction	Time slot assigner, eight TDM interfaces, transmission convergence layer for ATM, IMA, parallel I/O, eight baud rate generators, debug interface	\$33 to \$120
20-kbyte DPRAM	EDO, EPROM, FLASH, SDRAM, SRAM	64-entry TLB, two-way set associative	516 PBGA	Four 16-bit or two 32-bit, realtime	Two controllers for ATM, 10/100 Ethernet, or transparent; I2C, SPI, PCI, three controllers for HDLC, UART, transparent, BiSync, or QMC; USB, two serial transparent or UART channels	Eight IRQ, 24 external sources		0 to +105 junction -40 to 105 junction	Integrated security engine (IPsec, SSL, etc.), time slot assigner, two TDM interfaces supporting 64 HDLC channels, eight baud rate generators, debug interface	\$19 to \$32
64-kbyte DPRAM	EDO, EPROM, FLASH, SDRAM, SRAM	64-entry TLB, two-way set associative	480 TBGA, 516 PBGA	Four 16-bit or two 32-bit, realtime	Three controllers for ATM, 10/100 Ethernet, or transparent; two 128 channels of transparent or HDLC; four serial controllers for Ethernet, HDLC, UART, BiSync, transparent; two serial channels for transparent or UART, I2C, SPI, PCI, local bus, USB	Eight IRQ, 24 external sources		0 to +105 junction -40 to 105 junction	Time slot assigner, eight TDM interfaces, transmission convergence layer for ATM, IMA, eight baud rate generators, debug interface	\$30 to \$90
	DDR-1 SDRAM, SDRAM, DRAM, SRAM, Flash	64-entry TLB, two-way set associative	620 PBGA 672 TBGA	Eight 16-bit or four 32-bit or two 64-bit, realtime	Two 10/100/1000 Ethernet, Dual Hi-Speed USB, Dual 32-bit/66MHz PCI, 32-bit Local Bus, DUART, dual I2C, SPI	Eight IRQ, 35 external sources		0 to +105 junction -40 to 105 junction	Integrated security engine (IPsec, SSL, etc.), 64 muxed PIO, debug interface	\$20 to \$50
8-kbyte DPRAM	EDO, EPROM, FLASH, DRAM, SDRAM, SRAM	32-entry TLB, fully associative	357 PBGA	Four 16-bit or two 32-bit	10/100 Ethernet, four serial controllers for Ethernet, UTOPIA, HDLC, Async HDLC, UART, BiSync, transparent; two serial channels for UART, transparent; I2C, SPI, PCMCIA	Seven IRQ, 12 port pins, 23 internal sources		0 to +105 junction -40 to +115 junction	Time slot assigner, four baud rate generators, debug interface	\$27 to \$50
8-kbyte DPRAM	EDO, EPROM, FLASH, DRAM, SDRAM, SRAM	32-entry TLB, fully associative	357 PBGA 256 PBGA	Four 16-bit or two 32-bit	10/100 Ethernet, four serial controllers for Ethernet, UTOPIA, HDLC, Async HDLC, UART, BiSync, transparent; two serial channels for UART, transparent; I2C, SPI, PCMCIA	Seven IRQ, 12 port pins, 23 internal sources		0 to +95 junction -40 to +100 junction	Time slot assigner, four baud rate generators, debug interface	\$8 to \$45

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32-BIT MICROPROCESSORS

Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/ multiplication hardware support (bits)	FPU	Caching
	MPC885 PowerQUICC I Family (MPC885, 880, 875, 870)	PowerPC	66, 80, 133	32	32	1.8	0.43	Normal low	16x16 MAC		8/8-kbyte instruction/data, two-way set-associative
Xilinx	PowerPC 405 embedded in Virtex-II PRO FPGA	PowerPC	600	64/32 (Core Connect)	32	1 to 3.3 (FPGA usage)	0.9mW/MHz	Yes	556 multipliers, user-definable DSP, two-cycle 32x32 multiply, 32x32 multiply/divide		16-kbyte instruction/data
Hyperstone	F2-16X S2-6X M2-6X	RISC	up to 50	20/16 (16/16)	Variable 16, 32, 48	2.5		Automatic powerdown	32x32 16x16	Software instructions	128-byte instruction
NetSilicon	NET+40	RISC	33	28/32	16, 32	3.3	15mW/MHz		Yes		4-kbyte instruction/data
	NET+50	RISC	44	28/32	16, 32	2.5/3.3	480mW		Yes		8-kbyte instruction/data
	NS7520	RISC	55	28/32	16, 32	1.5/3.3	500mW		Yes		
	NS9750	RISC	200	32/32	16, 32	1.5/3.3	1.7W		Yes		8/4-kbyte instruction/data
	NS9775	RISC	200	32/32	16, 32	1.5/3.3	1.7W		Yes		8/4-kbyte instruction/data
Stretch	S5000	SCP	250, 300	24/8 or 24/16 or Multiplexed 24/32	16, 24	1.2	2W to 4W		64 16x16 multipliers and 256 32-bit ALU	Yes	32/32-kbyte instruction/data
STMicroelectronics	ST40RA (SH-4 core)	SH4	150, 166, 200	14/64 SDRAM, 26/32 peripheral, 32	16	1.8/3.3	980mW	Three	64-bit FPU with vector operations	Single/double-precision, IEEE-754, matrix, 3-D vector, transcendental	8/16-kbyte instruction/data, RAM/cache mode

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
8-kbyte DPRAM	EDO, EPROM, FLASH, DRAM, SDRAM, SRAM	32-entry TLB, fully associative	357 PBGA, 256 PBGA	Four 16-bit or two 32-bit	USB, Two 10/100 Ethernet, three serial controllers for Ethernet, UTOPIA, HDLC, Async HDLC, UART, BiSync, transparent; two serial channels for UART, transparent; I2C, SPI, PCMCIA	Six IRQ, 12 port pins, 23 internal sources		0 to +95 junction -40 to +100 junction	Integrated security engine (IPsec, SSL, etc.), time slot assigner, four baud rate generators, debug interface	\$9 to \$19
72- to 3456-kbyte, 216- to 10,006-kbit	SDRAM, DDR, SRAM, Flash, ZBT, SDARM (soft IP)	Embedded MMU	Virtex/E, SpartanII, SpartanIIE, Spartan3, VirtexII, VirtexII PRO	PIT, FIT, watchdog	CoreConnect-enabled UART, I2C, GPIO, SPI, 16450/550, 10/100 EMAC, UART lite, 1 Gbit Ethernet	Core-Connect enabled controller, PowerPC capability		0 to +70 -40 to +85 -40 to +125	1200 I/O and 125,126 logic cells, chip scope PRO for FPGA debugging	From \$40
16-kbyte SRAM, 8-kbyte boot ROM	NAND/AND FLASH		100 TQFP, 128 LQFP, 72 LGA Die	32-bit., watchdog		Four external		0 to +85 (case)	Compact Flash interface, multimedia interface	From \$3.75
Cache optionally configurable as 8 kbyte of RAM	SRAM, SDRAM, EDO DRAM, Flash, 10-channel DMA		208 PQFP	Two 27-bit, watchdog, bus	Two UART, two HDLC, two SPI, 24 PIO, four 1284, 10/100 Ethernet	Four external		-40 to +85	Co-processor interface	\$24.95
Cache optionally configurable as 16-kbyte of RAM	SRAM, SDRAM, EDO DRAM, Flash, 10-channel DMA		208 PQFP, 208 BGA	Two 27-bit, watchdog, bus	Two UART, two HDLC, two SPI, 40 PIO, four 1284, 10/100 Ethernet	36 external		-40 to +85	Co-processor interface	\$13.95 to \$16.95
	SRAM, SDRAM, EDO DRAM, Flash, 13-channel DMA		177 BGA	Two 27-bit, watchdog, bus	Two UART, two HDLC, two SPI, 16 PIO, four 1284, 10/100 Ethernet	Four external		-40 to +85		\$9.95
	SDRAM, static	Yes	352 BGA	Sixteen programmable 16 or 32-bit, watchdog, system bus monitor, system bus arbiter	50 GPIO, four programmable serial (UART, HDLC, SPI master /slave), USB host/device, 10/100 Ethernet, PCI/CardBus, 1284, I2C, LCD controller	Four external		-40 to +85		\$14.95 to \$19.95
	SDRAM, static	Yes	352 BGA	Sixteen programmable 16 or 32-bit, watchdog, system bus monitor, system bus arbiter	50 GPIO, four programmable serial (UART, HDLC, SPI master /slave), USB host/device, 10/100 Ethernet, PCI/CardBus, 1284, I2C, LCD controller	Four external		-40 to +85	Four parallel JBIG decoders for single-pass and 4-pass color and monochrome laser printers	Call
256-kbyte SRAM, 32-kbyte dual-port RAM	64-bit ECC, 32, 64-bit DDR400	Yes	480, 672, 1053 FCBGA	Two 32-bit, 32-bit watchdog	Two to four FIFO/Ethernet, PCI 2.3 or PCI-X, one or two TDM, two UART, TWI, SPI, Host Port, eight GPIO, SysAD (on S5610)	8 GPIO		0 to +100	Instruction Set Extension Fabric	\$35 to \$100
RAM/cache mode, 8-kbyte RAM/data cache	64-bit SDRAM/DDR, Flash, burst Flash, SRAM, DRAM, five-channel DMA	64-entry fully-associative UTLB, four-entry fully associate microTLB	372 PBGA	Three 32-bit, real-time	Two UART, PCI, 24 PIO	17, four external, NMI		0 to +70 -40 to +85	JTAG, real-time trace	\$19.95 (166 MHz)

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
SuperH www.superh.com	SH4-202 CPU hard core SH4-202S CPU soft core	SHcompact compatible to Renesas SuperH and ST ST40	266 (worst case) at 0.13um standard technology	32/64 Super Hyway Inter connect	16	Process dependent	330mW	Sleep, standby, module standby, clock-domain control	Four 32x32 floating-point multipliers, three 32-bit floating-point adders, 2-cycle double load, 32-bit integer MAC operation	Single/double-precision, IEEE-754, matrix, 3-D vector, transcendental	16/32-kbyte instruction/data, two-way set associative, RAM/cache mode, LRU, write-back/write-through
	SH4-501S CPU soft core	SHcompact compatible to Renesas SuperH and ST ST40	240 to 266 (worst case) at 0.13um standard technology	32/64 Super Hyway Inter connect	16	Process dependent	0.41mW/MHz (8K/8K cache)	Sleep, standby, module standby, clock-domain control	2-cycle double load, 32-bit integer MAC operation		4- to 64-kbyte instruction/data (independently configurable), two way set associative, RAM/cache mode, LRU, write-back/write-through
Intel www.intel.com	IXP420	StrongARM V5TE	266	24/16	16, 32	0.3 to 2.1	1W	Stop, halt	40-bit accumulator DSP Co-processor		32-kbyte instruction/data, 32-way set associative, 2-kbyte mini data cache
	IXP421	StrongARM V5TE	266	24/16	16, 32	0.3 to 2.1	1W	Stop, halt	40-bit accumulator DSP Co-processor		32-kbyte instruction/data, 32-way set associative, 2-kbyte mini data cache
	IXP422	StrongARM V5TE	266	24/16	16, 32	0.3 to 2.1	1W	Stop, halt	40-bit accumulator DSP Co-processor		32-kbyte instruction/data, 32-way set associative, 2-kbyte mini data cache
	IXP425	StrongARM V5TE	266, 400, 533	24/16	16, 32	0.3 to 2.1	1W	Stop, halt	40-bit accumulator DSP Co-processor		32-kbyte instruction/data, 32-way set associative, 2-kbyte mini data cache
Renesas Technology www.renesas.com	SH-2 Series SH7047F	SuperH	50	32/32	16	4.5 to 5.5	220 to 235mA	Four	32x32+64		
	SH-2 Series SH7145F	SuperH	50	32/32	16	3.3	160 to 220mA	Four	32x32+64		
	SH-3 DSP Series SH7729	SuperH	200	32/32, external: 29	16	2/3.3	1W	Four	32x32+64		16-kbyte, four-way set associative
	SH-3 Series SH7705	SuperH	133	32/32, external: 29	16	1.5/3.3	250mW	Four	32x32+64		32-kbyte, four-way set associative
	SH-4 Series SH7750R	SuperH	240	32/64, external: 29	16	1.5/3.3	345mW	Four	32x32+64	Single- and double-precision	16/32-kbyte instruction/data
	SH-4 Series SH7751R	SuperH	240	32/32, external: 29	16	1.5/3.3	382mW	Four	32x32+64	Single- and double-precision	16/32-kbyte instruction/data

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
Application dependent	External, application dependent	64-entry fully-associative UTLB, four-entry fully associate microTLB	N/A - IP core	Three 32-bit, watchdog, real-time with alarm and calendar functions	Full-duplex serial with 16-byte send/receive FIFOs, modem control, baud rate generator	128+, four external, 16 levels	Application dependent	N/A (Core)	SuperHyWay VSI compliant interconnect, UDI (JTAG), 1-kbyte debug RAM, AUD trace, hardware break points	License
Application dependent	External, application dependent	64-entry fully-associative UTLB, four-entry fully associate microTLB	N/A - IP core	Optional three 32-bit, watchdog, real time with alarm and calendar functions	Optional Full-duplex serial with 16-byte send/receive FIFOs, modem control, baud rate generator	128+, four external, 16 levels	Application dependent	N/A (Core)	SuperHyWay VSI compliant interconnect, Optional UDI (JTAG), 1-kbyte debug RAM, Optional AUD trace, hardware break points	License
8-kbyte RAM	SRAM, Flash, PC133-SDRAM	32-entry TLB, full-way associative	492 PBGA	Four 32-bit, watchdog	Two UART, 32-bit 33/66-MHz PCI bus v2.2, USB 1.1, two 10/100 Ethernet, 16 GPIO	32, eight highest priority		0 to +70 -40 to +85	JTAG debug, Commercial and Extended temp devices available	\$15 and \$18
8-kbyte RAM	SRAM, Flash, PC133-SDRAM	32-entry TLB, full-way associative	492 PBGA	Four 32-bit, watchdog	Two UART, 32-bit 33/66-MHz PCI bus v2.2, USB 1.1, 10/100 Ethernet, ATM, UTOPIA II multi-PHY/slave, 16 GPIO	32, eight highest priority		0 to +70	Two HSS, JTAG debug, eight-channel HDLC	\$17.15
8-kbyte RAM	SRAM, Flash, PC133-SDRAM	32-entry TLB, full-way associative	492 PBGA	Four 32-bit, watchdog	Two UART, 32-bit 33/66-MHz PCI bus v2.2, USB 1.1, 16 GPIO, two 10/100 Ethernet	32, eight highest priority		0 to +70	AES/DES/DES3, SHA-1/MD-5, JTAG debug	\$16.72
8-kbyte RAM	SRAM, Flash, PC133-SDRAM	32-entry TLB, full-way associative	492 PBGA	Four 32-bit, watchdog	Two UART, 32-bit 33/66-MHz PCI bus v2.2, USB 1.1, 16 GPIO, two 10/100 Ethernet, ATM, UTOPIA II multi-PHY/slave	32, eight highest priority		0 to +70 -40 to +85	JTAG debug, two HSS, AES/DES/DES3, eight-channel HDLC	\$20.58 to \$39.44 (\$24.70 to \$47.30 Extended temperature range)
256-kbyte Flash, 12-kbyte RAM	ROM, SRAM		100 QFP	Two to five 16-bit, six-phase PWM, watchdog	Three serial, CAN	49, five external	Two eight channel 10-bit	-40 to +85	Data-transfer controller, on-chip debug	\$16
256-kbyte Flash, 8-kbyte RAM	SRAM, ROM, four-channel DMAC		144 LQFP	Two to five 16-bit, watchdog	Four serial, I2C	51, nine external	Eight channel 10-bit	-40 to +85	Data-transfer controller, on-chip debug	\$17
8-kbyte X and 8-kbyte Y	SDRAM, SRAM, ROM, four-channel DMAC	Yes	208 LQFP, 216 TTFBGA	Three 32-bit, real-time	Three serial, IrDA	27, 19 external	Eight channel 10-bit; two channel 8-bit DAC	-40 to +85	Smart-card interface, on-chip debug	\$19 to \$25
	SDRAM, SRAM, ROM, four-channel DMAC	Yes	208C FP, 208A TBP	Three 32-bit, three 16-bit, real-time, watchdog	Two serial, USB	27, 23 external	Four channel 10-bit	-40 to +85	Smart-card interface, on-chip debug	\$11.50 to \$13.50
	SDRAM, SRAM, ROM, eight-channel DMAC	Yes	208E FP, 256 BP	Three 32-bit, real-time	Two serial	34, 16 external		-40 to +85	Smart-card interface, on-chip debug	\$22
	SDRAM, SRAM, ROM, eight-channel DMAC	Yes	208E FP, 256 BP	Five 32-bit, real-time	Two serial, PCI	39, 16 external		-40 to +85	Smart-card interface, on-chip debug	\$25

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/ multiplication hardware support (bits)	FPU	Caching
Toshiba America Electronic Components www.toshiba.com	900/H1 family	TLCS	8 to 40	24/16	8, 16, 32	3 to 3.6	30	Idle2: 4.5mA, idle1: 2mA, stop: 1.0mA	16x16 to 32-bits signed/unsigned		
	900/H2 family	TLCS	20	24/16	8, 16, 32	4.5 to 5.5	90	Run: 50mA, idle: 5mA, stop: 0.5mA	16x16 to 32-bits signed/unsigned		
Infineon Technologies www.infineon.com/microcontrollers	TC1765	TriCore V1.2	40	32/16/8	16, 32	2.5/3.3 to 5	675mW	Idle, sleep, deep sleep	Dual MAC, bit-reverse, signed-fraction, modulo, saturation, pre/post-increment, rounding		1-kbyte instruction, two-way set associative
	TC1775	TriCore V1.2	40	32/16/8	16, 32	2.5/3.3 to 5	675mW	Idle, sleep, deep sleep	Dual MAC, bit-reverse, signed-fraction, modulo, saturation, pre/post-increment, rounding		1-kbyte instruction, two-way set associative
	TC1130	TriCore v1.3	150	32/16/8	16, 32	1.5 / 3.3	744mW	3mW, idle, sleep, deep sleep	Dual MAC, bit-reverse, signed-fraction, modulo, saturation, pre/post-increment, rounding	Single-precision	16/4-kbyte instruction/data
	TC111B	TriCore V1.3	96	32/16/8	16, 32	1.8/3.3	900mW	Idle, sleep, deep sleep	Dual MAC, bit-reverse, signed-fraction, modulo, saturation, pre/post-increment, rounding		8-kbyte instruction/data, two-way set associative
	TC1910	TriCore V1.3	66	32/16/8	16, 32	1.8/3.3		Idle, sleep, deep sleep	Dual MAC, bit-reverse, signed-fraction, modulo, saturation, pre/post-increment, rounding		8-kbyte instruction/data, two-way set associative
	TC1912	TriCore V1.3	66	32/16/8	16, 32	1.8/3.3		Idle, sleep, deep sleep	Dual MAC, bit-reverse, signed-fraction, modulo, saturation, pre/post-increment, rounding		8-kbyte instruction/data, two-way set associative
	TC1920	TriCore V1.3	100	32/16/8	16, 32	1.8/3.3		Idle, sleep, deep sleep	Dual MAC, bit-reverse, signed-fraction, modulo, saturation, pre/post-increment, rounding		8-kbyte instruction/data, two-way set associative
	Toshiba America Electronic Components www.toshiba.com	TMPR 3911BU 3911BxB	TX	58.9	13 to 26/ 16 to 32	32	2.6/3.3	150mW	Doze, sleep	One-cycle 32x32+64 MAC	
TMPR 3912AU-92 3912XB-92		TX	92	13 to 26/ 16 to 32	32	3.3	360mW	Doze, sleep	32x32+64 MAC		4/1-kbyte instruction/data, LRU, two-way set associative
TMPR 3922CU		TX	129	13 to 26/ 16 to 32	32	2.7/3.3	500mW	Doze, sleep	One-cycle 32x32+64 MAC		16/8-kbyte instruction/data, LRU, two-way set associative
TMPR 3927CF		TX	133	20 to 28/ 16 to 32	32	2.5/3.3	1.0W	Halt, doze, reduce frequency	One-cycle 32x32+64 MAC		8/4-kbyte instruction/data, LRU, two-way set associative

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
Up to 256-kbyte Flash/ROM, 32-kbyte RAM	SDRAM, eight micro DMA channels	Yes	100 LQFP, 144 LQFP	Up to eight 8-bit, up to two 16-bit, 22-bit, watchdog, real-time	Up to three UART, synchronous SIO, SEI, CAN, IrDA, I2C, up to 70 PIO	40, nine CPU, four external, seven levels	Up to 12 channel 10-bit		Four 32-bit register banks, LCD controller	\$5 to \$8
Up to 512-kbyte ROM, 16-kbyte RAM	Four micro DMA channels		100 QFP, 160 QFP, 100 LQFP	Up to eight 8-bit, up to four 16-bit, 22-bit watchdog	Two UART, synchronous SIO, two SEI, CAN, up to 70 PIO	18, 10 external, seven levels	Up to 12 channel 10-bit; two channel 8-bit DAC		Four 32-bit register banks	\$7.25 to \$10
48-kbyte SRAM	32-bit, glueless, burst mode, DMA		260 PLBGA	Three 32-bit, 34 24-bit, 64 16-bit	TwinCAN, two SSC/SPI, two ASC, 77 PIO, 24 analog input	More than +100 IRQ nodes	Dual 12 channel 8/10/12-bit	-40 to +125	Prescaler, duty cycle, phase discrimination, digital PLL	\$22
92-kbyte SRAM	32-bit, glueless, burst mode		329 PBGA	Three 32-bit, 34 24-bit, 64 16-bit	TwinCAN, J1850, two SSC/SPI, two ASC, 11 16-bit port	More than +100 IRQ nodes	Dual 16 channel 8/10/12-bit	-40 to +125	Peripheral-control processor, prescaler, duty cycle, phase discrimination, digital PLL	\$27
144-kbyte SRAM	8-, 16-, 32-bit, glueless, burst mode, SDRAM, PC100, PC133	Yes	208 PLBGA	Three 32-bit, four 16-bit, watchdog, system timer	Four CAN, 10/100 MII Ethernet, USB 1.1, three UART, two SPI, two I2C, two MLI, four 16-bit port, 8-bit port	95 Total		0 to +85	Two motor-control peripheral	\$14.75
1.5-Mbyte eDRAM, 68-kbyte SRAM	32-bit, glueless, burst mode, PC100	Yes	388 PBGA	Six 32-bit (usable as 8- and 16-bit)	PCI, fast Ethernet, SSC/SPI, ASC (IrDA), MMCI, 96 PIO	86, 24 external		-25 to +85	Peripheral control processor	\$65
144-kbyte SRAM	32-bit, glueless, burst mode	Yes	208 PLBGA	Three 32-bit	SSC/SPI, two ASC, I2C	More than +100 IRQ nodes	Dual 14-bit CODEC	-40 to +85	Peripheral control processor, PLL	\$18
144-kbyte SRAM	32-bit, glueless, burst mode	Yes	208 PLBGA	Three 32-bit	TwinCAN, SSC/SPI, three ASC, I2C	More than +100 IRQ nodes	Dual 14-bit CODEC	-40 to +85	Peripheral control processor, PLL	\$18.50
164-kbyte SRAM	32-bit, glueless, burst mode	Yes	260 PLBGA	Six 32-bit	TwinCAN, J1850, SSC/SPI, three ASC, two I2C	More than +100 IRQ nodes	Six channel 8/10/12-bit, dual 14-bit CODEC	-40 to +85	Peripheral control processor, PLL	\$27
	SDRAM, DRAM, SRAM, ROM, Flash	32-entry, 4-kbyte pages	176 LQFP, 177 BCSP	Real-time, watchdog	UART, CHI, IrDA, SPI, 39 PIO	Up to 39 external			Codec interface for softmodem, voice recognition/synthesis	\$9
	SDRAM, DRAM, SRAM, ROM, Flash	32-entry, 4-kbyte pages	208 LQFP, 217 FBGA	Real-time, watchdog	UART, CHI, IrDA, SPI, 39 PIO	Up to 39 external			Codec interface for softmodem, voice recognition/synthesis	\$15
	SDRAM, DRAM (EDO), SRAM, ROM, Flash	64-entry, 4-kbyte to 4-Mbyte pages	208 LQFP	Two, watchdog	UART, CHI, IrDA, SPI, 48 PIO	Up to 48 external			Companion chip TC6358TB	\$28
	SDRAM, SGRAM, DIMM Flash, SMROM, SRAM, ROM, DMA	64-entry, 4-kbyte to 4-Mbyte pages	240 PQFP	Three 32-bit, watchdog	Two UART, 16 PIO	Six external			Debug support unit	\$17

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/ multiplication hardware support (bits)	FPU	Caching
	TMPR3916F	TX	60	26/16 to 32	32	3.3	1.2W	Doze, sleep	One-cycle 32x32+64 MAC		4/1-kbyte instruction/data, direct map, two-way set associative
Uvicom www.ubicom.com	IP3023	Uvicom	250	22/8 Flash, 15/16 SDRAM (See Ser/Par I/O for other busses)	32	1.2/2.5 to 3.3, 5 tolerant	575mW	Runtime clock control, separate control of I/O and core PLLs	One-cycle 16x16+48-bit MAC		None, single-cycle program/data memory on-chip
NEC Electronics America www.necelam.com	V850/V850S	V800	2 to 33	24/16	32	2.7 to 5.5	56 to 480mW	Halt, idle, stop	16x16		
	V850E1	V800	2 to 150	24/16, 26/32	32	1.5 to 3.6/ 3 to 5.5	270 to 630mW	Halt, idle, stop	32x32		Yes
	V850ES/Kx1	V800	2 to 20	24/16	32	2.7 to 5.5	27 to 385mW	Halt, idle, stop	16x16		Yes
	V850ES/SAx	V800	2 to 20	24/16	32	2.2 to 5.5	30 to 105mW	Halt, idle, stop	16x16		Yes
AMD www.amd.com	Athlon 64	x86	1800 to 2200	16/16 Hyper Transport	variable (x86)	0.95 to 1.4 (1.2 HT)	81.5W TDP	ACPI C1/C2/C3		Yes	64/64-kbyte instruction/data, L2: 1-Mbyte
	Geode GX 466@0.9W	x86	333	internal: 32	32		0.9W			Integrated	16-kbyte instruction/data
	Geode GX 500@1.0W	x86	366	internal: 32	32		1W			Integrated	16-kbyte instruction/data
	Geode GX 533@1.1W	x86	400	internal: 32	32		1.1W			Integrated	16-kbyte instruction/data
	Geode NX 1500@6W	x86	1000	internal: 32	32	1	6W	3W (Stop Grant)		Integrated	384-kbyte
	Geode NX 1750@14W	x86	1400	internal: 32	32	1.25	14W	3.0W (Stop Grant)		Integrated	384-kbyte
	Low-Power Mobile Athlon 64	x86	1600 to 1800	16/16 Hyper Transport	variable (x86)	0.9 to 1.2 (1.2 HT)	35W TDP	ACPI C1/C2/C3		Yes	64/64-kbyte instruction/data, L2: 512-kbyte
	Mobile Athlon 64	x86	1600 to 2000	16/16 Hyper Transport	variable (x86)	1.1 to 1.5 (1.2 HT)	62W TDP	ACPI C1/C2/C3		Yes	64/64-kbyte instruction/data, L2: 1-Mbyte
Intel www.intel.com	80386EX 80386EXTB	x86	25, 33, 25	32, external: 26/16	32	3.3 to 5	250 to 320mA	Idle, powerdown			
	80386SSX 80386SX	x86	25, 33, 40		32	5					
	80486DX2 80486DX4	x86	50, 66 +100	32/32	32	3.3/ 5 tolerant	318 to 395mA, 825 to 1075mA	Stop, auto halt/idle powerdown		32-, 64-, 80-bit formats	8- or 16-kbyte instruction/data, write-back
	80486SX 80486GX 80486SSX	x86	33	32/16	32	3.3/ 5 tolerant	220 to 289mA, 180 to 220mA	Stop clock, auto halt powerdown			8-kbyte instruction/data, write-through
	Celeron	x86	300, 366, 433	32/32	32	2 (Variable VID)	17.8 to 24.1W	Autohalt, stopgrant, sleep, deepsleep		Yes	L2: 128-kbyte
	Celeron	x86	1200	32/32	32	1.5 (Variable VID)	32.1W	Autohalt, stopgrant, sleep, deepsleep		Yes	16-kbyte data, L2: 256-kbyte

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
	SDRAM, DRAM, SRAM, ROM, Flash, two DMA	32-entry, 4-kbyte pages	208 LQFP	Two 16-bit	Four UART, two-channel CAN (16 mailboxes), 30 PIO	Three external, NMI	Three channel 6-bit RGB DAC		Digital RGB	\$20
256-kbyte SRAM (program or data), 64-kbyte data SRAM	Flash, SDRAM		228 uBGA	Two 32-bit, 32-bit watchdog, can add timers	Four MII, two Serdes (10bT MAC/PHY, USB host/device, GPSI, SPI, UART). Soft I/O capable (PCMCIA, CF, IDE, MPEG-TS, PCI for 802.11a/g, UART, SPI, I2C, I2S, AC97	Up to 64	Analog squelch for 10base-T Ethernet PHY	0 to +70	Eight-way hardware multithreading, zero-cycle context switching, 32-bit random-number generator, software I/O supports interfaces via GPIO,	\$12
Up to 512-kbyte ROM/Flash, up to 24-kbyte SRAM	Four DMA		LQFP, FBGA	Up to 10 16-bit, four PWM	UART, CSI, I2C	12 external	Up to 16 channel 10-bit	-40 to +85		\$5.50 to \$15
Up to 128-kbyte ROM/Flash, up to 4-kbyte SRAM	EDO SDRAM, SRAM, four DMA		LQFP, FBGA	Up to 12 16-bit, six PWM	UART, CSI, I2C, USB	Up to 32 external	Up to eight channel 10-bit	-40 to +85	ROM correction	\$8 to \$24
Up to 256-kbyte ROM/Flash, up to 6-kbyte SRAM			LQFP, FBGA	Up to 10 16-bit	UART, LIN, CSI, I2C	Eight external	Up to six channel 16-bit; two channel 8-bit DAC	-40 to +85	ROM correction, POC, LVI, clock monitor, 240 khz on-chip osc	\$3 to \$10
Up to 256-kbyte ROM/Flash, up to 16-kbyte SRAM			LQFP, FBGA	Up to 10 16-bit	UART, CSI, I2C	Eight external	Up to six channel 16-bit	-40 to +85		\$4.50 to \$13
DDR400/333/266 /200	Integrated		754-pin uPGA, lidless					0 to +95	NX bit	
See cache	DDR SDRAM	256 entry TLB								\$26.50
See cache	DDR SDRAM	256 entry TLB								\$29.15
See cache	DDR SDRAM	256 entry TLB								\$32.75
See cache	SDRAM	256 entry TLB	453-Pin Socket A OPGA					-40 to +95		\$65
See cache	SDRAM	256 entry TLB	453-Pin Socket A OPGA					-40 to +95		\$55
DDR400/333/266 /200	Integrated		754-pin uPGA, lidless					0 to +95	NX bit	
DDR400/333/266 /200	Integrated		754-pin uPGA, lidless					0 to +95	NX bit	
	Refresh control unit		144 TQFP, 100/132 PQFP	32-bit down-counter, watchdog	UART, SIO, three 8-bit GPIO	10				\$8 to \$10.40
										\$5.12 to \$5.20
			208 SQFP, 168 PGA			Reset, maskable, NMI				\$15.20 to \$29.28
			168 PGA, 196 PQFP, 176 TQFP			Reset, maskable, NMI				\$28.75 to \$33.25; \$6.40 (SSX)
			370 PPGA					+5 to +85 (Tcase)	Streaming SIMD extensions	\$60
			370 FC-PGA2					+70 maximum	Streaming SIMD extensions	\$38

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/multiplication hardware support (bits)	FPU	Caching
	Celeron	x86	566, 733, 850	32/32	32	1.75 (Variable VID)	19.2 to 26.7W	Autohalt, stopgrant, sleep, deepsleep		Yes	L2: 128-kbyte
	Celeron	x86	2000, 2500	32/32	32	1.525 (Variable VID)	52.8 to 61W	Autohalt, stopgrant, sleep, deepsleep		Yes	8-kbyte data, L2: 128-kbyte
	Celeron Low Power	x86	300, 400	32/32	32	1.1 to 1.35	5.7 to 10.1W	Autohalt, stopgrant, sleep, deepsleep		Yes	L2: 128-kbyte
	Celeron Ultra Low Voltage	x86	400, 650	32/32	32	0.95 to 1.1	4.2 to 8.3W	Autohalt, stopgrant, sleep, deepsleep		Yes	L2: 256-kbyte
	Celeron M 320	x86	1300	32/32	32	1.356	24.5W	Autohalt, stopgrant, sleep, deepsleep		Yes	512-kbyte, L2: 512-kbyte
	Celeron M Ultra Low Voltage	x86	600	32/32	32	1.04	7W	Autohalt, stopgrant, sleep, deepsleep		Yes	512-kbyte, L2: 512-kbyte
	Pentium 4	x86	2000, 2400, 2600, 2800	36/32	32	1.525 (Variable VID)	54.3 to 68.4W	Autohalt, stopgrant, sleep, deepsleep		Yes	8-kbyte data, L2: 512-kbyte
	Pentium 4 M	x86	1700, 2200	36/32	32	1.3	30 to 35W	Autohalt, stopgrant, sleep, deepsleep, deeper sleep		Yes	8-kbyte data, L2: 512-kbyte
	Pentium 4 with Hyper-Threading	x86	3000	36/32	32	1.25 to 1.4 (Variable VID)	103W	Autohalt, stopgrant, sleep, deepsleep		Yes	8-kbyte data, L2: 1-Mbyte
	Pentium II Low Power	x86	266, 333	32/32	32	1.6	9.8 to 11.8W	Autohalt, stopgrant, sleep, deepsleep		Yes	L2: 256-kbyte
	Pentium III	x86	1260	32/32	32	1.45	29.5W	Autohalt, stopgrant, sleep, deepsleep		Yes	16-kbyte instruction/data, L2: 256- to 512-kbyte
	Pentium III	x86	600, 700, 733, 850, 866, +1000	32/32	32	1.75	19.6 to 29.5W	Autohalt, stopgrant, sleep, deepsleep		Yes	16-kbyte instruction/data, L2: 256- to 512-kbyte
	Pentium III Low Power	x86	800, 933	32/32	32	1.15	11.2 to 12.2W	Autohalt, stopgrant, sleep, deepsleep		Yes	16-kbyte instruction/data, L2: 256-kbyte
	Pentium III Low Power	x86	400, 500, 700	32/32	32	1.35	10.1 to 16.1W	Autohalt, stopgrant, sleep, deepsleep		Yes	16-kbyte instruction/data, L2: 256-kbyte
	Pentium M	x86	1100, 1600	32/32	32	1.18 to 1.484	12 to 24.5W			Yes	1-Mbyte, L2: 1-Mbyte
	Xeon	x86	2000, 2400, 2800	32/32	32	1.5	58 to 74W	Autohalt, stopgrant, sleep			512-kbyte, L2: 512-kbyte
	Xeon Low Voltage	x86	1600, 2000, 2400	32/32	32	1.3	30 to 40W	Autohalt, stopgrant, sleep			512-kbyte, L2: 512-kbyte

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
			370 FC-PGA					+80 to +90 maximum (Tjunction)	Streaming SIMD extensions	\$33 to \$42
			478 μ FC-PGA2					+68 to +72 maximum (Tcase)	Streaming SIMD extensions	\$64 to \$78
			495 BGA					0 to +100 (Tjunction)	Streaming SIMD extensions	\$45 to \$50
			479 μ FC-BGA					0 to +100 (Tjunction)	Streaming SIMD extensions	\$35 to \$94
			478 μ FC-PGA, 479 μ FC-BGA					0 to +100 (Tcase)	Dynamic execution, Streaming SIMD Extensions 2, 400 MHz source-synchronous FSB	\$130
			479 μ FC-BGA					0 to +100 (Tjunction)	Dynamic execution, Streaming SIMD Extensions 2, 400 MHz source-synchronous FSB	\$143
			478 FC-PGA2					+5 to +75 (Tcase)	Rapid execution engine, hyper pipelined, dynamic execution, SSE2 instructions, NetBurst microarchitecture	\$139 to \$180
			478 μ FC-PGA					+100 maximum (Tjunction)	Rapid execution engine, hyper pipelined, dynamic execution, SSE2 instructions, NetBurst microarchitecture	\$171 to \$196
			478 FCHPGA4					+5 to +73.5 (Tcase)	Rapid execution engine, hyper pipelined, dynamic execution, SSE2 instructions, NetBurst microarchitecture	\$252
			615 BGA					0 to +100 (Tjunction)	Quad Port Acceleration (QPA), ECC memory	\$85 to \$88
			370 FC-PGA2					+69 maximum (Tcase)	Streaming SIMD extensions	\$153
			370 FC-PGA					+75 to +82 maximum (Tjunction)	Dual-processor capable, streaming SIMD extensions	\$78 to \$115
			479 μ FC-BGA					0 to +100 (Tjunction)	Streaming SIMD extensions	\$187 to \$210
			495 BGA					0 to +100 (Tjunction)	Streaming SIMD extensions	\$77 to \$99
			478 μ FC-PGA, 479 μ FC-BGA					+100 maximum (Tjunction)	Supports up to 2-Gbyte of single channel DDR 333 memory	\$262 to \$292
			604 FCmPGA2p and 603 INT3					+70 to +75 maximum (Tcase)	Intel NetBurst microarchitecture, Hyperthreading	\$188 to \$220
			604 FCmPGA2p					+81 to +83 maximum (Tcase)	Intel NetBurst Architecture, Hyperthreading	\$204 to \$234

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Company name	Device name or family	Instruction set architecture	CPU frequency (MHz)	Bus interface (address/data) (bits)	Instruction width (bits)	Core / I/O operating voltages (V)	Typical power at maximum frequency	Powerdown modes and minimum power	DSP/ multiplication hardware support (bits)	FPU	Caching
STMicroelectronics www.st.com	STPC Atlas Consumer-II Elite	x86	66 to 133	64	32	2.5/3.3, 5 tolerant	3W	Three		8087 compatible, IEEE-754, single/double-precision	8-kbyte instruction/data or unified
	STPC Vega	x86	66 to 200	64	32	1.8/3.3, 5 tolerant	1.85W	Three		8087 compatible, IEEE-754, single/double-precision	8-kbyte instruction/data or unified
Transmeta Corporation www.transmeta.com	Crusoe TM5800 TM5500	x86	Up to +1000	32	32	0.9 to 1.3	Application Dependent	Auto-halt, quick start, deep sleep, DSX	Yes	Yes	64-kbyte instruction/data, L2: 512-kbyte
	Crusoe TM5900 TM5700	x86	Up to +1000	32	32	0.9 to 1.3	Application Dependent	Auto-halt, quick start, deep sleep, DSX	Yes	Yes	64-kbyte instruction/data, L2: 512-kbyte
	Efficeon TM8600	x86	Up to 1100	32	32	0.85 to 1.4	Application Dependent	Auto-halt, quick start, deep sleep, DSX	Yes	Yes	128/64-kbyte instruction/data, L2: 1-Mbyte
	Efficeon TM8620	x86	Up to 1100	32	32	0.85 to 1.4	Application Dependent	Auto-halt, quick start, deep sleep, DSX	Yes	Yes	128/64-kbyte instruction/data, L2: 1-Mbyte
VIA Technologies www.viatech.com	Antaur-M	x86	1000 to 1400	32/64	32	15 to 1.45	19W TDP	Autohalt, stopgrant, sleep, deepsleep		Yes	64-kbyte instruction/data, L2: 64-kbyte
	C3	x86	1000 to 1400	32/64	32	1.4	17.1W TDP	Autohalt, stopgrant		Yes	64-kbyte instruction/data, L2: 64-kbyte
	Eden ESP	x86	400 to +1000	32/64	32	15, 1.15	7W TDP	Autohalt, stopgrant		Yes	64-kbyte instruction/data, L2: 64-kbyte
	Eden-N	x86	533, 800, +1000	32/64	32	0.9, 0.95, 1	7W TDP	Autohalt, stopgrant, sleep, deepsleep		Yes	64-kbyte instruction/data, L2: 64-kbyte
Tensilica www.tensilica.com	Xtensa LX	Xtensa	350 (worst case 0.13)	32; general-purpose bus: 32, 64, 128; custom I/O: up to 1M	16, 24, 32, 64 modeless mix	Process dependent	0.075 mW/MHz base processor (0.13, 1V)	Powerdown during wait	3-issue, 4-way SIMD Vectra DSP co-processor, custom DSP instructions, options: 16x16 MAC, 16x16 and 32x32 multiply	Optional, IEEE-754 compatible	Configurable 0- to 32-kbyte instruction/data, four-way set associative
	Xtensa V	Xtensa	350 (worst case 0.13)	32/32, 64, 128	16, 24 modeless mix	Process dependent	0.1mW/MHz base processor (0.13, 1V)	Powerdown during wait	Five 16x16, 32x32 Vectra DSP co-processor options, user instructions, options: 16x16 MAC, 16x16 and 32x32 multiply	Optional, IEEE-754 compatible	Configurable 0- to 32-kbyte instruction/data, four-way set associative

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Memory	Memory controller	MMU	Package selection	Timers	Serial, Parallel I/O	Interrupts	ADC/DAC	Temperature ranges (degrees Celsius)	Additional features	Price (10,000)
	64-bit SDRAM UMA controller	PC Compatible	388 or 516 PBGA	PC-compatible	PCI, ISA, EIDE, PCMCIA, I2C, keyboard, mouse, USB, UART	PC- compatible		0 to +85 -40 to +115	VGA, SVGA, TFT controller, video input/output port	\$20 to \$30
	64-bit SDRAM controller	PC Compatible	388 PBGA	PC-compatible	PCI, ISA, EIDE, I2C, UART, USB Host, Ethernet	PC- compatible		0 to +85		\$28 to \$40
	64-bit DDR, SDR	Yes	474 BGA					0 to +100 (Tjunction)	MMX, LongRun Power Management	\$50 to \$100
	64-bit DDR	Yes	399 BGA					0 to +100 (Tjunction)	MMX, LongRun Power Management	\$50 to \$100
	64-bit DDR	Yes	783 BGA					0 to +100 (Tjunction)	MMX, SSE, SSE2, Enhanced LongRun Power Management, ECC Memory Support	\$75 to \$150
	64-bit DDR	Yes	592 BGA					0 to +100 (Tjunction)	MMX, SSE, SSE2, Enhanced LongRun Power Management, ECC Memory Support	\$75 to \$150
			EBGA					0 to +85 (Tcase)	3DNow!	\$70 to \$150
			EBGA					0 to +85 (Tcase)	Streaming SIMD extensions	\$50
			EBGA					0 to +85 (Tcase)	3DNow!	\$50 to \$100
			nanoBGA					0 to +85 (Tcase)	3DNow!	\$85 to \$150
Configurable local for instruction/data, up to 256-kbyte RAM and ROM, XLMI interface to memories or tightly coupled hardware		Configurable region protection	N/A - IP core	Up to three 32-bit	Up to one-million custom I/O ports	Up to 32		N/A (Core)	Automated processor- generation system creates new processor and tool suite in one hour	License
Configurable local for instruction/data, up to 256-kbyte RAM and ROM, XLMI interface to memories or tightly coupled hardware		Optional and configurable	N/A - IP core	Up to three 32-bit		Up to 32		N/A (Core)	Automated processor- generation system creates new processor and tool suite in one hour	License