



# 2004 EDN Microcontroller/Microprocessor directory

## 64-BIT MICROPROCESSORS

| Company name  | Device name or family | Instruction set architecture | CPU frequency (MHz) | Bus interface (address/data) (bits) | Instruction width (bits) | Core / I/O operating voltages (V) | Typical power at maximum frequency | Powerdown modes and minimum power                  | DSP/ multiplication hardware support (bits)  | FPU  | Caching   |
|---|-----------------------|------------------------------|---------------------|-------------------------------------|--------------------------|-----------------------------------|------------------------------------|--|--|--|---|
| PMC-Sierra<br>Microprocessor<br>Products Division<br><a href="http://www.pmc-sierra.com/processors">www.pmc-sierra.com/processors</a> | RM5261A               | MIPS IV                      | 250, 300, 350, 400  | 64                                  | 32                       | 1.65, 1.8/2.5, 3.3                | Less than 1W (400MHz)              | Standby  | MAC/MAD/MADU, multiply (three-operand and cycle)                                   | One/two-cycle rate single/double-precision IEEE-754        | 32-kbyte instruction/data, two-way set associative  |
|   | RM7000C               | MIPS IV                      | 533, 600            | 64                                  | 32                       | 1.5/2.5/3.3                       | 2.5W (600MHz)                      | Standby  | MAD/MADU, multiply (three-operand and cycle)                                       | Single/double-precision IEEE-754                           | 16-kbyte instruction/data, L2: 256-kbyte, four-way set associative, line locking, write back/through            |
|   | RM7065C               | MIPS IV                      | 300, 466, 533, 600  | 64                                  | 32                       | 1.5/2.5/3.3                       | 2.5W (600MHz)                      | Standby  | MAD/MADU, multiply (three-operand and cycle)                                       | Single/double-precision IEEE-754                           | 16-kbyte instruction/data, L2: 256-kbyte, four-way set associative, line locking, write back/through            |
|   | RM5231A               | MIPS IV                      | 250, 300, 350, 400  | 32                                  | 32                       | 1.65, 1.8/2.5, 3.3                | Less than 1W (400MHz)              | Standby  | MAC/MAD/MADU, multiply (three-operand and cycle)                                   | One/two-cycle rate single/double-precision IEEE-754        | 32-kbyte instruction/data, two-way set associative  |
| MIPS Technologies<br><a href="http://www.mips.com">www.mips.com</a>   | 20Kc                  | MIPS64                       | 600                 | 64/64                               | 64                       | 1                                 | 2.5mW/MHz (0.13)                   | Wait   | 32x32, 32x64, 64x64  | 64-bit paired-single with MIPS-3D                          | 32-kbyte instruction/data   |
|   | 5Kc<br>5Kf            | MIPS64                       | 310 to 350          | 64/64                               | 64                       | Process dependent                 | 0.17 to 1mW/MHz                    | Wait   | 32x32, 32x64, 64x64  | Optional, IEEE-754-compliant                               | 0- to 64-kbyte instruction/data   |
| NEC Electronics<br>America<br><a href="http://www.necelam.com">www.necelam.com</a>  | VR4133                | MIPS64                       | 266                 | 32                                  | 16                       | 1.5/3.3                           | 370mW                              | Full speed, standby, suspend, exsuspend, hibernate | IPSec engine   |  | 16-kbyte instruction/data   |
|   | VR5500A               | MIPS64                       | 300 to 400          | 64, external: 64, 32 option         | 32                       | 1.5/3.3                           | 1.5W                               | Standby  | MAC, 32x32 and 64x64 floating point, integer multiply, integer multiply-accumulate | IEEE-754, 64/32-bit floating-point arithmetic and multiply | 32-kbyte instruction/data, two-way set associative, line locking, four pending instructions, blocking, prefetch |
|   | VR7701                | MIPS64                       | 400                 | 64                                  | 32                       | 1.5/2.5 or 3.3                    | 4W                                 | Standby  | MAC, 32x32 and 64x64 floating point, integer multiply, integer multiply-accumulate | IEEE-754, 64/32-bit floating-point arithmetic and multiply | 32-kbyte instruction/data, two-way set associative, line locking, four pending instructions, blocking, prefetch |
| PMC-Sierra<br>Microprocessor<br>Products Division<br><a href="http://www.pmc-sierra.com/processors">www.pmc-sierra.com/processors</a> | RM7035C               | MIPS64                       | 300, 466, 533, 600  | 32                                  | 32                       | 1.5/2.5/3.3                       | 2.5W (600MHz)                      | Standby  | MAD/MADU, multiply (three-operand and cycle)                                       | Single/double-precision IEEE-754                           | 16-kbyte instruction/data, L2: 256-kbyte, four-way set associative, line locking, write back/through            |
|   | RM7900                | MIPS64                       | 668, 750, 835, 900  | 64                                  | 32                       | 1.5/2.5/3.3                       | 5W (900MHz)                        | Standby  | MAD/MADU, Multiply/Subtract, multiply (three-operand and cycle)                    | Single/double-precision IEEE-754                           | 16-kbyte instruction/data, L2: 256-kbyte, four-way set associative, line locking, write back/through, ECC       |

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| Memory       | Memory controller                                    | MMU   | Package selection           | Timers                   | Serial, Parallel I/O   | Interrupts                              | ADC/DAC | Temperature ranges (degrees Celsius) | Additional features   | Price (10,000) |
|--------------|--|---|-----------------------------|--------------------------|--|---|---------|--------------------------------------|---|----------------|
|              |  | 48 dual-entry TLB, 96 pages, 4-kbyte to 16-Mbyte                    | 208 QFP<br>216 Exposed Pad  |                          | 64-bit SysAD   | Six, NMI                                |         | -45 to +85<br>0 to +85<br>0 to +70   |   | \$12 to \$18   |
|              | L3 cache controller for up to 8-Mbyte external cache | 64/48 dual-entry TLB, 128/96 pages                                  | 304 TBGA                    | 32-bit counter           | 64-bit SysAD   | 10 external, two internal, two software |         | 0 to +70<br>0 to +85                 |   | \$77 to \$87   |
|              |  | 64/48 dual-entry TLB, 128/96 pages                                  | 256 TBGA<br>216 Exposed Pad | 32-bit counter           | 64-bit SysAD   | 10 external, two internal, two software |         | 0 to +70<br>-40 to +85<br>0 to +85   |   | \$41 to \$75   |
|              |  | 48 dual-entry TLB, 96 pages, 4-kbyte to 16-Mbyte                    | 128 QFP<br>128 Exposed Pad  |                          | 32-bit SysAD   | Six, NMI                                |         | -45 to +85<br>0 to +85<br>0 to +70   |   | \$12 to \$18   |
| Configurable | Optional   | 48 dual-entry jTLB, 8-entry uTLB, 4-kbyte to 16-Mbyte pages         | N/A - IP core               |                          |  |   |         | N/A (Core)                           | Full custom hard core, dual-issue seven-stage pipeline  | License        |
| Configurable | Optional   | 16, 32, or 48 dual-entry jTLB with variable page size, optional FMT | N/A - IP core               |                          |  |   |         | N/A (Core)                           | Synthesizable core, coprocessor interface   | License        |
|              | 133-MHz SDRAM  | 32 dual-entry TLB, fully associative, 4-kbyte to 1-Gbyte page size  | 240 FPBGA                   | Real-time, watchdog      | Two 16550-compatible, serial debugging, synchronous three-line serial clock, 32/66MHz PCI v2.3 | Yes                                     | Yes     | -40 to +85                           | Clock-generator unit  | \$25           |
|              | 133-MHz SDRAM  | 48 dual-entry TLB, fully associative, 4-kbyte to 1-Gbyte page size  | 272 BGA                     | Two 32-bit for 11 events |  | 6-bit addressing                        |         | -40 to +85                           | Dual-issue superscalar, DSP instruction, JTAG, N-Wire/N-Trace, 64 and 32-bit SysAD bus, clock modes from x2 to x5.5 | \$35 to \$42   |
|              | 133-MHz SDRAM<br>PC266 DDR<br>64-bit                 | 48 dual-entry TLB, fully associative, 4-kbyte to 1-Gbyte page size  | 500 BGA                     | Two 32-bit for 11 events | Two UART, clocked serial interface   | 6-bit addressing                        |         | -40 to +85                           | Dual-issue superscalar, L2 cache interface  | \$97           |
|              |  | 64/48 dual-entry TLB, 128/96 pages                                  | 128 Exposed Pad             | 32-bit counter           | 32-bit SysAD   | 10 external, two internal, two software |         | 0 to +70<br>0 to +85                 |   | \$35 to \$72   |
|              | L3 cache controller for up to 8-Mbyte external cache | 64/48 dual-entry TLB, 128/96 pages                                  | 304 EPBGA                   | Two 32-bit counters      | 64-bit SysAD   | 10 external, two internal, two software |         | 0 to +70<br>0 to +85                 | ECC on L2 cache, on-chip EJTAG  | \$104 to \$158 |

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|---|-------------------------------------|------------------------------|---------------------|--|--------------------------|-----------------------------------|--|-----------------------------------|---|---|---|
|   | RM7935                              | MIPS64                       | 668, 750, 835, 900  | 32   | 32                       | 1.5/2.5/3.3                       | 5W (900MHz)                              | Standby                           | MAD/MADU, Multiply/Subtract, multiply (three-operand and cycle) | Single/double-precision IEEE 754            | 16-kbyte instruction/data, L2: 256-kbyte, four-way set associative, line locking, write back/through, ECC |
|   | RM7965                              | MIPS64                       | 668, 750, 835, 900  | 64   | 32                       | 1.5/2.5/3.3                       | 5W (900MHz)                              | Standby                           | MAD/MADU, Multiply/Subtract, multiply (three-operand and cycle) | Single/double-precision IEEE 754            | 16-kbyte instruction/data, L2: 256-kbyte, four-way set associative, line locking, write back/through, ECC |
|   | RM9000x1 (RM9100)                   | MIPS64                       | 800, +1000          | 64/8, local: 8, 16, 32; 8 Hyper-Transport, 64 SysAD                        | 32                       | 1.2, 2.5, 3.3                     | Less than 5W (maximum with peripherals)  | Standby                           | 64-bits   | IEEE-754                                    | 16-kbyte instruction/data, L2: 256-kbyte, four-way set associative, ECC                                   |
|   | RM9000x1GL (RM9124, RM9122, RM9120) | MIPS64                       | 800, +1000          | 64/8, local: 8, 16, 32; 8 Hyper-Transport, 64 SysAD, 32 PCI                | 32                       | 1.2, 2.5, 3.3                     | 7.5W                                     | Standby                           | 64-bits   | IEEE-754                                    | 16-kbyte instruction/data, L2: 256-kbyte, four-way set associative, ECC                                   |
|   | RM9000x2 (RM9200)                   | MIPS64                       | 800, +1000          | 64/8, local: 8, 16, 32; 8 Hyper-Transport, 64 SysAD                        | 32                       | 1.2, 2.5, 3.3                     | Less than 10W (maximum with peripherals) | Standby                           | 64-bits   | IEEE-754                                    | 16-kbyte instruction/data per core, L2: 256-kbyte, ECC, four-way set associative                          |
|   | RM9000x2GL (RM9224, RM9222, RM9220) | MIPS64                       | 800, +1000          | 64/8, local: 8, 16, 32; 8 Hyper-Transport, 64 SysAD, 32 PCI                | 32                       | 1.2, 2.5, 3.3                     | 12W                                      | Standby                           | 64-bits   | IEEE-754                                    | 16-kbyte instruction/data per core, L2: 256-kbyte, ECC, four-way set associative                          |
|   | RM9150                              | MIPS64                       | 600 to +1000        | 64 DDRI/DDRII SDRAM, 8 Hyper-Transport, two GE, two 32 PCI, PL3, Local Bus | 32                       | 1.2, 2.5, 3.3                     | 5 to 8W                                  | Standby                           | 64-bits   | IEEE-754                                    | 16-kbyte instruction/data, L2: 256-kbyte, four-way set associative, ECC                                   |
| Toshiba America Electronic Components<br><a href="http://www.toshiba.com">www.toshiba.com</a> | TMPR 4925XB                         | MIPS64                       | 200                 | 20 to 28/ 8 to 64  | 32                       | 1.5/3.3                           | 0.9W                                     | Halt, doze, reduce frequency      | One-cycle 64x64 MAC   | IEEE-754-compliant, single/double-precision | 16-kbyte instruction/data, four-way set associative, FIFO, lock   |
|   | TMPR 4926XB                         | MIPS64                       | 200                 | 20 to 28/ 8 to 32  | 32                       | 1.5/3.3                           | 0.9W                                     | Halt, doze, reduce frequency      | One-cycle 64x64 MAC   | IEEE-754-compliant, single/double-precision | 16-kbyte instruction/data, four-way set associative, FIFO, lock   |
|   | TMPR 4927ATB-200                    | MIPS64                       | 200                 | 20 to 28/ 8 to 64  | 32                       | 1.5/3.3                           | 1.2W                                     | Halt                              | One-cycle 64x64 MAC   | IEEE-754-compliant, single/double-precision | 32-kbyte instruction/data, two-way set associative, FIFO, lock  |
|   | TMPR 4937XB                         | MIPS64                       | 300                 | 20 to 28/ 8 to 32  | 32                       | 1.5/3.3                           | 1.2W                                     | Halt                              | One-cycle 64x64 MAC   | IEEE-754-compliant, single/double-precision | 32-kbyte instruction/data, two-way set associative, FIFO, lock  |

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|--|--|---|-----------------------------|-----------------------------------|---|---|---------|--------------------------------------|--|----------------|
|  |  | 64/48 dual-entry TLB, 128/96 pages                | 128 Exposed Pad             | Two 32-bit counters               | 32-bit SysAD  | 10 external, two internal, two software |         | 0 to +70<br>0 to +85                 | ECC on L2 cache, on-chip EJTAG   | \$85 to \$130  |
|  |  | 64/48 dual-entry TLB, 128/96 pages                | 256 TBGA<br>216 Exposed Pad | Two 32-bit counters               | 64-bit SysAD  | 10 external, two internal, two software |         | 0 to +70<br>0 to +85                 | ECC on L2 cache, on-chip EJTAG   | \$92 to \$137  |
| 8-kbyte scratch RAM linear address mapping | DDR, SDRAM, DMA, 200-MHz DDR                 | 64 dual-entry TLB, 4-kbyte to 256-Mbyte page size | 896 FCBGA                   | Performance counters              | HyperTransport, SysAD   | 256 prioritized                         |         | 0 to +85                             | Can DMA packet header to L2 cache and put remainder into main memory                 | \$159 to \$200 |
| 8-kbyte scratch RAM linear address mapping | DDR, SDRAM, DMA, 200-MHz DDR                 | 64 dual-entry TLB, 4-kbyte to 256-Mbyte page size | 672 FCBGA<br>896 FCBGA      | Performance counters              | Two UART, 2BI, PCI, GPI, HyperTransport, three 10/100/1000 Ethernet | 10 external, NMI, 256 levels, intra-CPU |         | 0 to +85                             | Can DMA packet header to L2 cache and put remainder into main memory                 | \$212 to \$250 |
| 8-kbyte scratch RAM linear address mapping | DDR, SDRAM, DMA, 200-MHz DDR                 | 64 dual-entry TLB, 4-kbyte to 256-Mbyte page size | 896 FCBGA                   | Performance counters              | HyperTransport, SysAD   | 256 prioritized, CPU to CPU             |         | 0 to +85                             | Dual CPU Cores. Can DMA packet header to L2 cache and put remainder into main memory | \$244 to \$370 |
| 8-kbyte scratch RAM linear address mapping | DDR, SDRAM, DMA, 200-MHz DDR                 | 64 dual-entry TLB, 4-kbyte to 256-Mbyte page size | 672 FCBGA<br>896 FCBGA      | Performance counters              | Two UART, 2BI, PCI, GPI, HyperTransport, three 10/100/1000 Ethernet | 10 external, NMI, 256 levels, intra-CPU |         | 0 to +85                             | Dual CPU Cores. Can DMA packet header to L2 cache and put remainder into main memory | \$326 to \$450 |
| 32-kbyte scratch                           | 200 MHz DDRI/DDRII SDRAM                     | 64 dual-entry TLB, 4-kbyte to 256-Mbyte page size | 896 FCBGA                   | Four general-purpose, watchdog    | HyperTransport, two GE, two PCI, DUART                              | 256 vectored                            |         | 0 to +85                             |  | \$120 to \$180 |
|  | Four-channel SDRAM, NOR/NAND Flash, DMA      | 48-entry fully associative TLB                    | 256 PBGA                    | Three 32-bit, real-time, watchdog | PCI 2.2 32-bit, 33-MHz, two serial, up to 32 PIO, SPI, ACLC, PCMCIA | Seven external, NMI                     |         |                                      | EJTAG debug  | \$18           |
|  | Four-channel SDRAM, NOR/NAND Flash, ROM, DMA | 48-entry fully associative TLB                    | 256 PBGA                    | Three 32-bit, real-time, watchdog | PCI 2.2 32-bit, 33-MHz, two serial, up to 32 PIO, SPI, ACLC, PCMCIA | Seven external, NMI                     |         |                                      | DES/3DES, EJTAG debug  | \$20           |
|  | Four-channel SDRAM, NOR Flash, ROM           | 48-entry fully associative TLB                    | 420 TBGA                    | Three 32-bit, watchdog            | PCI 2.1 32-bit, 66-MHz, two serial, up to 16 PIO, ACLC              | Five external, NMI                      |         |                                      | EJTAG debug  | \$25           |
|  | Four-channel SDRAM, NOR Flash, ROM, DMA      | 48-entry fully associative TLB                    | 484 PBGA                    | Three 32-bit, watchdog            | PCI 2.2 32-bit, 66-MHz, two serial, up to 16 PIO, ACLC              | Five external, NMI                      |         |                                      | EJTAG debug  | \$32           |

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|---|-------------------------------|--|---|-------------------------------------|--------------------------|-----------------------------------|------------------------------------|---|---|---|--|
|   | TMPR 4938XB                   | MIPS64   | 300   | 20 to 28/ 8 to 32                   | 32                       | 1.5/3.3                           | 1.2W                               | Halt  | One-cycle 64x64 MAC   | IEEE-754-compliant, single/double-precision                           | 32-kbyte instruction/data, two-way set associative, FIFO, lock   |
|   | TMPR 4955AF-200<br>4955BF-300 | MIPS64   | 200, 300  | 32                                  | 32                       | 1.5/3.3                           | 450 or 600mW                       | Halt, doze  | One-cycle 64x64 MAC   | IEEE-754-compliant, single/double-precision                           | 32-kbyte instruction/data, two-way set associative, FIFO, lock   |
|   | TMPR 4955CF                   | MIPS64   | 350, 400, 450   | 32                                  | 32                       | 1.2/3.3                           | 600mW                              | Halt, doze  | One-cycle 64x64 MAC   | IEEE-754-compliant, single/double-precision                           | 32-kbyte instruction/data, two-way set associative, FIFO, lock   |
|   | TMPR 4956CXB                  | MIPS64   | 350, 400, 450   | 64/32                               | 32                       | 1.2/3.3                           | 700mW                              | Halt, doze  | One-cycle 64x64 MAC   | IEEE-754-compliant, single/double-precision                           | 32-kbyte instruction/data, two-way set associative, FIFO, lock   |
|   | TMPR 7901XB                   | MIPS64   | 200   | 64                                  | 32                       | 1.5/3.3                           | 2W                                 | Halt  | One-cycle 64x64 MAC   | IEEE-754-compliant, single/double-precision                           | 32-kbyte instruction/data, two-way set associative, FIFO, lock   |
| <a href="http://www.superh.com">SuperH<br/>www.superh.com</a> | SH4-401S CPU soft core        | SHcompact compatible to Renesas SuperH and ST ST40           | 240 to 266 (worst case) at 0.13um standard technology | 32/64 Super Hyway Inter connect     | 16                       | Process dependent                 | 0.38mW/MHz (8K/8K cache)           | Sleep, standby, module standby, clock-domain control                                  | 2-cycle double load, 32-bit integer MAC operation   |   | 4- to 64-kbyte instruction/data (independently configurable), two way set associative, RAM/cache mode, LRU, write-back/write-through |
|   | SH4-450S CPU soft core        | SHcompact compatible to Renesas SuperH and ST ST40           | 133 (worst case) at 0.13um standard technology        | 32/64 Super Hyway Inter connect     | 16                       | Process dependent                 | 0.32mW/MHz (8K/8K cache)           | Sleep, standby, module standby, clock-domain control                                  | 2-cycle double load, 32-bit integer MAC operation   |   | 4- to 64-kbyte instruction/data (independently configurable), two way set associative, RAM/cache mode, LRU, write-back/write-through |
|   | SH5-103 CPU hard core         | SHcompact compatible to Renesas SuperH and ST ST40 & Shmedia | 400 (worst case) at 0.13um standard technology        | 32/64 Super Hyway Inter connect     | 16, 32                   | 1.2                               | Less than 400mW                    | Economy, sleep, quick wakeup standby, deep standby, module stop, clock-domain control | Two-, four- and eight-way SIMD packed arithmetic in 64-bit registers, permute, shuffle, extract, conversion | Single/double-precision, IEEE-754, matrix, 3-D vector, transcendental | 32-kbyte instruction/data, four-way set associative, cache locking, LRU, write-back/write-through                                    |
| <a href="http://www.amd.com">AMD<br/>www.amd.com</a>          | Athlon 64                     | x86  | 1800 to 2200  | 16/16 Hyper Transport               | variable (x86)           | 0.95 to 1.4 (1.2 HT)              | 81.5W TDP                          | ACPI C1/C2/C3   |   | Yes   | 64/64-kbyte instruction/data, L2: 1-Mbyte  |
|   | Low-Power Mobile Athlon 64    | x86  | 1600 to 1800  | 16/16 Hyper Transport               | variable (x86)           | 0.9 to 1.2 (1.2 HT)               | 35W TDP                            | ACPI C1/C2/C3   |   | Yes   | 64/64-kbyte instruction/data, L2: 512-kbyte  |
|   | Mobile Athlon 64              | x86  | 1600 to 2000  | 16/16 Hyper Transport               | variable (x86)           | 1.1 to 1.5 (1.2 HT)               | 62W TDP                            | ACPI C1/C2/C3   |   | Yes   | 64/64-kbyte instruction/data, L2: 1-Mbyte  |

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|-----------------------|--|--|-----------------------|--|---|--------------------------------|-----------------------|--------------------------------------|--|----------------|
|                       | Four-channel SDRAM, NAND/NOR Flash, ROM, DMA | 48-entry fully associative TLB                                       | 484 PBGA              | Three 32-bit, watchdog   | PCI 2.2 32-bit, 66-MHz, ACLC, SPI, two EtherMAC, two serial, up to 16 PIO                       | Five external, NMI             |                       |                                      | EJTAG debug  | \$36           |
|                       |  | 48 dual-entry TLB  | 160 QFP               |  |   | Six external                   |                       |                                      | EJTAG debug  | \$10 to \$15   |
|                       |  | 48 dual-entry TLB  | 160 QFP               |  |   | Six external                   |                       |                                      | EJTAG debug  | \$22           |
|                       |  | 48 dual-entry TLB  | 217 FPBGA             |  |   | Six external                   |                       |                                      | EJTAG debug  | \$25           |
|                       | Four-channel SDRAM, DMA                      | 48-entry fully associative TLB                                       | 484 PBGA              | Three 24-bit, watchdog   | Dual PCI 2.2 32-bit 33/66-MHz, two EtherMAC, two serial, SPI                                    | Seven external, NMI            |                       |                                      | JTAG   | \$30           |
| Application dependent | External, application dependent              |  | N/A - IP core         | Optional three 32-bit, watchdog, real time with alarm and calendar functions | Optional Full-duplex serial with 16-byte send/receive FIFOs, modem control, baud rate generator | 128+, four external, 16 levels | Application dependent | N/A (Core)                           | SuperHyway VSI compliant interconnect, Optional UDI (JTAG), 1-kbyte debug RAM, Optional AUD trace, hardware break points | License        |
| Application dependent | External, application dependent              |  | N/A - IP core         | Optional three 32-bit, watchdog, real time with alarm and calendar functions | Optional Full-duplex serial with 16-byte send/receive FIFOs, modem control, baud rate generator | 128+, four external, 16 levels | Application dependent | N/A (Core)                           | SuperHyway VSI compliant interconnect, Optional UDI (JTAG), 1-kbyte debug RAM, Optional AUD trace, hardware break points | License        |
| Application dependent | External, application dependent              | 64-entry fully associative UTLB, four-entry fully associate microTLB | N/A - IP core         | Three 32-bit, watchdog, real time with alarm and calendar functions          | Full duplex serial with 16-byte send and receive FIFOs, modem control, baud rate generator      | Up to 64                       | Application dependent | N/A (Core)                           | SuperHyway VSI compliant interconnect, SHdebug runtime control and trace on-chip debugging with watchpoints              | License        |
| DDR400/333/266 /200   | Integrated                                   |  | 754-pin uPGA, lidless |  |   |                                |                       | 0 to +95                             | NX bit   |                |
| DDR400/333/266 /200   | Integrated                                   |  | 754-pin uPGA, lidless |  |   |                                |                       | 0 to +95                             | NX bit   |                |
| DDR400/333/266 /200   | Integrated                                   |  | 754-pin uPGA, lidless |  |   |                                |                       | 0 to +95                             | NX bit   |                |