

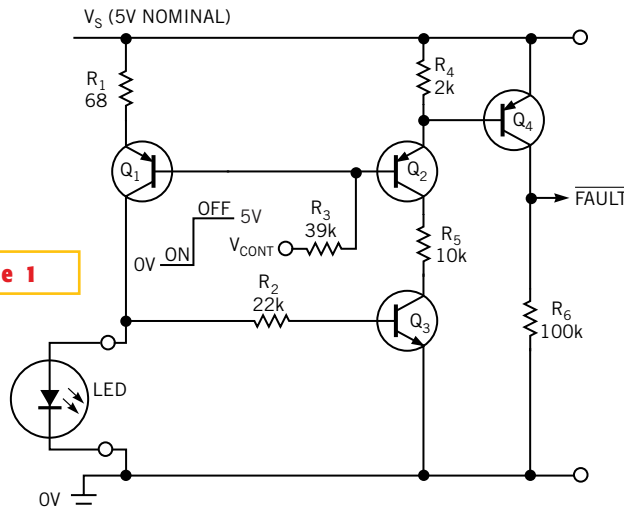
Edited by Bill Travis

## LED driver doubles as fault monitor

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LEDs find wide use as indicators and as light emitters in devices such as optocouplers. In some applications, the LED or the emitter may be located remotely at some distance from the main unit. Typical examples are dashboard-mounted automotive indicators and industrial optosensors. In critical applications, you may require some means of monitoring the integrity of the LED. Using just four transistors and six resistors, this circuit provides switchable, constant-current drive for an LED and indicates both open- and short-circuit fault conditions (Figure 1). And there's a bonus, too. Control signal  $V_{CONT}$  switches the LED on and off. When  $V_{CONT}$  is high,  $Q_1$  and the LED are off. When  $V_{CONT}$  is as low as 0V,  $Q_1$  turns on and sources a constant current to the LED. Because most LEDs have a

**Figure 1**



**This LED driver doubles as a fault monitor and limits short-circuit current to boot.**

forward-voltage drop of at least 1.2V, adequate base-bias voltage exists for  $Q_3$ , which turns on, thereby providing a conduction path for  $Q_2$ . This conduction, in turn, provides bias for  $Q_4$ , which turns on

and pulls high, thus indicating a healthy LED.

Because  $Q_2$  and  $Q_4$  are both now on, the base potential of  $Q_1$  sits at roughly two  $V_{BE}$  drops below the positive-supply rail,  $V_S$ , thereby placing one  $V_{BE}$  drop

diately turns off and deprives  $Q_2$  of collector current.  $Q_2$ 's base-emitter junction now behaves like a diode, clamping  $Q_1$ 's base to a potential dictated mainly by  $Q_2$ 's  $V_{BE}$  drop and by the ratio of  $R_3$  to  $R_4$ . Because  $R_4$ 's value is smaller than

that of  $R_3$ ,  $Q_2$ 's emitter potential now rises toward  $V_S$ . Once again,  $Q_4$  turns off and goes low to indicate the fault condition. With the resistor values shown in Figure 1,  $Q_1$ 's base now sits at approximately 4V, leaving only 200 to 300 mV across  $R_1$ . Therefore, the short-circuit current is effectively "choked back" to less than a third of the normal value, thereby saving power—the bonus. Under normal conditions, with the LED on,  $Q_1$  conducts more current than  $Q_2$ , causing its  $V_{BE}$  drop to be slightly larger than that of  $Q_2$ . Consequently, the potential across  $R_1$  is slightly less than a diode drop, and you

may need to experiment with the value of  $R_1$  to set the desired LED current.

You must select  $R_3$  to satisfy the base-current requirements of  $Q_1$  and  $Q_2$  when  $V_{CONT}$  is low. Tests on the prototype circuit produced good results with  $R_3 = 39$  kΩ, although a smaller value may be required, depending on the LED current and the current gain of  $Q_1$  and  $Q_2$ . When the LED is on, both  $Q_2$  and  $Q_3$  are fully on, so a reasonably large value of  $R_5$  is required to limit their joint collector current to an acceptable level. However,  $R_5$  must not be too large, or  $Q_2$  will be unable to furnish the current that  $R_4$  and  $Q_4$ 's base require. Making  $R_5$  approximately four or five times larger than  $R_4$  is a good starting point.

Although the circuit in Figure 1 has a

across  $R_1$ . Consequently, with  $R_1 = 68\Omega$ ,  $Q_1$  sources a steady current of approximately 10 mA to the LED. Provided that the value of  $R_2$  is large enough, little of the LED's forward current diverts into  $Q_3$ 's base. As long as the LED remains undamaged, FAULT stays high, signaling normal drive conditions. Should the LED go open-circuit,  $Q_1$ 's collector load becomes just  $R_2$  in series with  $Q_3$ 's base. Because  $R_2$  is much larger than  $R_1$ ,  $Q_1$  saturates, the voltage across  $R_1$  falls to around 20 mV or so, and the emitter potentials of  $Q_1$  and  $Q_2$  rise toward  $V_S$ . With insufficient base drive,  $Q_4$  now turns off, and the output falls to 0V to signal the fault condition.

On the other hand, if a fault puts a short circuit across the LED,  $Q_3$  imme-

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5V supply, you could use other voltages, provided that you scale the resistor values accordingly. Operation at lower voltages is possible as long as  $Q_1$  has adequate “headroom” to stay out of

saturation, but beware of problems if you use a blue or a white LED, because these devices tend to have relatively high forward-voltage drops. The transistor types are not critical; most small-signal

devices with high current gain should be adequate, although  $Q_1$  may need to be a power device if your design requires a high LED current, a high supply voltage, or both. □

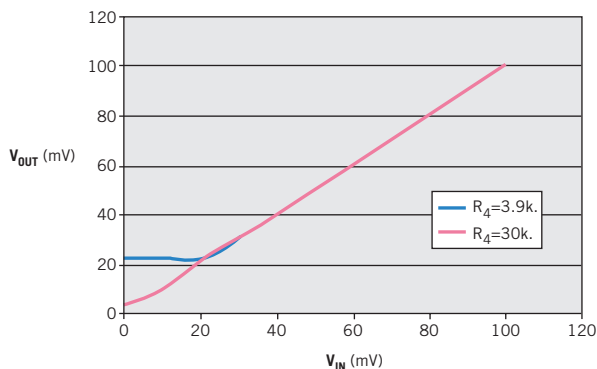
# Current source enables op amp’s output to go to ground

Frank Chan, Vancouver, BC, Canada

**T**HE LM324 is a cost-effective choice for an op amp, especially when you need to apply ground-level inputs. Although its output purportedly includes ground, its poor current-sinking capability limits the applications. At output voltages lower than 0.5V, the op amp’s sinking current ranges only from 2 to 100  $\mu$ A. You can add an external current-sinking circuit to bring the usable output

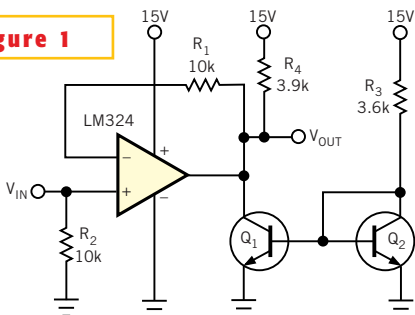
voltage down to the millivolt level. In **Figure 1**,  $Q_1$ ,  $Q_2$ , and  $R_3$  form a 4-mA current source that drains the output of the LM324.  $R_4$  is the load, demanding a sink current of 4 mA. This design

uses a 2N2222 transistor for its low saturation voltage. The output characteristic becomes the saturation characteristic of the added transistors,  $Q_1$  and  $Q_2$ . Using this current source, the output voltage is linear down to 22 mV above ground. **Figures 2** and **3** show the output characteristics. The lowest usable output voltage depends on the load (sink) current. When the load current is 0.5 mA ( $R_4 = 30$  k $\Omega$ ), the output

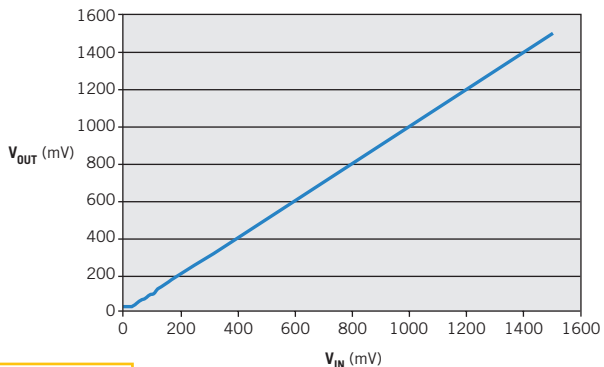


**Figure 3** With 0.5-mA load current, the output voltage is linear down to 4 mV.

**Figure 1**

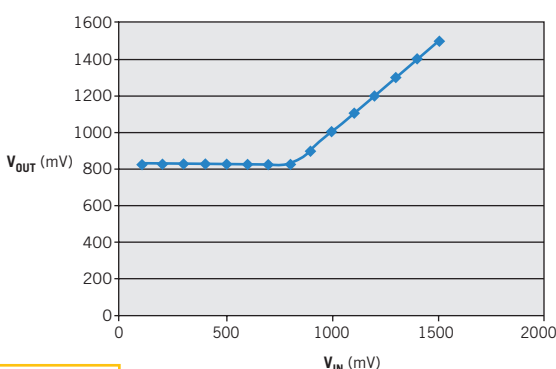


An external current source can bring the usable output level of an LM324 down to the millivolt level.



**Figure 2** The transfer function of Figure 1’s circuit is linear down to the low-millivolt level.

is linear down to 4 mV. **Figure 4** is the original output characteristic of the LM324 driving  $R_4$  (3.9 k $\Omega$ ) without the added sinking current source. The current source presents a constant load to the LM324. You can configure a leftover op amp as a voltage comparator to cut off the current source when the output voltage is higher than 1V. □

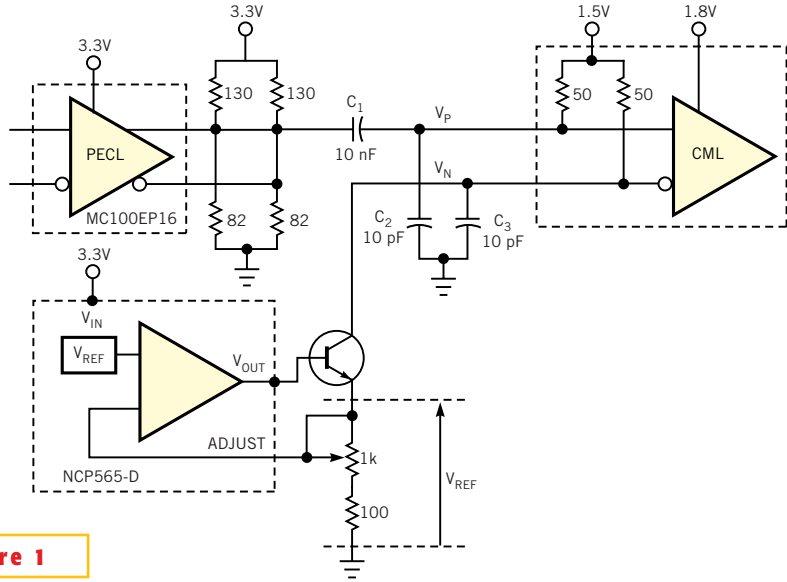


**Figure 4** This graphic shows the LM324 transfer function without the added current source.

# Circuit distorts duty cycle for CML inputs

Dieter Verhulst and Xin Yin, Ghent University, Belgium

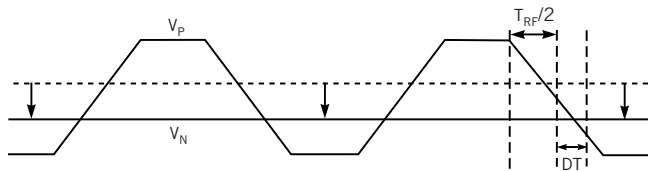
**T**O TEST A GIGABIT-SPEED data-recovery chip, you need a clock with a controllable duty cycle. Because most pattern and clock generators have a fixed duty-cycle output of 50%, the design may require a small circuit to distort the duty cycle. The signal with controllable duty cycle drives a standard CML (current-mode-logic) input with on-chip termination resistors. One side,  $V_p$ , of the differential CML input takes single-ended drive from a PECL (positive-emitter-coupled-logic) circuit (Figure 1). The other input,  $V_n$ , connects to a controllable dc voltage. If this dc voltage is equal to the average voltage of the single-ended signal, the duty cycle stays 50%. If the signal has nonzero rise and fall times ( $T_{RF}$ ), you can distort the duty cycle by lowering the dc



**Figure 1**

This circuit can make slight adjustments to the duty cycle you apply to a CML input.

voltage (Figure 2). The distortion generated is equal to the time difference between the crossing of the single-ended signal and its average and the crossing between the single-ended signal and the set dc voltage (DT). Thus, the theoretical maximum distortion that you can generate is  $T_{RF}$ .



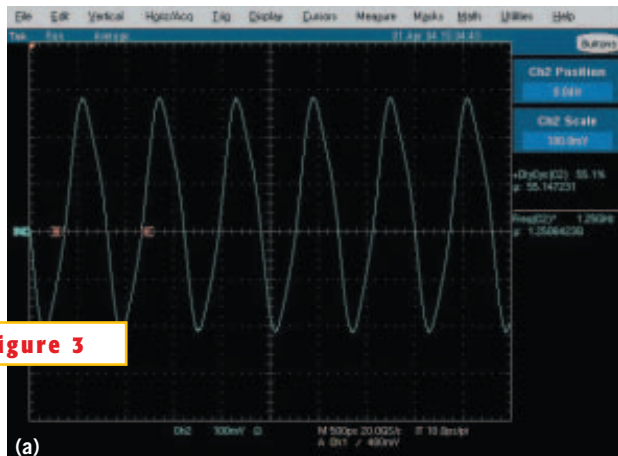
**Figure 2**

By exploiting the rise and fall time of a signal and manipulating a dc bias voltage, you can control the duty cycle of a CML signal.

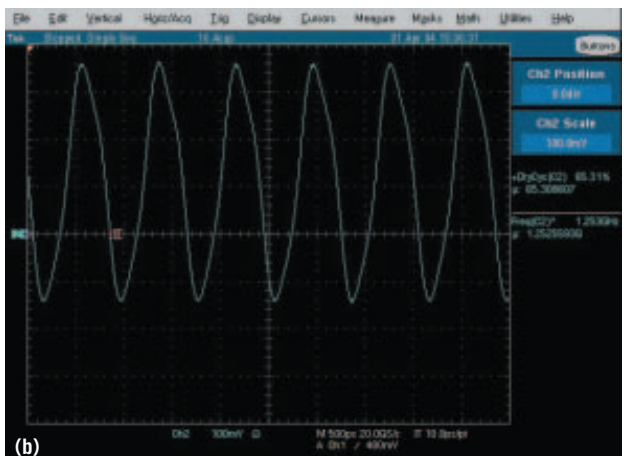
You can control  $T_{RF}$  by selecting a buffer with the desired  $T_{RF}$  value, the MC00EP16 buffer in this design, and by changing the output capacitance for this buffer ( $C_2$ ). To set the voltage at node  $V_n$ , the design uses the internal termination resistors and a controllable current

source instead of applying a dc voltage source. This procedure makes the circuit more immune to power-supply changes.

Because the single-ended signal is ac-coupled, the average voltage of this signal at node  $V_p$  is equal to the internal ter-



**Figure 3**



This photo shows duty cycles of 55.1% (a) and 65.3% (b).

mination voltage of the CML input. If no current enters the  $V_N$  input, this node also assumes the internal termination voltage, and the duty cycle is 50%. This voltage is independent of the average voltage of the single-ended signal at the buffer's output and the internal termination voltage.

The NCP565-D voltage reference, using a reference voltage,  $V_{REF}$ , of 0.9V,

creates a stable, controllable current source. The buffer inside the reference drives the bias voltage of an npn transistor and changes it until the voltage at Adjust is equal to  $V_{REF}$ . The current pulled through the transistor and the  $V_N$  input is equal to  $V_{REF}/R$ . R is the resistance between the emitter of the transistor and ground. Changing R changes this current, the voltage at  $V_N$ , and,

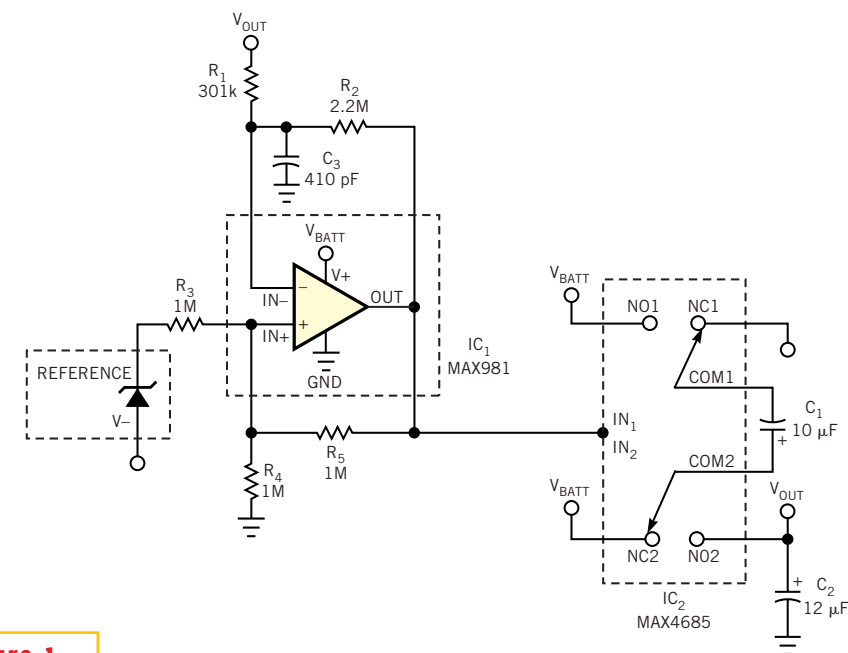
therefore, the duty cycle for the signal that the CML input sees. The circuit was tested with a 1.25-GHz clock. **Figure 3** shows the waveforms of the differential signal ( $V_p - V_N$ ) at the CML input set at 55% (**Figure 3a**) and 65% (**Figure 3b**). The described circuit increases the duty cycle; if the duty cycle needs to decrease, you'd connect the single-ended signal to  $V_N$  and the current source to  $V_p$ . □

## Build a charge pump with ultralow quiescent current

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**P**ORTABLE BATTERY-powered devices often spend most of their life in standby mode, in which the quiescent current of an internal boost converter continuously bleeds the battery. The quiescent current during standby can be larger than the actual load current. Though several inductor-based converters offer maximum quiescent current of less than 10  $\mu$ A, designers usually prefer or require a regulated charge pump for cost-sensitive designs that must be intrinsically safe. Off-the-shelf regulated charge pumps with output-current capabilities of at least 10 mA have typical minimum quiescent currents of 50 to 100  $\mu$ A. If that level of quiescent current is unacceptable, you can reduce the overall average by adding circuitry that remotely monitors the regulated voltage and toggles the charge pump into and out of shutdown. That approach, however, may not achieve the desirable quiescent-current level of less than 10  $\mu$ A. The advent of low-on-resistance analog switches and ultralow-current comparators and references makes possible a charge-pump circuit whose maximum quiescent current is approximately 7  $\mu$ A (**Figure 1**).

Charge pumps use an ac-coupling technique to transfer energy from a transfer capacitor to a storage capacitor. The transfer capacitor first charges via analog switches to the level of  $V_{BATT}$ , and then other analog switches transfer the



**Figure 1**

This charge-pump circuit uses analog switches to achieve ultralow quiescent current.

energy to a storage capacitor tied to  $V_{OUT}$ . The transfer capacitor then charges again, and the cycle repeats. With ideal analog switches exhibiting zero loss, the  $V_{OUT}$  level equals two times  $V_{BATT}$ . As expected, however, the analog switches' finite on-resistance produces an output level that drops in proportion to the load current. The basic regulated charge pump in **Figure 1** includes an oscillator, several analog switches, a volt-

age reference, and a comparator. The comparator serves as a voltage monitor and an oscillator. When the circuit is in regulation, the comparator output is low, which closes the NC (normally closed) switches and allows  $C_1$  to charge to  $V_{BATT}$ . When the voltage at  $V_{OUT}$  dips below the output-regulation threshold—3.3V in this case—the comparator output goes high. The NO (normally open) switches close, transferring  $C_1$ 's

charge to  $C_2$ . This cycle repeats until  $V_{OUT}$  regains regulation.

Resistors  $R_3$  to  $R_5$  provide the hysteresis necessary for oscillation. Their value,  $1\text{ M}\Omega$ , creates a notable level of hysteresis and minimizes  $V_{BATT}$  loading. As the comparator output changes state, feedback resistor  $R_5$  creates hysteresis by moving the threshold you apply to the comparator's positive input. For the resistor values shown, reference value nominal for  $IC_1$  ( $1.182\text{V}$ ), and  $V_{BATT}=3\text{V}$ , the  $V_{IN+}$  threshold swings between approximate values of  $V_{IN+}(\text{low})=0.39\text{V}$  and  $V_{IN+}(\text{high})=1.39\text{V}$ . When the circuit is in regulation,  $V_{IN-}$  slightly exceeds  $V_{IN+}$ , the comparator output is low, the  $R_1$ - $R_2$  divider senses the voltage at  $V_{OUT}$ , and the threshold at  $V_{IN+}$  is low ( $0.39\text{V}$ ). With  $V_{IN+}$  at  $0.39\text{V}$ , you can calculate the  $R_1$  and  $R_2$  values from the equation

$V_{IN+}=V_{OUT}[R_2/(R_1+R_2)]$ . The resistance of  $R_1+R_2$  should be greater than  $1\text{ M}\Omega$  to minimize  $V_{BATT}$  loading. If  $V_{OUT}=3.3\text{V}$  and  $R_2$  is  $2.2\text{ M}\Omega$ ,  $R_1$  calculates to  $301\text{ k}\Omega$ . Capacitor  $C_3$  connects to the comparator's  $V_{IN-}$  input. Along with  $R_1$  and  $R_2$ ,  $C_3$  sets the oscillation frequency according to the following simplified relationships:  $t_{DISCHARGE}=t_{LOW}=-\text{ln}[(V_{IN+}(\text{LOW})/(V_{IN+}(\text{HIGH})))]/(R_2C_3)$ ;  $t_{CHARGE}=t_{HIGH}=-\text{ln}[1-(V_{IN+}(\text{HIGH})-V_{IN+}(\text{LOW}))/(V_{BATT}-V_{IN+}(\text{LOW}))]$ ; and  $f_{OSC}=1/t_{PERIOD}$ , where  $t_{PERIOD}=t_{LOW}+t_{HIGH}$ .

To maximize efficiency and reduce the effects of comparator slew rate, you should set a relatively low frequency. Choosing  $C_3=470\text{ pF}$  yields the following:  $t_{LOW}=178\text{ }\mu\text{sec}$ , and  $t_{HIGH}=68\text{ }\mu\text{sec}$ ; thus,  $f_{OSC}=4\text{ kHz}$ .

Select the values of  $C_1$  and  $C_2$  to achieve the desired load current and rip-

ple. For this application ( $I_{LOAD}=10\text{ mA}$ ),  $C_1=10\text{ }\mu\text{F}$ . To calculate the value of  $C_2$ , make an approximation based on the desired ripple voltage:  $C_2=(I_{LOAD}\times t_{LOW})/V_{RIPPLE}$ . With  $I_{LOAD}=10\text{ mA}$  and  $V_{RIPPLE}=150\text{ mV}$ ,  $C_2=12\text{ }\mu\text{F}$ .

With these component values, the circuit draws a maximum quiescent current of  $6.9\text{ }\mu\text{A}$  and offers a considerable improvement over off-the-shelf charge pumps. You can further lower the quiescent current by increasing the resistor values, but that effect is minimal because  $IC_2$ 's maximum quiescent current of  $3.8\text{ }\mu\text{A}$  dominates the total. This circuit lets you implement an ultralow-quiescent-current-regulated charge pump. Until off-the-shelf options are available, it provides an alternative for designers seeking to implement a low-cost design without the use of inductors. □