

Edited by Bill Travis

## Dual-voltage regulator meets USB-power needs

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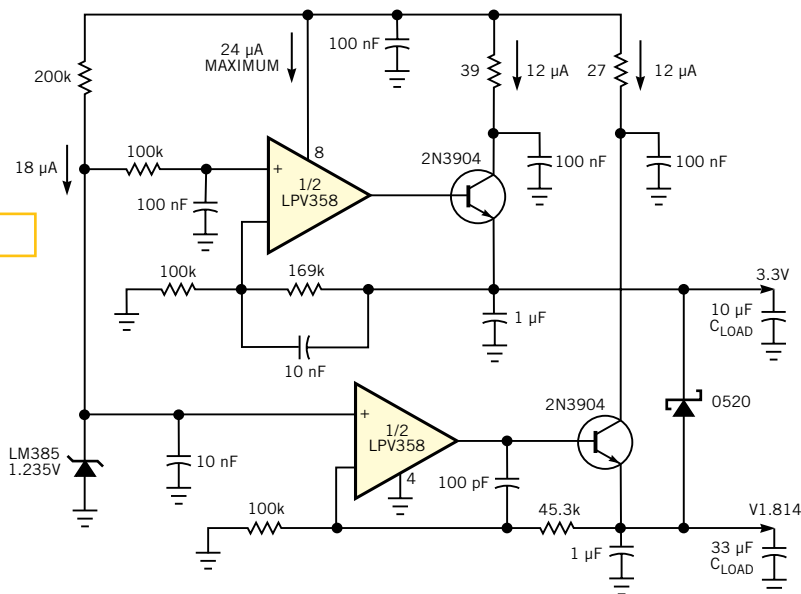
**T**HIS DESIGN IDEA stems from the limited availability of IC voltage regulators that can meet key USB-power specs, coupled with the need for turn-on sequencing and rise-time control at each output. As always, for PC-related designs, minimum cost is a primary motivation. USB specs require all loads to limit inrush current to less than 100 mA plus 50  $\mu$ C of charge when powered on. If permission is granted to increase the load to 500 mA, inrush limiting may be required again to prevent excursions over the 500-mA limit. The other troublesome USB-power requirement is the “suspend”-current maximum of 500  $\mu$ A, of which you may use only 250  $\mu$ A; a termination resistor requires the rest. Suspend requires the load to power down but keep alive just enough to listen for permission to power up again. So, the sum of the regulators’ operating currents plus load current must be less than 250  $\mu$ A. The dual-regulator circuit meets the USB spec and powers an ASIC

**Figure 1**

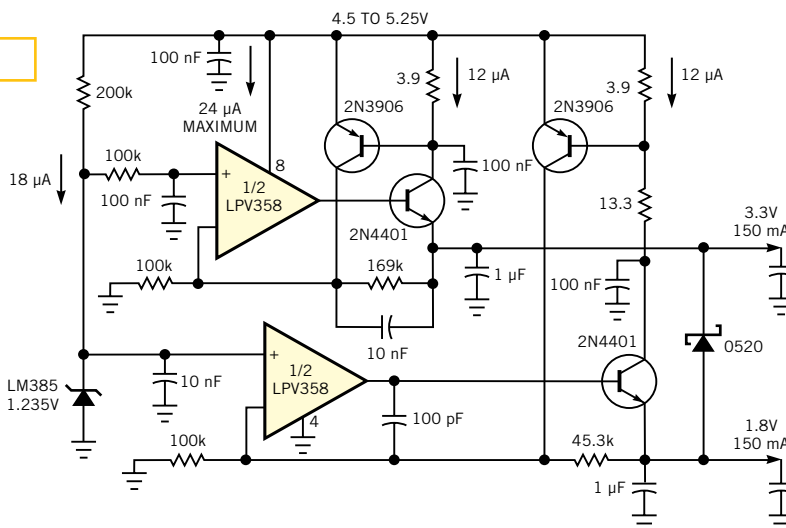
that requires a core voltage of 1.8V and I/O voltage of 3.3V to rise with a controlled sequence and slew rate (Figure 1). Specifically, the core and I/O voltages track within 0.5V until the core voltage reaches 1.8V. The controlled slew rate limits inrush current to less than 100

**Figure 2**

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This circuit meets USB specs for controlled power-up sequence and slew rate.



This configuration boosts the output current of Figure 1’s circuit to more than 200 mA.

mA. Two micropower linear regulators use a very-low-power bandgap voltage reference and a dual op amp. The dual op amp must draw low power, have inputs active to ground, provide rail-to-rail

drive, and not reverse polarity as you apply power. Each op amp has an npn transistor buffering its output to provide greater than 100 mA. The regulator loops are stable with these components and

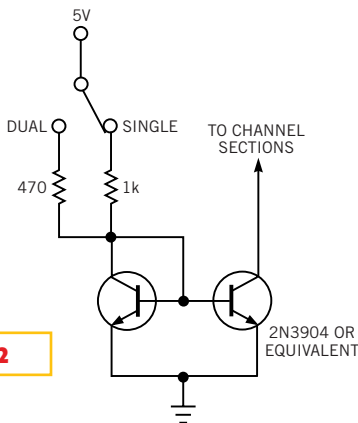


sic “active-channel” indication.

The operating principle of this circuit is based on current steering. A current sink comprising an n-channel JFET, the BF256C, provides approximately 5-mA current draw, which is approximately the hold current of any one of the small-signal SCRs (silicon-controlled rectifiers). When you select a channel by momentarily depressing the corresponding switch, the associated SCR turns on, lighting the LED connected to its cathode and providing a

logic one on the CHANx line. The SCR automatically latches the selected line until you depress another channel switch. When you actuate any other channel switch, the corresponding SCR latches, releasing the previous channel. This latch behavior is the result of the inability of the current sink to draw enough current to sustain more than one SCR at a time.

The circuit needs blocking diodes to isolate the cathodes of the SCRs. If you use an LED, as in Figure 1, it also doubles as an “active-channel” indicator. You can



**Figure 2**

A current mirror replaces the JFET in Figure 1 and allows the choice of single or dual channels.

use the CHANx line to select an analog switch, a mechanical relay, or another device. Scalability is straightforward: Additional channel sections require only the momentary switch, a 1.5-kΩ resistor, an SCR, and a diode. Because this method uses a current-based scheme, the use of long lines is not an issue. Channel

sections can be across control rooms. Upon initial power-up, all channels are in the off-state. In addition, Figure 1 shows an optional reset-all pushbutton. Depressing the reset-all switch steers the entire current sink’s capacity through this switch, thus delatching any SCR that was active.

You can substitute other n-channel JFETs, but you must accordingly scale the drain current of the chosen JFET by varying the value of  $R_1$ . You can easily modify this circuit to allow more than one SCR to be active at a given time. For a multiple-active-channel system, you must set the current level to activate only the number of SCRs desired and no more. For example, a system with two active channels would require a current level of 8 to 10 mA in the current sink. Figure 2 shows a possible alternative current sink, replacing the JFET and  $R_1$ , for this arrangement. If you use indicating LEDs in a multiple-channel arrangement, you should take proper precautions with maximum LED current. □

## Phone-line-voltage monitor meets FCC specs

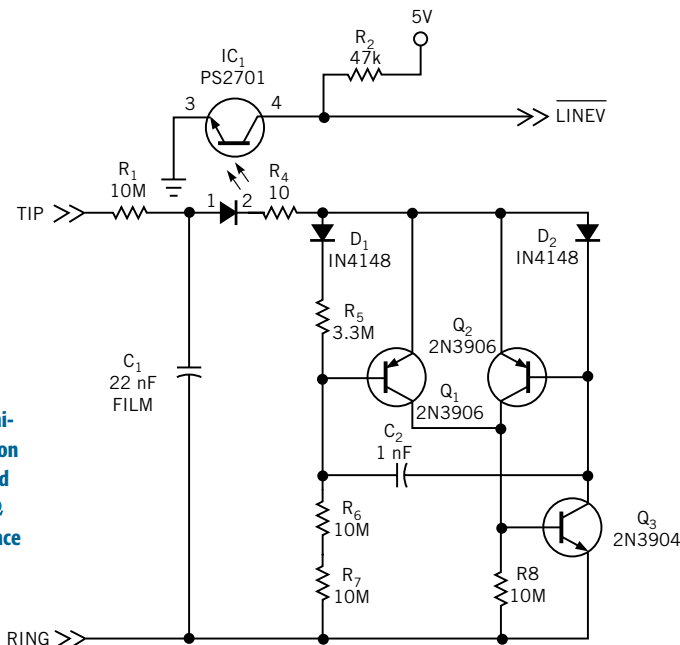
Brad Peeters, Theta Engineering, Costa Mesa, CA

WHEN YOU DESIGN equipment that interfaces to a phone line, it is often desirable to be able to monitor the dc voltage on the line. This ability can be useful, for example, to determine whether a line is in use before attempting to go off-hook and possibly interrupting somebody’s phone call. FCC regulations place strict limits on the amount of leakage current an on-hook device can draw from a phone line. The specifications work out to approximately the equivalent of 5 MΩ as the minimum leakage resistance. So, you have the challenge of monitoring the line voltage without exceeding the regulatory limits and also maintaining the galvanic isolation required between the phone line and your equipment. The circuit in Figure 1 shows a method of meeting this challenge with 100% margin. In other

(continued on pg 76)

**Figure 1**

This circuit monitors dc voltage on a phone line and presents 10-MΩ leakage resistance across the line.



words, it presents approximately 10-M $\Omega$  leakage resistance across the line.

The basic relaxation oscillator has the LED of an optoisolator in the discharge path of the main capacitor. It delivers a pulse train, the frequency of which varies with the voltage on the phone line. By measuring the period between pulses, the equipment's microcontroller can easily determine the approximate line voltage.  $C_1$  is the timing capacitor. It should be a film-type capacitor rather than ceramic for good results. It slowly charges through  $R_1$ , a 10-M $\Omega$  resistor. When the voltage across  $C_1$  reaches approximately 3V, the remainder of the circuit turns on, causing  $C_1$  to rapidly discharge through  $R_4$  and the optoisolator's LED. This action causes the optoisolator's output transistor to briefly turn on, creating a low-going pulse approximately 200  $\mu$ sec wide (the signal labeled  $\overline{\text{LINEV}}$ ). This width is sufficient for even a slow microcontroller to capture an interrupt. When  $C_1$  discharges to approximately 1.5V, the circuit turns off, and the cycle repeats.

$Q_2$  and  $Q_3$  form an SCR (silicon-controlled-rectifier)-like regenerative pair.  $D_2$  and  $Q_2$  function basically as a current mirror. Normally, you construct a current mirror using two or more identical transistors. By using a 1N4148 diode rather than another 2N3906, you reduce the gain of the current mirror to well below unity. The 1N4148 functions as though it has many times the base-emitter diode area of the 2N3906. Reducing the gain in this fashion helps the regenerative pair to turn off at the appropriate point, keeping the oscillator from "sticking" on.  $Q_1$  and the diode-resistor network driving its base function as the trigger circuit. When the voltage across  $C_1$  gets high enough,  $Q_1$  starts to turn on and inject current into  $Q_3$ . Once  $Q_3$  starts to turn on, regeneration kicks in, and  $Q_3$  and  $Q_2$  turn on hard and stay turned on until the capacitor discharges sufficiently.  $C_2$  provides additional positive feedback through  $Q_1$ ; it im-

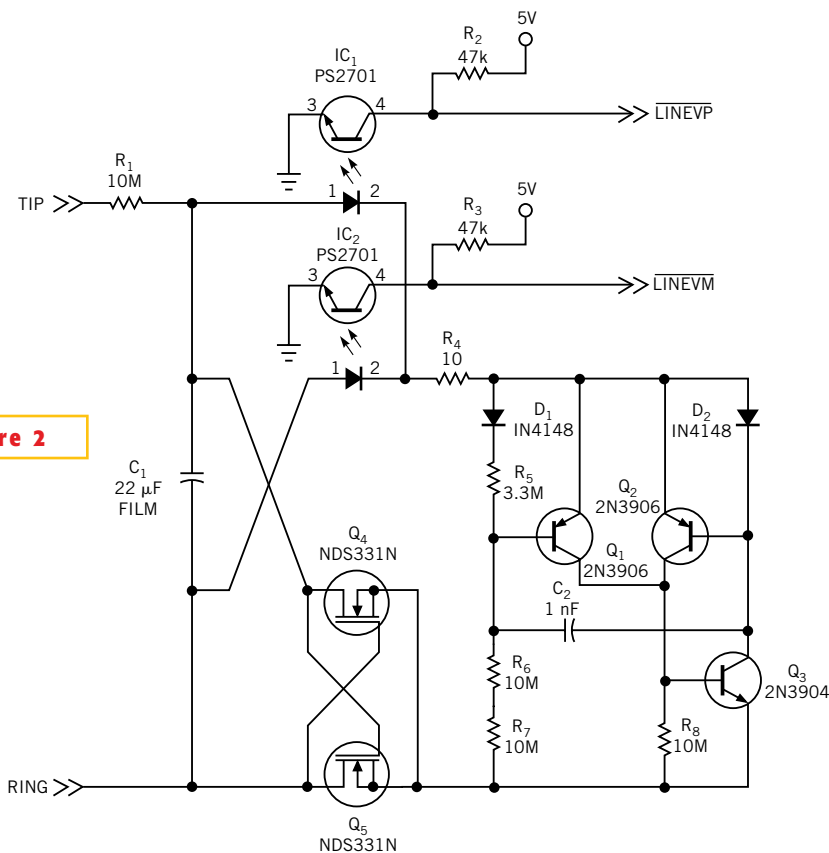


Figure 2

This circuit works with either the Tip or the Ring polarity and reports the polarity of the line to the host microcontroller.

proves the operating characteristics of the circuit.

This circuit assumes that Tip and Ring have protection against polarity reversal such that Tip is always more positive. The circuit of Figure 2 works with either po-

larity and reports the polarity of the line to the host microcontroller. This circuit is suitable when you need to know not only the magnitude, but also the polarity of the line voltage. As you can see, it has two outputs, one for each polarity.  $Q_4$

and  $Q_5$  are low-threshold n-channel MOSFETs, connected in such a way as to always connect the bottom rail of the relaxation circuit to the most negative side of the timing capacitor. The positive rail of the relaxation circuit connects to the most positive side of the timing capacitor using diode isolation, taking advantage of the fact that the optoisolator LEDs are diodes.

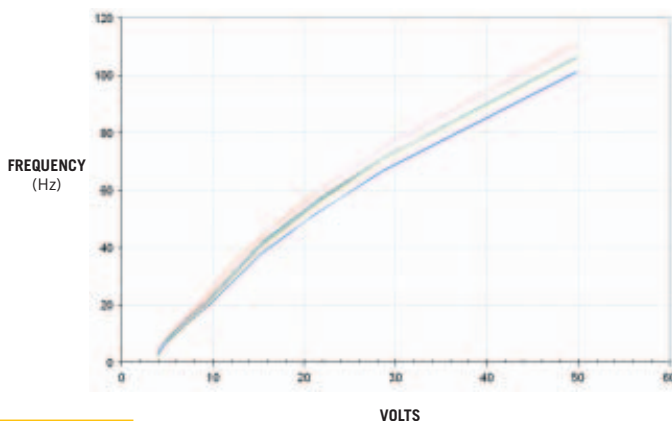


Figure 3

The frequency-versus-voltage response for the circuit of Figure 2 shows the spread across a sampling of five units for both polarities of line voltage.

Figure 3 shows a plot of the frequency-versus-voltage response of the circuit of Figure 2. It shows the

spread across a sampling of five units for both polarities of line voltage. Generally, the responses for the positive and negative voltages in a given unit are so close that the plot lines overlay each other. The unit-to-unit variations are larg-

er and in production are mostly attributable to variations in  $C_1$ . Although not highly precise, the circuit is more than adequate for distinguishing between on-hook (typically, greater than 18V) and off-hook (typically, less than 12V) con-

ditions. You can also use it to detect the small voltage changes that might be of interest in detecting barging in—when another device on the line goes off-hook while this device is using the line. □

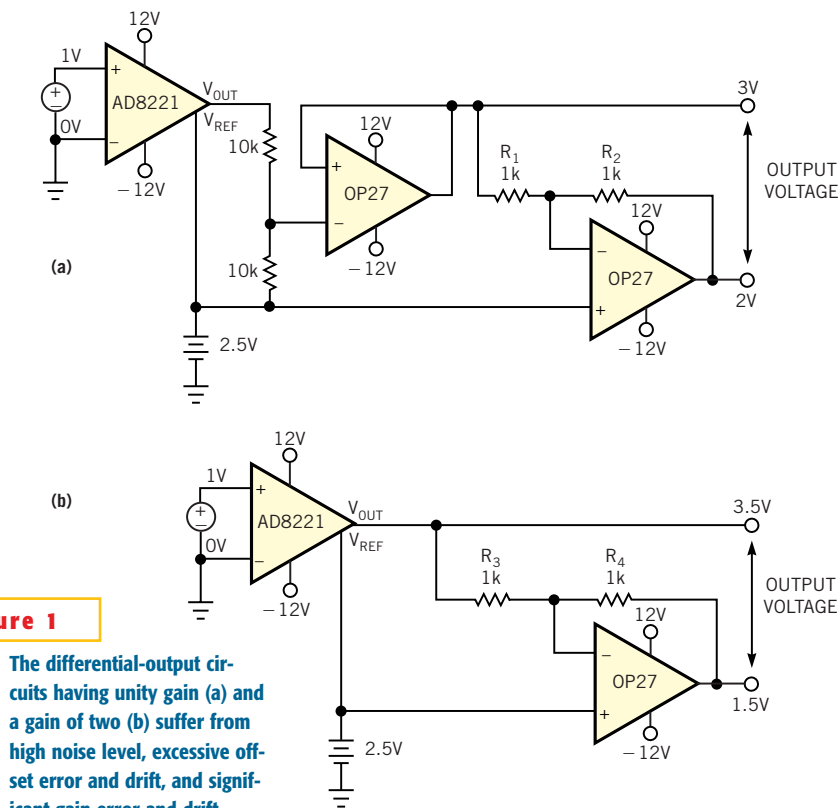
## Instrumentation amp has differential outputs

Moshe Gerstenhaber and Stephen Lee, Analog Devices, Wilmington, MA

**S**TATE-OF-THE-ART ADCs accept differential inputs, allowing you to differentially implement the entire signal path from sensor to converter. This structure provides significant performance advantages, because differential signals increase the dynamic range, reduce hum, and eliminate ground noise. **Figures 1a** and **1b** show two common differential-output instrumentation-amplifier circuits. The first provides unity gain, and the second implements a gain of two. Both circuits, however, suffer from increased noise, offset error, offset drift, gain error, and gain drift as compared with an instrumentation amplifier with a single-ended output. **Figure 2** shows a differential-output instrumentation amplifier that has none of these deficiencies. The design exploits the fact that the output of an instrumentation amplifier is the difference between the output pin,  $V_{OUT}$ , and the reference pin,  $V_{REF}$ . This application adds an inverter with a gain of  $-1$  between the two pins.

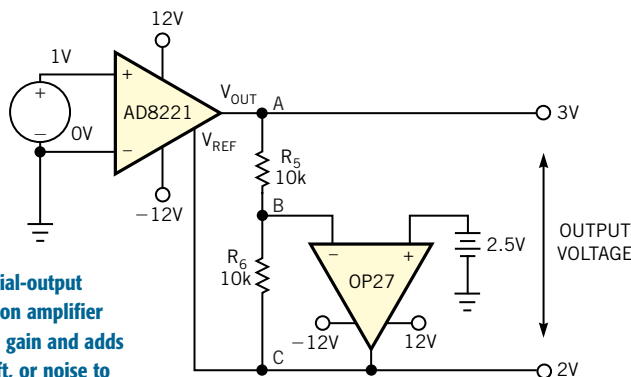
With an input voltage,  $V$ , the output voltage ( $V_{OUT} - V_{REF}$ ) must also be equal to  $V$ . The reference pin's voltage is opposite in polarity to the output pin's voltage. Therefore, the output must produce  $V_{OUT} = V_{IN}/2$  and  $V_{REF} = -V_{IN}/2$  to satisfy  $(V_{OUT} - V_{REF}) = V$ . Applying a 2.5V signal to the noninverting terminal of the op amp sets the common-mode output level. The op amp establishes 2.5V at Node B. Accordingly, if you apply 1V to the input, 3V appears at Node A,

and 2V appears at Node C. Thus, the output is 0.5V higher than and 0.5V lower than 2.5V. Errors from  $V_{OUT} - V_{REF}$  are a function only of the instrumentation amplifier. Errors such as offset, noise, and gain error that stem



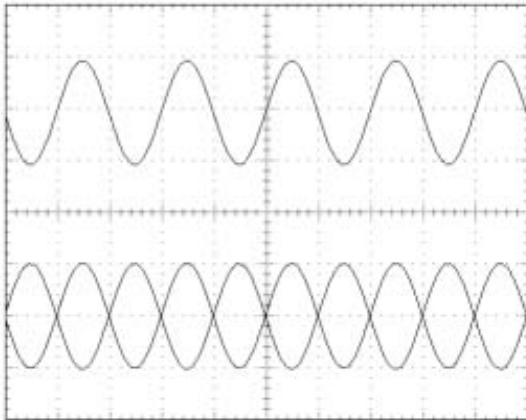
**Figure 1**

The differential-output circuits having unity gain (a) and a gain of two (b) suffer from high noise level, excessive offset error and drift, and significant gain error and drift.

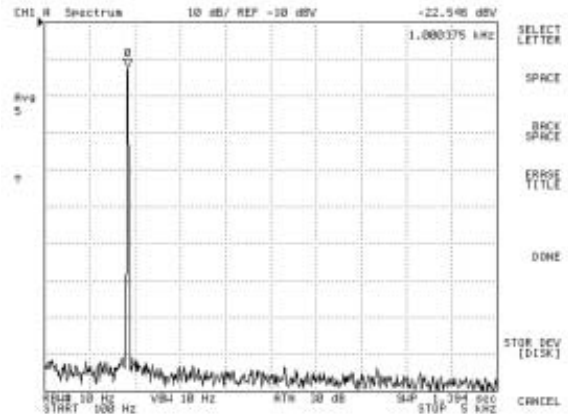


**Figure 2**

This differential-output instrumentation amplifier preserves the gain and adds no offset, drift, or noise to the output signal.



**Figure 3** A 2V p-p, 1-kHz input signal (top), and 1V p-p differential-output signals (bottom) have an output common-mode voltage of 2.5V.



**Figure 4** The spectral analysis of the differential-output signal shows that input to the instrumentation amplifier is 2V p-p, 1 kHz.

from the inverter amplifier and resistors equally affect both outputs. Thus, they contribute only to the common-mode output, which the ADC rejects. The top

waveform in a performance photo shows the 2V p-p, 1-kHz input (**Figure 3**). The two outputs appear at the bottom. The output common-mode voltage is 2.5V.

Another performance photo shows the spectral density of the differential output (**Figure 4**). □