designfeature *By Fabien Franc, California Micro Devices*

ENABLING A PC TO RESPOND TO IMPORTANT STIMULI, SUCH AS INCOMING FAXES, WHILE IT APPEARS TO BE OFF TO SAVE ENERGY, PRESENTS SOME INTRIGUING POWER-SYSTEM-DESIGN CHALLENGES.

Implementing power management for instantly available PC cards

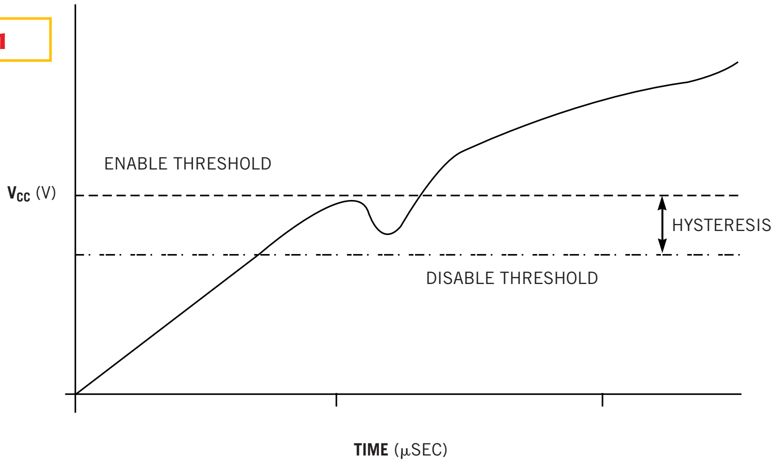
INSTANTLY AVAILABLE PCs (IAPCs) are creating new power-management requirements. You can provide the continuous 3.3V output necessary to support PCI cards in such PCs. After a quick introduction to PC and PCI-card power requirements, you can learn how to avoid supply-voltage discontinuities during critical power transitions. A detailed performance analysis explains the measured power-up and -down transient response of several hardware configurations. The analysis illustrates the effect on performance of variables such as voltage-regulator hysteresis, decoupling-capacitor values, power-supply line series resistance, and load current.

WHAT IS AN INSTANTLY AVAILABLE PC?

Today, PCs need to remain constantly connected to the outside world but, at the same time, consume minimal power. Even when a computer appears idle, it must still receive e-mail messages and incoming faxes or phone calls. The PC must automatically switch from sleep mode to on mode; in other words, it must be instantly available. The challenge is to maintain a system's modem or LAN connection while minimizing power consumption. These power-management features are called wake on ring (or wake on modem), wake on LAN (WOL), and wake on power-management event (PME).

The main qualities and benefits of such systems are that the PC is available any time to receive mes-

Figure 1

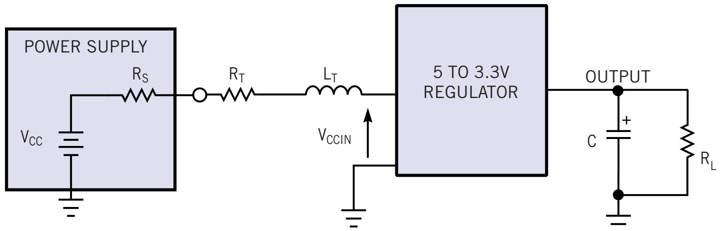


Voltages at regulator inputs don't always change monotonically, as this example shows. Hysteresis in comparator thresholds helps to prevent undesirable changes in comparator outputs.

sages; the PC responds any time, allowing you to perform operations such as maintenance; and the PC saves energy by being silent in the idle mode.

Microsoft's OnNow initiative defines requirements for many PC hardware and software components, including the Windows operating system, software applications, device drivers, and system hardware. All of these elements must work together to provide a fully transparent power-management system. This article focuses only on the hardware aspects.

Figure 2



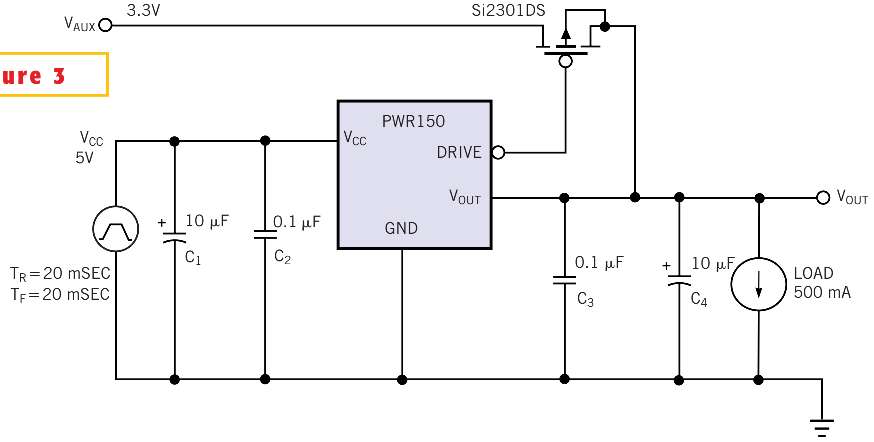
Because of internal series resistance, power supplies are not perfect voltage sources. Similarly, power-supply-distribution buses suffer voltage drops because of their series resistance and inductance. This circuit includes the parasitic elements.

ACPI SYSTEM DESIGN

An IAPC appears to be off, yet it can snap back within seconds to its full-ready state, for example, responding to a ringing phone in time to service a call. To meet these requirements, Intel, Microsoft, and Toshiba defined the Advanced Configuration and Power Interface (ACPI) Specification.

Instantly available motherboards include an ACPI BIOS, an ACPI chip set, and PCI slots that comply with the PCI Bus Power Management Interface Specification Version 1.1. An Intel chip set supports the power-management features that define the ACPI sleep states and also generates the signals that control power planes and turn the main power supplies on and off.

Figure 3

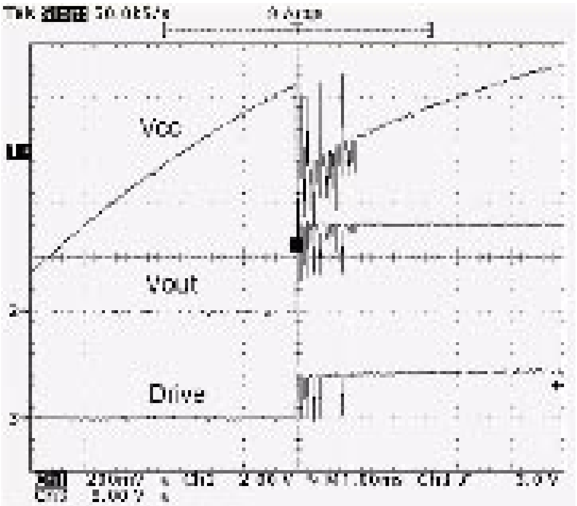


This test circuit, which is used to characterize voltage-regulator ICs includes both low- and high-frequency bypass capacitors at the input and output of the device under test.

The implementation includes multiple power sources and uses separate power planes in the system. The state that the system demands determines which power source is active. One of the major requirements is to automatically and repeatedly switch between power sources without interruption.

The sleep state of an IAPC is called "suspend to RAM." To implement this state, the system uses split power planes and an auxiliary power source (V_{AUX}) for dual-mode power distribution. By definition, all PCI add-in cards connect to the motherboard through the PCI bus. The PCI connector reserves several pins to support instant availability.

On newer PCs, three independent voltage sources are now available on the PCI bus: $3.3V_{AUX}$, $3.3V_{CC}$, and $5V_{CC}$. In a power-plane partitioning system of an IAPC, $3.3V_{AUX}$ is always electrically isolated from the main PCI 3.3V rail. During normal operation, the $3.3V_{AUX}$ supply remains on, whereas the system can switch the other main supplies, $3.3V_{CC}$ and $5V_{CC}$, on and off as needed.



NOTES: CHANNEL 1: V_{CC}, OFFSET 4.1V. CHANNEL 2: V_{OUT}. CHANNEL 3: DRIVE.

Figure 4

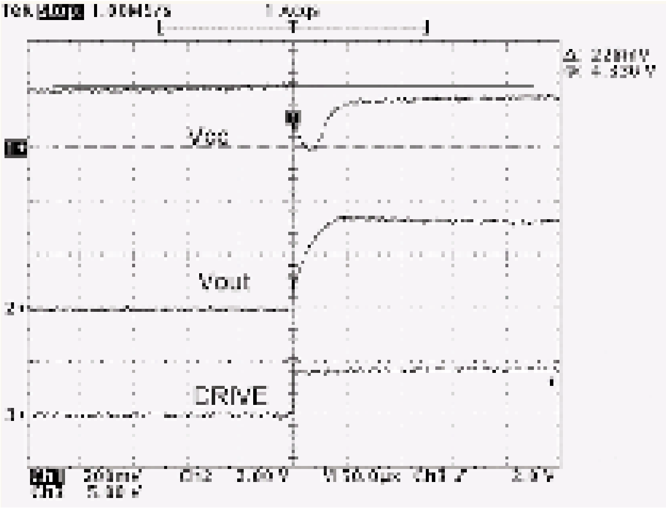
This cold-start V_{CC} power-up measurement uses an improper test setup. A 0.5Ω resistor supplies most of V_{CC}'s total series resistance, which is 0.7Ω. This figure indicates the output response as V_{CC} approaches the select threshold and the oscillatory behavior under full load. At a load current of 300 mA, the oscillation disappears.

PCI CARDS

PCI network-interface cards (NICs) and modem cards use split power planes. To operate in sleep mode and wake up the system, these cards require only the V_{AUX} power supply. Some

NICs that operate in wake-on-LAN mode get 5V standby power through a cable that connects directly to a header on the motherboard.

Today, PCI-card chip sets and ASICs operate at 3.3V, so their power consumption is much lower than that of older 5V modem chips. However, older PCs still supply 5V and do not have a $3.3V_{AUX}$ supply. To ensure compatibility with both old and new PCs, newer PCI cards operating in PCs that lack a 3.3V supply derive their own 3.3V regulated power from the system's 5V supply. The PCI Power Management Specification limits the output current of such 3.3V regulators to 375 mA.



NOTES: CHANNEL 1: V_{CC}, OFFSET 4.1V. CHANNEL 2: V_{OUT}. CHANNEL 3: DRIVE.

Figure 5 A cold-start power-up measurement indicates the output response as V_{CC} approaches the select threshold. The uncharged output capacitor causes maximum inrush current to flow, resulting in a large voltage disturbance of about 230 mV at the V_{CC} pin. The built-in hysteresis of 250 mV ensures that the regulator remains enabled throughout the transient.

HYSTERESIS

Hysteresis voltage, $V_{HYSTERESIS}$, is the difference between the enabling threshold (at which the regulator turns on) and the disabling threshold (at which the regulator turns off) (**Figure 1**). $V_{HYSTERESIS}$ establishes the maximum level of acceptable noise or disturbance on V_{CC} or V_{AUX}. Noise susceptibility is critical during power transitions.

As shown in **Figure 2**, the voltage that the device sees is given by:

$$V_{CCIN}=V_{CC}-(R_SI)-(R_TI)-(L_TdI/dt)\,, \qquad (1)$$

where V_{CC} is the power-supply voltage, R_S is the power-supply output impedance, R_T is the interconnect series resistance (between supply and regulator), L_T is the trace (line) inductance (between supply and regulator), and I is the current.

Assuming an ideal situation in which there is minimal parasitic inductance, the hysteresis level should follow:

$$V_{HYSTERESIS}>(R_S+R_T)\ I. \qquad (2)$$

The worst-case condition, with respect to the inrush current, occurs at turn-on, when the initial output-capacitor voltage is zero. During turn-on, the current rises from zero to a high value. The inrush current is highest when the initial output-capacitor voltage is zero. Higher capacitor values also increase inrush current. You can assume an inrush current equal to twice the device's maximum dc load current. An inrush current of 1A and a hysteresis of 250 mV give a maximum recommended series resistance of 0.25Ω (**Equation 2**).

POWER REGULATORS

Today, several companies offer low-dropout regulators that provide a fixed 3.3V output with a current load exceeding 375 mA. These products also feature an intelligent controller that allows either a 5V supply or an auxiliary 3.3V supply to supply power to the 3.3V load via an external switch. California Micro Devices, Cherry Semiconductor, and Semtech all offer regulators that satisfy the demanding requirements for uninterrupted and reliable power (**Table 1**).

The CMPWR150 from California Micro Devices can supply as much as 500 mA of continuous output current when it operates from a 5V V_{CC}. **Figure 3** shows the test setup used during transient characterization of this IC. The setup uses an external P-channel MOSFET to switch the 3.3V V_{AUX} at full-load current. **Figure 4** shows how improper implementation of the test circuit can produce oscillation at the regulator output.

The circuit compares the V_{CC} input to a 4.1V internal-threshold level. Whenever V_{CC} drops below that level, the regulator is disabled and the DRIVE output is enabled (active low). The DRIVE output controls an external P-channel MOSFET switch, which connects an auxiliary 3.3V source to the load. When the regulator is enabled, the DRIVE output is set to V_{CC}.

The setup includes the V_{CC} supply's effective source impedance, R_S, which is approximately 0.2Ω. As measurement data later demonstrate, this impedance should be no greater than 0.25Ω to ensure that precise switching is maintained during V_{CC} selection and deselection.

During V_{CC} power-up/down sequencing, the test setup controls both the rise and fall times to maintain a 20-msec duration. This switching time represents the

TABLE 1—REPRESENTATIVE SUPPLIERS OF POWER-MANAGEMENT REGULATORS

Company	Product	Output voltage/current
California Micro Devices Corp 1-408-263-3214 www.calmicro.com **Circle No. 301**	CMPWR150	3.3V/500 mA
Cherry Semiconductor Corp 1-401-885-3600 www.cherry-semi.com **Circle No. 302**	CS5231	3.3V/500 mA
Semtech Corp 1-805-498-2111 www.semtech.com **Circle No. 303**	SC1534	3.3V/400 mA

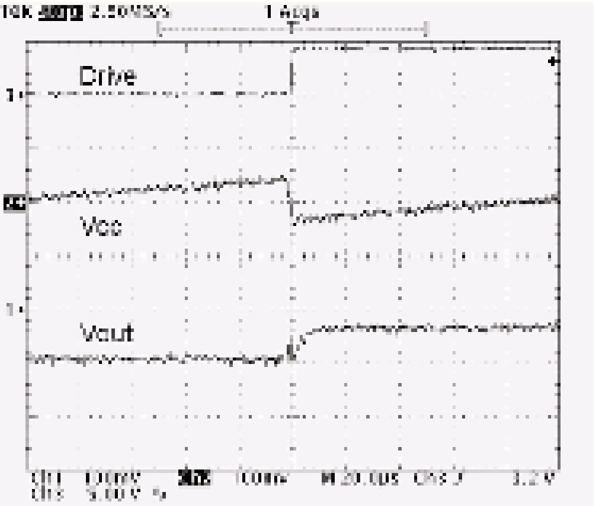
NOTE: These regulators meet the PCI-defined maximum 375-mA load requirement.

worst case in most applications. During characterization, the maximum load current is 500 mA unless otherwise specified.

When you perform the transient analysis for the V_{CC} power-up and power-down sequences, V_{AUX} normally equals 3.3V—its nominal value. A cold-start power-up occurs when V_{CC} rises from 0 to 5V with V_{AUX} connected to ground (**Figure 5**). As soon as the 5V source reaches the *regulator_enable* threshold (4.25V typical), the regulator turns on. At that time, the voltage across the output capacitor begins to rapidly charge, pulling a large transient current, which can easily exceed 1A. It is, therefore, important to consider the parasitic series resistance and parasitic inductance between the supply voltage, V_{CC}, and the device. **Equation 1** gives the voltage that the device sees. Clearly, a large, rapidly changing current creates a large change in V_{CCIN}. If the input level drops below the *regulator_disable* threshold (4.1V typical), the regulator turns off. The input level then starts to rise back toward 5V, turning the regulator back on. This situation results in an unstable state ("motorboating"). The regulator turns on and off until it has finally charged the output capacitor to 3.3V.

CAPACITORS

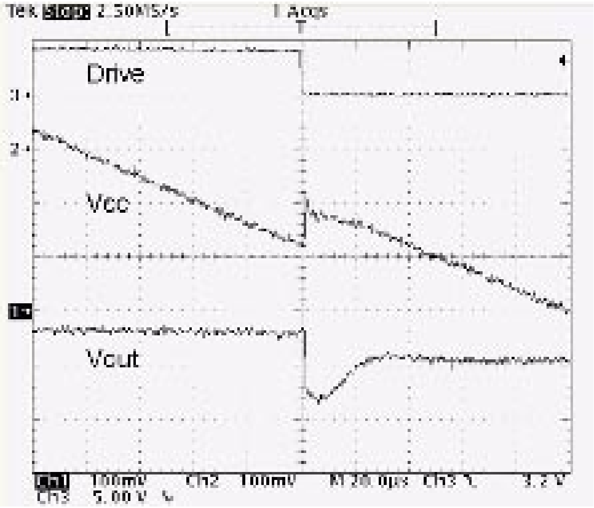
Minimizing this effect requires an input capacitor in close proximity to the V_{CC} input pin. When a transition occurs from V_{AUX} to V_{CC}, the capacitor serves as a charge reservoir to provide some of the load current (**Figure 6**). This function is especially critical when the output capacitor is not yet charged at power-up or when the output level is much lower than 3.3V. The regulator goes into current limiting until V_{OUT} returns to its nominal level. The input capacitor should be a tantalum device of 1 µF or more.



NOTES: CHANNEL 1: V_{OUT}, OFFSET 3.3V. CHANNEL 2: V_{CC}, OFFSET 4.3V. CHANNEL 3: DRIVE.

Figure 6

A V_{CC} power-up measurement with V_{AUX} = 3.3V shows the output response as V_{CC} approaches the selected threshold. The output capacitor is already fully charged. When V_{CC} reaches the selected threshold, the inrush current is minimal and the V_{CC} disturbance is only 130 mV. The built-in hysteresis of 250 mV ensures that the regulator remains enabled throughout the transient.



NOTES: CHANNEL 1: V_{OUT}, OFFSET 3.3V. CHANNEL 2: V_{CC}, OFFSET 4.3V. CHANNEL 3: DRIVE.

Figure 7

A V_{CC} power-down measurement indicates the output response as V_{CC} approaches the deselect threshold during a power-down transition. V_{AUX} equals 3.3V. When V_{CC} reaches the deselect threshold (4.1V), the regulator turns off, causing a step reduction in V_{CC} current and resulting in a small voltage increase at the V_{CC} input. This disturbance is approximately 100 mV, and the built-in hysteresis of 250 mV ensures that the regulator remains disabled throughout the transient. The output voltage experiences a disturbance of approximately 100 mV during the transition.

During power transitions, a previously charged output capacitor provides the load current until the regulator or the auxiliary supply takes over (**Figure 7**). A tantalum capacitor of 10 µF or more at the output improves this transition.

Additionally, you should place ceramic chip capacitors of 0.1 µF next to both the input and the output pins to reduce high-frequency noise.

CONCLUSION

IAPCs require specialized power-management devices to provide regulated voltage sources and smart switches among power sources. High-performance integrated devices are ideal because they reduce component counts and simplify design and manufacturing start-up. These products allow interface-card manufacturers to meet IAPC power requirements.□

REFERENCES

1. "Instantly Available Power Managed Desktop PC," Design Guide, Rev. 1.2, Sept 25, 1998, Intel Corp.
2. "Instantly Available PC System Power Delivery Requirements and Recommendations," Revision 1.0, Dec 30, 1997, Intel Corp.
3. "PCI Bus Power Management Interface Specification," Revision 1.1, Dec 18, 1998, PCI Special Interest Group.

AUTHOR'S BIOGRAPHY

Fabien Franc is a senior application engineer at California Micro Devices. He has an MSEE from École Polytechnique Federale (Lausanne, Switzerland), and he is a member of the development team for power-management products at California Micro Devices.