



MANO A MANO WITH MANUFACTURING

**HIGH SPEED, LOW POWER,
AND DIMINISHING FEATURE
SIZES MAKE IT IMPOSSIBLE
FOR DESIGNERS TO MAIN-
TAIN A WALL BETWEEN
DEVELOPMENT AND
MANUFACTURING.**

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MANY ELECTRONIC-PRODUCT DESIGNERS, whether they are developing ICs or pc boards, must now consider manufacturing issues much earlier in the design cycle than they did a few years ago. Most of these engineers are facing this problem for the first time

and lack in-house knowledge of the available approaches or even the most severe pitfalls. Design engineers have worried about postdevelopment issues since the beginning of our industry, but their focus was testability, not manufacturability. When, as early as the 1970s, managers warned designers not to throw designs over the wall to manufacturing, they focused on the manufacturer's ability to test the finished product. Manufacturing technologies kept pace with engineering, and designers focused on meeting the functional requirements of the product, not the fabrication method. Although design for test is still an important goal, DFM (design for manufacturing) has become even more important—because if you can't build it, you don't need to test it. Personal computing and the introduction of portable devices are the main forces behind a radical change in engineering methodology. Products must offer more functions but decreased power consumption and product size. Also, to provide reasonable performance, operating frequencies must increase. Miniaturization, whether in ICs or pc boards, is generating new classes of problems that electronics engineers are still learning to address and solve.



Successful product development requires a bidirectional exchange of information and knowledge between development and manufacturing. In most instances, the fact that these two groups belong to different companies complicates the communication. In addition, a third industry sector is developing the tools that improve the quality of communication and help designers and manufacturers to avoid or, at worst, solve the problems: EDA vendors, which traditionally focused mainly on design issues. For ICs, the problem is even more complicated when the product contains circuitry designed by more than one company or both hardware and software blocks. New design methods will develop as a result of the cooperation among manufacturers, EDA vendors, and designers. For example, TSMC has announced its Reference Flow 5.0 to help designers using its 130- or 90-nm processes. The semiconductor foundry established working relationships with Cadence, Mentor, and Synopsys for this effort, and, to improve designers' support, they also included smaller EDA companies with experience in point tools, such as Apache Design Automation, Atrenta, Optimal Corp, and Logic Vision. But the coalition represents only two legs of a three-legged stool. Designers now need to do their part and provide

AT A GLANCE

- ▶ Designers are struggling to keep pace with manufacturing capabilities.
- ▶ PC boards must provide more functions in less space.
- ▶ IC processes using subwavelength techniques complicate the tasks of designers.
- ▶ Economics may replace technology as the motivator for process introduction.

feedback so that the companies can improve the proposed methodology and better adapt it to the needs and approaches of product designers.

PLM (product-life-cycle management) is effective at providing a synchronization and communication system in mechanical design. Yet, electronic designers have not embraced such techniques. The main reason for such a lack of interest has been the fact that most electronic design deals with only one part, in the case of ICs, or has an established method to list the components, in the form of a bill of materials for pc boards. But, more and more, designers and manufacturers must communicate even when dealing with electronics products (see sidebar "EDA companies: Sell

PLM products or just coexist with them?"). At the 2004 DAC (Design Automation Conference) in June, MatrixOne, a leader in mechanical PLM, announced the purchase of Synchronicity, a company that develops and sells electronic-design-management products. In 2005, MatrixOne will introduce its own electronic PLM tool.

PC-BOARD DESIGN

The challenges that pc-board designers face are not new; they have been present for more than 20 years in hybrid circuits. But a small and specialized group of engineers skilled in analog design addressed those designs. What has changed is the use of those technologies on high-volume, low-cost pc boards with predominantly digital blocks. Particularly relevant issues are embedded passives, microvias, bare die, and new manufacturing materials. Embedded passives technology enables companies to build products that would otherwise be too large, heavy, or expensive. Designers use them to reduce the number of pc-board layers, to place termination devices directly at the chip pins, and to cluster all necessary passives by a device next to it. Microvias help provide interconnects required in ultra-high-speed design. You can use them with packages that have reduced pin pitches, and they offer signif-

EDA COMPANIES: SELL PLM PRODUCTS OR JUST COEXIST WITH THEM?

By Kent McLeroth, Zuken USA

Virtually every major PLM (product-life-cycle-management) company has its roots in mechanical design. Today, these PLM companies provide tools to all manner of engineering and manufacturing companies, though their expertise remains firmly in the mechanical world. Such tools are well-suited for companies that design and manufacture primarily mechanical products. From heavy equipment to automotive to modular office furniture, mechanically oriented PLM tools make sense. Many of the sectors that have used PLM for years are seeing more electronics components in their products. How can companies whose products are

primarily electronic take advantage of PLM tools?

The design process, manufacturing process, life cycle, and cost breakdown of an electronic product differ greatly from those of a mechanical product. Electronic-product-life cycles tend to be shorter and more dynamic. Yet many electronic product companies have tried to use mechanically based PLM systems to manage their electronic-product life cycles because they lacked an alternative. EDA companies have lagged behind in developing PLM for electronic products. Instead, they forged agreements with mechanically oriented PLM companies, pro-

ducing a host of interfaces that did nothing more than move incomplete electronic-product data into systems not designed to manage it.

In the mid-1990s, an EDA company began to offer a product to handle electronic products. This e-PLM product places a heavier emphasis on the unique requirements of the electronic-component life cycle; the dynamic relationship between component, assembly, and product; and a direct, bidirectional pipeline between engineering and manufacturing. Typical areas of improvement an e-PLM system generates include component-overhead cost

reductions and a dramatic reduction in design-to-production cycle times. The design phase frequently determines 70 to 80% of the final product cost. The best approach is to give designers the freedom they need to select the optimum components and materials and ensure, through a common database, that these elements are compatible with both purchasing and manufacturing requirements.

AUTHOR'S BIOGRAPHY

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icantly less reactance, thus increasing circuit performance. To achieve reduced form factors, designers eliminate the device package and use a bare die. This practice results in a variety of device types, including wire-bonded chip on board, flip-chip, chip-scale packaging, and stacked die.

The increased use of advanced technologies creates the need to find new, cost-efficient technologies. An example is the search for embedded materials that can provide better capacitance density. Materials that simplify the manufacturing process, facilitate better component tolerances, or have lower dielectric constant and loss present designers with both new techniques and new challenges. The new required technologies increase both the time and the cost of pc-board manufacturing, which in turn requires engineers to incorporate the new aspects in the design flow from the beginning. EDA tools play a role in bridging the expertise gap. EDA vendors are working with designers, materials suppliers, and standards-making bodies to develop new tools and methods addressing these design challenges. The most important manufacturing challenges facing pc-board designers include:

- modeling embedded passives, via structures, and layer structures;
- building libraries with parametric data for new materials;
- creating embedded passive devices using user-defined parameters;
- placing embedded passive devices; and
- routing microvias structures and patterns.

New manufacturing technologies directly impact the place-and-route tools, which EDA companies have significantly improved. EDA vendors have also offered improved analysis tools for signal integrity, power consumption, and EMI (electromagnetic interference).

IC DESIGN

“Beyond initial design considerations,” according to Mark Miller, vice president of marketing and business development for design for manufacturing

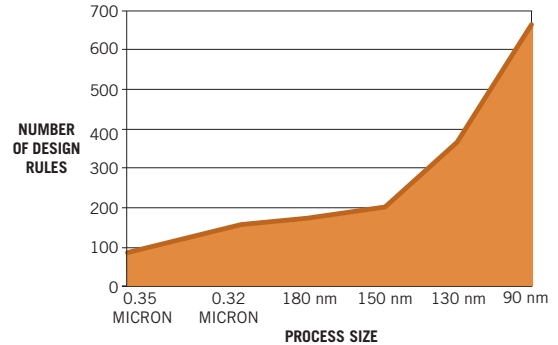


Figure 1

The number of design rules increases with every new process introduction.

at Cadence Design, “design engineers will need to address manufacturing-yield issues throughout the design chain, into production ramp-up, and then after volume manufacturing for yield improvements.”

Semiconductor manufacturers inform designers of the electrical and physical characteristics of a process by providing a set of design rules. A design team that respects all of the design rules significantly increases the probability that the chip will have no physical defects and that yields will be average or above. As **Figure 1** shows, the number of design rules to follow has increased to such an extent, beginning with the 150-nm process, that engineers have a difficult time understanding and coherently applying them throughout the design flow. Lithography issues, turnaround time and cost of mask sets, and yield problems are primarily responsible for the significant increase in the number of design rules.

IC features are now smaller than the wavelength of light that optical-lithography equipment uses. All third-party manufacturers use steppers that support 193-nm wavelengths. You can understand the correlation between the wavelength of light used in manufacturing and the increase of the number of design rules beginning at 150 nm. The greater the gap between the wavelength of light and the feature size, the more difficult the problem becomes, the number of design rules has increased from approximately 200 at 150 nm to more than 700 for 90-nm processes. To produce smaller geometries than the wavelength of light the process uses, semiconductor companies employ RET (resolution-enhancement techniques)—most often, OPC (optical proximity correction), PSM

(phase-shift masks), SRAF (subresolution-assist features), and OAI (off-axis illumination). All of these techniques require designers to perform additional layout modifications after they run the DRC (design-rule-check) program. In addition to the new design rules established by the manufacturers, many design teams now include engineers familiar with lithography and process issues. All such modifications are error-prone because, in general, there is no

way to verify the result. Synopsys has developed a tool that addresses this shortcoming. SiVL compares a target design with its simulated silicon image to verify a design's manufacturability.

To create a set of masks, chip designers today send the mask manufacturer a file containing the layout data. The volume of data is as large as 50 Gbytes for a single design, which has caused significant increases in turnaround time for mask manufacturing. The increase is especially significant when the prototype devices show the design contains an error, because the time it takes to produce a new set of masks directly impacts the product's profitability. You cannot solve a problem of this magnitude simply by purchasing faster computers, but you can make it more manageable by using grid computing. EDA tools can segment the data and use a number of computers in parallel to improve throughput. As manufacturing techniques move to deep-sub-wavelength technologies, many new issues associated with the aggressive use of RET come to the forefront. Applying

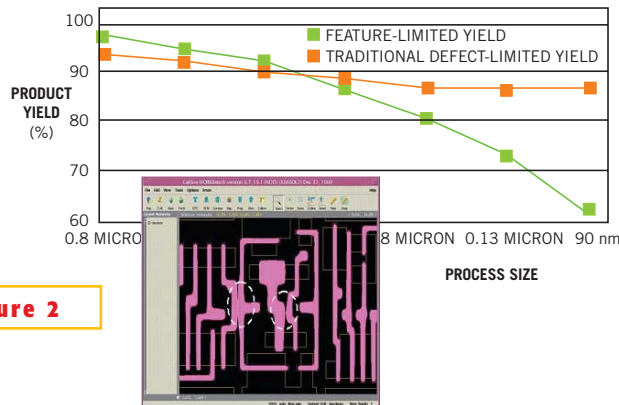


Figure 2

Defects increase with every new process node and drive yield down.

SRAF and OPC to a 90-nm pattern greatly complicates the mask set and, therefore, increases its cost. Mask-write and mask-inspection times are the two major factors in determining the cost. One way to lower the cost is by applying design-intent information to the mask-synthesis flow. Engineers can use design intent to create a tolerance margin in OPC applications, thereby applying only the minimum amount of OPC necessary to meet the lithography goals.

Yield issues change with each new process node, as does the time required to bring a new process to acceptable yield levels. Engineers generally encounter three types of yield problems: Random yields are generally associated with particle defects, the process or the lithography application is generally responsible for systemic problems, and device physics and interconnect effects produce parametric failures generally observed as timing violations. **Figure 2** shows the decrease in yield brought about by failure to properly generate features due to shrinking geometries.

Improvements in manufacturing equipment have enabled not only smaller features, but also larger wafers. Most commercial wafers today have a diameter of 300 mm, or almost 1 ft. The greater the dimension, the greater the probability that an impurity will deposit on the surface, despite manufacturers' precautions. Random defects and nonparametric issues are the dominant effects of yield loss. Impurities can cause catastrophic failures, such as shorts between two

metal lines or opens in a metal line. Layout designers traditionally design using the minimum specifications to improve speed or minimize power consumption. Designing to minimum width and spacing tolerances, however, may actually increase a design's susceptibility to random effects.

Systematic yield issues are not random; they relate to the design process technology, including the chemical impact of the process materials, the mechanical impact of the manufacturing process, the postlayout application of lithographic processes, and more. Unlike random-defect issues, the likelihood of failure from systematic defects is proportional to the number of instances of a given type of feature. Examples of systematic defects include planarity, which is the difference in oxide heights for a given region of the design; antenna effects caused by charge accumulation on interconnect; via opens; and electromigration. Design rules help engineers to at least be aware of the dangers, but the large volume of rules makes it difficult to

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For more information on products such as those discussed in this article, contact any of the following manufacturers directly, and please let them know you read about their products in *EDN*.

Altera
www.altera.com

Apache Design Automation
www.apache-da.com

Atrenta
www.atrenta.com

Cadence Design Systems
www.cadence.com

Logic Vision
www.logicvision.com

Mentor Graphics
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Optimal Corp
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Synplicity
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Synopsys
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www.zuken.com

OTHER SOURCES OF INFORMATION OR EDA TOOLS

Accellera
www.accelera.org

IBM
www.ibm.com

Magma Design Automation
www.magma-da.com

MatrixOne
www.matrixone.com

ReShape
www.reshape.com

Praesagus
www.praesagus.com

Sigma-C
www.sigma-c.com

VSI Alliance
www.vsia.org



be correct the first time. RET techniques help to avoid systematic-yield issues. Mentor Graphics' Calibre product is the market leader in helping engineers deal with RET/OPC methods.

Parametric-yield losses seriously impact nanometer designs. In such situations, all of the logic elements of a design or chip function as expected, but the timing or electrical requirements, such as power consumption, fail to meet specifications. Parametric defects are the results of interconnect parasitics and device physics. Engineers know that avoiding a problem is better than fixing one. EDA company Chip Vision offers Orinoco, a tool that helps designers plan power consumption and distribution during the initial design phases. The Accellera consortium has worked since its inception to develop standards to help semiconductor manufacturers, EDA vendors, and designers improve the quality of communication in

DFM. Some of its standards are now IEEE standards, such as IEE 1481 (Circuit Delay and Power Calculation), IEEE 1497 (Standard Delay Format), and IEEE 1603 (Advanced Library Format).

Juan-Antonio Carballo, research staff member with the IBM research Laboratory in Austin, TX, and chairman of the VSI Alliance R&D Pillar, says that manufacturers are investigating ways to improve manufacturing processes and account for design factors. They are looking into new materials, such as copper, that ease design convergence by reducing wire resistance and SOI (silicon-on-insulator)

techniques that promise lower capacitance and leakage characteristics. New devices, such as multithreshold, multioxide-thickness devices provide increased design flexibility to balance power and performance.

Although the more regular layout of FPGA devices has minimized many of the yield

problems in ASIC and standard ICs, designers are also beginning to see some parasitic-yield problems with FPGAs. Structured ASICs, which also offer a more regular geometry, have surprised many of their early supporters, because they also suffer from parametric-yield problems. To deal with these issues, EDA companies are beginning to collaborate with FPGA vendors early in the development of devices that use a new process. Synplicity has been a pioneer in this effort, and Altera always develops its proprietary synthesis tool and the new devices in parallel. Unless the industry can quickly find a way to manage yield problems and minimize their impact on profitability, the pace of new manufacturing-process introduction will slow. Economics, not technology, will then become the major factor in semiconductor-technology progress. □

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