



**Figure 1**

To generate VMSK/2 coding, you first generate a duty-cycle-modulated signal (D) that begins each period in the high state. The portion of the time the signal spends in that state is determined by the data (1 or 0) and is either slightly greater than or slightly less than 50%. You then invert the signal in all of the even-numbered intervals (E). Finally, you delay the signal (F) so that its edges either slightly precede or slightly follow the edges of the times-one clock (B). In this example, signal D has a duty cycle of either  $\frac{1}{8}$  or  $\frac{7}{8}$  of the times-one clock period,  $T_B$ . Signals E and F thus spend  $(n+x)T_B$  in the high or low state (where  $n$  is any integer  $\geq 0$  and  $x = \frac{1}{8}, \frac{5}{8}, \text{ or } \frac{7}{8}$ ).