

**MUCH OF YOUR SYSTEM'S PERFORMANCE  
DEPENDS ON JITTER SPECIFICATIONS, SO  
CAREFUL ASSESSMENT IS CRITICAL.**

# Understand the effects of clock jitter and phase noise on sampled systems

**A**S HIGHER RESOLUTION data converters that can perform direct IF sampling come to market, system designers need help making performance-versus-cost trade-off decisions on low-jitter clock circuits. Many of the traditional methods manufacturers use to specify clock jitter do not apply to data converters or, at best, reveal only a fraction of the story. Without a proper understanding of how to specify and design the clocking circuit, you may not achieve optimal performance of these data converters.

A simple jitter specification is rarely sufficient for making an informed clock selection. Instead, it is important that you know the bandwidth and spectral shape of the clock noise so that you can properly account for them during sampling. Many system designers do not adequately specify the phase-noise and jitter requirements for the data-converter clock, and picoseconds of clock jitter quickly translate to decibels lost in the signal path.

At the opposite extreme, some designers may be paying too much for an expensive clock source, simply because they are unclear about how clock noise affects the converter and ultimately their product's performance. Note that the most expensive clock generator does not always yield the best system performance. Many trade-offs relate to jitter, phase-noise, and converter performance. Once you understand these trade-offs, you can select the best clock for the application at the lowest cost.

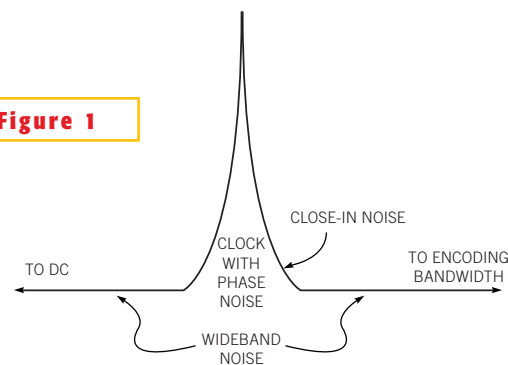
For IF- and RF-sampling systems, the encoding source functions more like a local oscillator than a clock. Many designers expect manufacturers to specify clock requirements in the frequency domain, just as they do RF synthesizers. It is difficult to provide a direct correlation between clock jitter and phase noise, but some guidelines exist for designing or selecting encoding sources from either a clock-jitter or a phase-noise perspective.

The primary purpose of a data converter is either to produce an analog waveform from regular time samples or to produce a series of regular time sam-

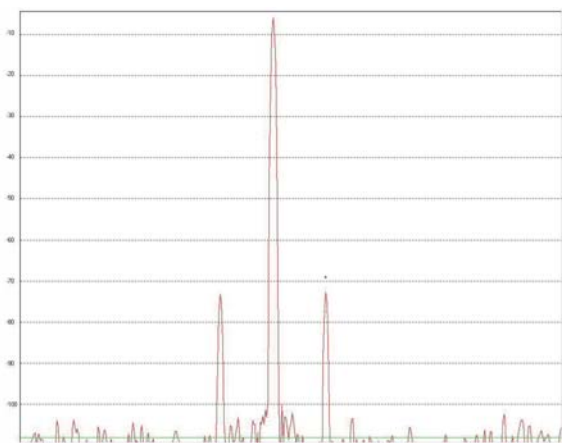
ples from an analog signal. Therefore, stability of the sampling clock is important. From a data-converter perspective, this instability, or random clock jitter, results in uncertainty about when the analog converter samples the input. Random jitter is characteristically gaussian; the rms time value or standard deviation of the occurrences specifies this random jitter. Although there are several methods to directly measure clock jitter, the clock-stability requirements tighten when you need to measure sub-picosecond-timing variations, so you need to use indirect measurements.

From a converter perspective, the encoding bandwidth can extend over many hundreds of megahertz. When considering the bandwidth of the noise that constitutes jitter for a data converter, the range is from dc to the encoding bandwidth, which exceeds far beyond the typical 12 kHz to 20 MHz that vendors often quote for standard clock-jitter measurements. Because the concern with jitter is increased wideband-converter noise, it is easy to estimate clock jitter by observing the degradation in noise performance of a converter. **Equation 1** defines the SNR limitation due to jitter:

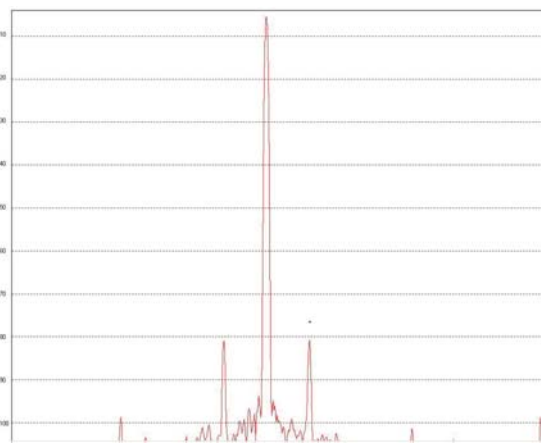
$$\text{SNR} = -20 \log (2\pi f_{\text{ANALOG}} t_{\text{JITTER,RMS}}) \text{dB.} \quad (1)$$



**Clock jitter in the frequency domain has a relatively sharp close-in component (skirt) plus a wideband component at much lower amplitude.**



**Figure 2** Spectrum of phase-modulated encoding source shows that, for relatively low-level angles of modulation, only the first elements of the sidebands are visible above the noise floor.



**Figure 3** A phase-modulated encoding source from Figure 2 samples a 30.62-MHz pure sine source, resulting in a side-spur level of  $-74$  dBc.

where  $f$  is the analog input frequency and  $t$  is the jitter. Solving this equation for  $t$  puts it in the form of Equation 2, which defines the clock-jitter requirement, given a frequency of operation and an SNR requirement:

$$t_{\text{JITTER}} = \frac{10^{-\frac{\text{SNR}}{20}}}{2\pi f_{\text{ANALOG}}} \quad (2)$$

If jitter were the only limitation to converter performance, sampling an IF signal of 70 MHz and maintaining an SNR of 75 dB would require a clock jitter of just 400 fsec.

You can easily use data converters, especially ADCs, to compute an SNR using FFT techniques by examining the degradation in SNR as the analog input frequency increases. By subtracting the noise contribution of the ADC from the total noise, you can estimate the noise due to the clock jitter. Once you know the noise figure, you can calculate the time jitter (Reference 1).

This method has two drawbacks. First, if you use windowing during the FFT processing, the impulse response of the window blurs the spectral resolution. Second, spectral resolution is limited for most reasonable FFT sizes. For example, using an encoding rate of 61.44M samples/sec and a 64k-sample FFT, each FFT bin represents a bandwidth of about 938 Hz. Spectral blurring causes the loss of clock noise within several FFT bins, which results in the loss of information for several kilohertz on either side of the fundamental, at which much of the phase noise exists.

Even in the case in which you implement synchronous FFTs without windows, the limitation of at least one FFT bin still exists, representing about 1-kHz bandwidth. From a close-in phase-noise point of view, the first few kilohertz around the clock source contain much of the frequency. Therefore, using the FFT method for estimating jitter causes you to lose much of the clock-noise information. However, because the goal is usually wideband SNR, this test is generally acceptable in measuring the wideband performance of the ADC.

#### THERE'S NOISE, AND THERE'S MORE NOISE

Equation 3 represents a sampling signal with a modified sinusoidal function with amplitude-, frequency-, and phase-modulation terms:

$$f_{\text{SAMPLE}} = A_T \sin((\omega_c t) + \phi_t) \quad (3)$$

Because the sample source is often hard-limited using differential-comparison techniques, the effects of amplitude modulation are minimal, as long as sufficient drive from the encoding source exists to drive the sampling switches so that amplitude-to-phase-modulation distur-

tion is not a problem. The effects of phase and frequency noise yield similar degradations in the sampling process, except that phase modulation is identical to frequency modulation with the derivative of the modulating signal (Reference 4). Note that, in the case of gaussian noise, the derivative is also gaussian-distributed, resulting in nearly identical results.

The traditional manner of observing clock jitter is by looking at its spectrum, in which much of the noise clusters near the clock signal (Figure 1). However, because of jitter, the ideal impulse in the frequency domain spreads out in the skirting, and much of the energy remains close to the desired frequency. However, the wider bandwidth contains much of the frequency. Because phase noise can often extend to high frequencies and because the ADC-encoding pin typically has a much wider bandwidth than the converter's sampling rate, this noise impacts the converter performance.

Sampling is a multiplication process in the time domain and, therefore, a convolution process in the frequency domain. Whereas it is clear that a mixer multiplies two analog signals in the time

**TABLE 1—ALLOWABLE ADJACENT-CHANNEL PHASE-NOISE REQUIREMENTS FOR GSM SYSTEMS**

GSM per 05.05 in wideband application	Offset	Performance*
Adjacent 1: 9 dBc	100 kHz to 300 kHz	~ -101 dBc/Hz
Adjacent 2: 41 dBc	300 kHz to 500 kHz	~ -133 dBc/Hz
600-kHz blocker: -26 dBm	500 kHz to 700 kHz	~ -151 dBc/Hz
800-kHz blocker: -16 dBm	700 kHz to 2.9 MHz	~ -161 dBc/Hz
3-MHz blocker: -13 dBm	2.9 MHz to band edge	~ -164 dBc/Hz

\* This number assumes that the noise due to phase noise is equal to 6 dB below the thermal noise of the overall receiver. The typical noise figure is 4 dB; therefore, the total thermal noise is  $-170$  dBm/Hz referenced to the antenna, and the equivalent phase noise would be 6 dB below this figure, or  $-176$  dB.

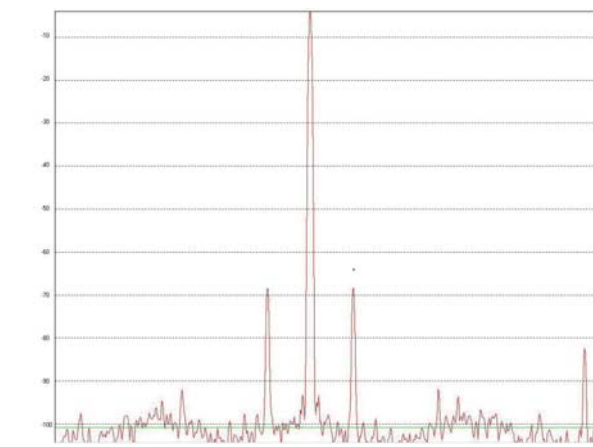
domain, equivalent to convolution of those two signals in the frequency domain, it may be less clear that the sampling process is also a multiplication-in-time process.

The sampling clock usually begins as a sinusoid and eventually drives a sample bridge circuit with a unit pulse of constant amplitude and finite duration at the zero crossing of the encoding signal. The results of this process are the multiplication of the unit pulse with the analog input in the time domain and, therefore, convolution in the frequency domain. Although the convolution between the clock and the analog input is true for the full signal spectrum, it is also true for the details of the spectrum that centers closely on the clock, because these signals become convolved with the detailed spectrum centering closely on the analog signal. Any phase noise associated with the clock becomes convolved with the analog input, distorting the spectral shape of the digitized analog signal. Because it is difficult to observe the phase noise of a clock, you can use a sinusoidal phase modulation to simulate the effects of a discrete frequency line of phase noise (Reference 2).

Spectrum analysis clarifies this convolution. Figure 2 shows the spectral nature of an encoding source with a 78M-sample/sec clock source that is phase-modulated at 100 kHz and with 0.001 radians of deviation. Due to the relatively low-level angle of modulation, only the first elements of the sidebands are visible above the noise floor. The first sideband is about -66 dBc below the power of the encoding signal. With an encoding signal voltage of 2V p-p, the value is 0.707V rms, and each spurious tone is 0.3543 mV rms.

By applying a phase-modulated signal to the clock port of the ADC, and a pure sine wave to the analog input port, you can see the replication of the sidebands of the clock on the analog signal as expected, by convolving the phase-modulated clock source with a pure sine wave (Figure 3).

The challenge is to predict the level of the phase noise. For sinusoidal inputs,



**Figure 4** A phase-modulated encoding source from Figure 2 samples a 108.62-MHz pure sine source, resulting in a side-spur level changes to -63 dBc.

Equation 4 characterizes the phase noise term exiting the ADC:

$$V_{\text{PHASE\_NOISE\_ADCOUT}} = V_{\text{PHASE\_NOISE\_ADCIN}} \times \left[ \frac{d(v_{\text{SIGNAL}})/dt}{d(v_{\text{CLK}})/dt} \right] \quad (4)$$

This equation assumes that the phase-noise voltage is the single-sideband voltage and correlates to the voltage of one of the sidebands in Figure 3. This equation simplifies to Equation 5 for most applications:

$$V_{\text{PHASE\_NOISE\_ADCOUT}} = V_{\text{PHASE\_NOISE\_ADCIN}} \times \frac{V_{\text{SIGNAL}} \times f_{\text{SIGNAL}}}{V_{\text{CLK}} \times f_{\text{CLK}}} \quad (5)$$

which applies to a sampling system and assumes that the encoding signal is sinusoidal. If the encoding signal is a logic signal, the slew rate does not depend on the frequency of the encoding signal, and an engineer can determine it from the man-

ufacturer's data sheet or with direct measurement.

In this simplified form of the equation,  $V_{\text{PHASE\_NOISE\_ADCIN}}$  is the level of the phase-modulated single-sideband signal or a single frequency line of the phase noise, modulated on the clocking signal.  $V_{\text{CLK}}$  is the rms level of the clock,  $V_{\text{SIGNAL}}$  is the rms level of the main analog signal,  $f_{\text{CLK}}$  is the frequency of the clock, and  $f_{\text{SIGNAL}}$  is the frequency of the main analog signal.

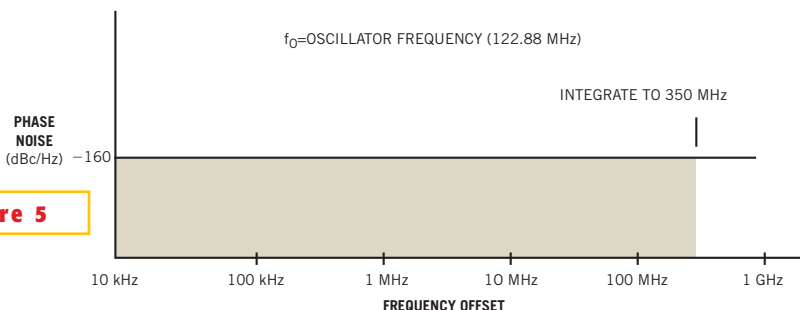
From either Equation 4 or Equation 5, you can predict the output spurious level if you know the clock's spurious voltage and frequency along with

the voltage and frequency of the analog input. Furthermore, the ratio of the signal voltage to the clock voltage, as well as the signal frequency and spurious frequency, directly impact the resultant spurious-signal values. Once you establish the ratio of the signal voltage to the clock voltage, you can predict the resulting spurious-signal level for a given input spurious signal. For this example, the ratio between the clock voltage and the signal voltage is 1-to-1.

When working with phase noise, it is customary to work in terms of decibels. Equation 6 can easily be reworked in terms of dB for any spectral line:

$$\frac{V_{\text{PHASE\_NOISE\_ADCOUT}}}{V_{\text{CLK}}} = \frac{V_{\text{SIGNAL}}}{V_{\text{CLK}}} \times \frac{f_{\text{SIGNAL}}}{f_{\text{CLK}}} \quad (6)$$

The log expressions of the equation define the relationship of the analog and clock voltages, as well as their respective frequencies.



**Figure 5**

Using a typical crystal oscillator as a clock yields extremely wideband phase-noise spectrum.

If the amplitude of the encoding clock and analog input are both 2V p-p (0.707V rms) and the associated clock phase spur is 0.3543 mV rms (-66 dBc), then by using either **Equation 5** or **Equation 6**, you can calculate the resultant side-spur level. If the sample rate is 78M samples/sec and the deviation is small, a full-scale analog input of 30.62 MHz should produce side spurs of about -74.1 dBc (**Figure 3**). At 108.62 MHz, the side tones should be about -63.1 dBc (**Figure 4**).

Note the degradation between these two measurements. If you compare either the SNR performance, which the side tones dominate, or the spurious performance with the calculations, the

**TABLE 2—ALLOWABLE ADJACENT-CHANNEL PHASE-NOISE REQUIREMENTS FOR CDMA2000 SYSTEMS**

CDMA2000 per spec	Offset	Performance*
50 dBc at 750 kHz	125 kHz	~ -107 dBc/Hz
87 dBc at 900 kHz offset	275 kHz	~ -144 dBc/Hz

\*Allows the noise due to phase noise to equal kT noise for the stated reference sensitivities.

degradation due to jitter that occurs as the frequency increases is as you would expect. As the input frequency increases, you would expect the energy due to jitter to increase by 6 dB for each doubling of the input frequency (doubling of the analog input slew rate).

In the example, the change from 30.62 to 108.62 MHz is a frequency ratio of 3.55 (not quite doubled twice), which ideally represents an increase in noise of

$6 \times \log_2(108.62/30.62)$ , or 10.9 dB. Between these two measurements, the spur level changed from -74 to -63 dBc, or 11 dB, as you would expect.

Both the wideband noise of the clock and the close-in noise are important, and it follows the same behavior as the wideband noise. However, the overall impact differs somewhat. Although the noise outside the channel bandwidth more or less uniformly increases the overall noise, the close-in noise causes reciprocal mixing and thus affects only nearby signals.

You can define two regions around the clock. The first starts at the center frequency of the clock and ends at one-half the desired channel bandwidth in both

## SPECTRAL DENSITY DEMANDS ANALYSIS

If you assume that the noise limitations of the sampling process are completely in the wideband noise of the clock, as opposed to 1/f noise (discussed separately), then it is possible to determine the wideband limitations to the clock source and to equate them to the traditional clock jitter equations.

To determine the wideband spectral density of the encoding clock, first determine the required output spectral density using **Equation A**:

$$ADC_{\text{SPECTRAL DENSITY}} = SNR_{\text{FS}} - 10 \log_{10} \left( \frac{\text{SAMPLERATE}}{2} \right)$$

Substitute the traditional equation for jitter into the equation for SNR, to give a direct method for determining spectral noise density with reference to jitter using **Equation B**:

$$ADC_{\text{SPECTRAL DENSITY}} = 20 \log_{10} (2\pi f_{\text{ANALOG}} t_{\text{JITTER RMS}}) - 10 \log_{10} \left( \frac{\text{SAMPLERATE}}{2} \right)$$

Because this **equation** assumes that wideband-noise density is uniform, it is valid for offset frequencies only from the point at which the 1/f noise intersects the noise floor up to the Nyquist rate on the high side of the desired signal and to dc on the lower side of the signal. Because high-performance converters have encoding bandwidths of 500 to 1000 MHz, noise on the encoding input aliases back into the Nyquist band many times.

Therefore, to determine the actual clock spectral density, an engineer must make an estimate on the unaliased spectral density of the noise. Because you assume that the noise is gaussian and noncoherent, you can make a close approximation by noting that each time the spectrum doubles, the noise doubles and vice versa. To make an estimate, use **Equation C**:

$$CLOCK_{\text{SPECTRAL DENSITY}} = 20 \log_{10} (2\pi f_{\text{ANALOG}} t_{\text{JITTER RMS}}) - 10 \log_{10} \left( \frac{\text{SAMPLERATE}}{2} \right) - 3 \log_2 \left( \frac{\text{CLOCK BANDWIDTH}}{\text{SAMPLERATE}/2} \right) - 20 \log \left( \frac{f_{\text{ANALOG}}}{f_{\text{SAMPLERATE}}} \right)$$

and determine the required wideband spectral density of the clock. Note that the results are valid for a narrowband, single-tone input to the ADC. The narrowband sine wave is almost always the worst-case

condition for a bandlimited analog input and useful in the analysis.

Conversely, spread-spectrum signals, such as those for CDMA2000 and WCDMA, are less stringent and usually lead to better performance than expected for narrowband sources. **Equation C** is useful for determining the required spectral density for a given jitter. Therefore, given an IF frequency and a jitter specification, you can approximate clock spectral density.

For example, if the IF frequency is 108.62 MHz, the jitter is 0.2 psec rms, the sample rate is 61.44M samples/sec, and the clock bandwidth is 350 MHz (limited by transformer coupling), **Equation D** shows the clock-noise spectral density:

$$CLOCK_{\text{SPECTRAL DENSITY}} = 20 \log_{10} (2\pi \times 108.62 \text{ MHz} \times 200 \text{ FS}) - 10 \log_{10} \left( \frac{61.44 \text{ MHz}}{2 \times 1 \text{ Hz}} \right) - 3 \log_2 \left( \frac{350 \text{ MHz}}{61.44 \text{ MHz}/2} \right) - 20 \log \left( \frac{108.62 \text{ MHz}}{61.44 \text{ MHz}} \right)$$

which computes to an NSD (noise spectral density) of -167.7 dBc/Hz. It is difficult to judge how much noise jitter contributes over and above thermal and quantization noise. In reality, jitter is in most cases the dominant contributor to NSD at high frequencies.

A typical data sheet shows that, at these frequencies, jitter dominates SNR, which typically approaches 73 dB full scale. Therefore, the expected NSD of such a clock would approach an average of -168 dBc/Hz over a typical 350-MHz span, indicating that it probably is higher closer to the clock frequency, and it is lower at the extreme.

You can use **Equation E** to solve for clock jitter and thus estimate the maximum allowed clock jitter, given the clock noise-spectral density and other terms:

$$t_{\text{JITTER RMS}} = \frac{10^{\left( \frac{CLOCK_{\text{SPECTRAL DENSITY}} + 10 \log_{10} \left( \frac{\text{SAMPLERATE}}{2} \right) + 3 \log \left( \frac{\text{CLOCK BANDWIDTH}}{\text{SAMPLERATE}/2} \right) + 20 \log \left( \frac{f_{\text{ANALOG}}}{f_{\text{SAMPLERATE}}} \right)}{20} \right)}{2\pi f_{\text{ANALOG}}}$$

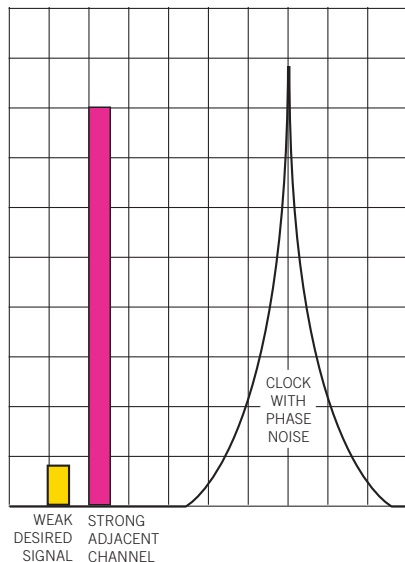
directions. In some cases, this region may comprise the entire Nyquist band, whereas in others, it may be somewhat less than the Nyquist band, depending on the end application. The second region starts one-half of the desired channel bandwidth away from the clock and ends at the bandwidth of the encoding logic for the data converter in one direction and down to dc in the other, including both internal and external limits; devices such as transformers sometimes limit this range. In most cases, the bandwidth of the encoding circuitry extends to several hundred megahertz and even into the gigahertz range on some wide-dynamic-range converters.

The encoding circuitry passes the spectrum that is convolved with the desired analog input during sampling, causing the spectral shape of the clock to appear on the analog signal itself (figures 3 and 4). However, because the ADC is also a sampled system, the wideband noise of the sample clock also aliases within the band of interest. This situation causes all of the wideband noise that enters the encode port to alias within the Nyquist band. This effect, in turn, results in a significant accumulation of the noise and a significant reduction in SNR.

All of the wideband noise aliases within the Nyquist spectrum, causing an accumulation of that energy and potentially increasing beyond the power within the close-in phase noise. If the encoding bandwidth is 750 MHz, the noise from this bandwidth aliases more than 24 times with a 61.44M-sample/sec clock. The effect is that the NSD (noise spectral density) from wideband jitter increases by almost 14 dB. At low analog frequencies, quantization and thermal noise also determine NSD.

In contrast, the close-in noise—the bandwidth of the signal of interest—cannot alias by definition and, therefore, contributes only once. The implications for implementation are that, although a fast-slewing edge is important for accurate clock-edge placement, limiting the amount of wideband noise on the clock can be of equal importance to maximizing converter performance, thus often making the balance tricky between the two.

For IF-sampling systems in which jitter is an issue, only jitter places a limitation on SNR (Equation 7):



**Figure 6** A comparison of the spectrum of adjacent weak and strong analog signals and the sampling clock before sampling shows relative amplitude and spacing.

$$\text{SNR}_{\text{FS}} = -20 \log(2\pi f_{\text{ANALOG}} t_{\text{JITTER}_{\text{RMS}}}), \quad (7)$$

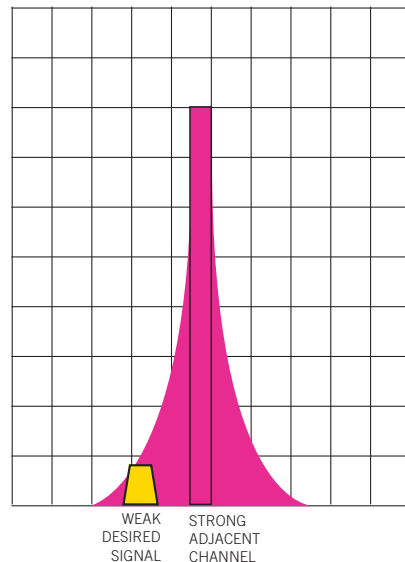
which lets you determine the clock-jitter requirement (Equation 8):

$$\frac{10^{-\frac{\text{SNR}_{\text{FS}}}{20}}}{2\pi f_{\text{ANALOG}}} = t_{\text{JITTER}_{\text{RMS}}}. \quad (8)$$

The frequently discussed close-in noise is usually 1/f noise. This noise is closest to the central frequency of the clock and experiences rapid decay as the offset frequency increases. The convolution process of ADC sampling simply mirrors this effect on the output. Therefore, the 1/f clock noise is primarily important in its effect on the phase error of the signal of interest and on reciprocal mixing of adjacent and alternative channels back into the desired channel. Once the 1/f noise reaches the noise floor, the emphasis changes to the wideband thermal noise that falls in-band. If the 1/f noise satisfactorily meets the requirements of reciprocal mixing, then the focus can be on the wideband thermal noise. You can determine the wideband limitations to the clock source and equate them to the traditional clock-jitter equations (see sidebar, “Spectral density demands analysis”).

#### PHASE NOISE AND JITTER

A direct relationship exists between phase noise and jitter (Reference 2).



**Figure 7** After sampling, the relative effects of phase noise of the clock shows that the analog signals now have the skirted shape of the clock and the spreading effect overpowers the weak signal.

When dealing with data converters, the wideband noise is generally the most important factor. Although not always the case, this assumption appears in a simple example, which shows the wideband noise characteristics of a typical crystal clock oscillator (Figure 5). This calculation omits the close-in, 1/f<sup>n</sup>, noise.

Although these numbers are important in the overall system, they are less important for the noise performance of the ADC, but more important for error-vector magnitude and reciprocal mixing. Therefore, you should consider them separately. To determine the jitter, the first step is to determine total noise power by integrating the noise over the bandwidth from 10-kHz frequency offset to 350 MHz in this case. Because 10 kHz is much smaller than 350 MHz, the lower limit barely affects the calculation for the case of wideband white noise.

Integration in the log domain is a simple addition operation. Equation 9 shows the total noise power:

$$\text{NOISE}_{\text{INTEGRATED}} = -160 \text{ dBc/Hz} + 10 \log [350 \times 10^6 - 10 \times 10^3] = -74.56 \text{ dBc}. \quad (9)$$

The next objective is to determine the angle of modulation, which you base on the observed power of the phase noise. The analysis can be simple for some cases and complex for others (see sidebar

“Determining the phase and jitter” on the Web version of this article at [www.edn.com](http://www.edn.com)).

Although you can determine wideband jitter in terms of wideband SNR and noise-spectral density, close-in noise differs. It is best to determine close-in phase noise in terms of reciprocal mixing, which occurs when a stronger signal is near the desired weaker signal. If the

clock or local-oscillator phase noise mixes with the undesired signal, it increases the noise floor of the desired signal. If the phase noise is large enough, it can overpower the desired weak signal and cause loss of that signal.

**Figure 6** shows the relative spectral densities of the signals. Note the skirted shape of the clock signal. When you use this clock to sample the analog input, this skirt

convolves onto all of the analog signals you are converting (**Figure 7**). The result is that all of the signals take on this general shape. The strong nearby signal now overpowers the weak desired signal, making it impossible to further process this signal.

You cannot determine the general requirements for close-in phase noise, because application requirements differ. However, once standards emerge for the spacing and level of typical signals, you can set phase-noise requirements. For example, based on the GSM requirements in Section 05.05, you can estimate the specifications based on the specified minimum sensitivity (**Table 1**). These specifications meet an overall noise figure of 4 dB and require that the antenna-referenced phase noise of the clock source be 6 dB below the effective noise-spectral density. In many cases, the reference sensitivity of a typical receiver is much better than the required minimum value. In addition, any selectivity you employ before sampling or mixing the signal eases the requirement in most cases on a decibel-for-decibel basis.

Similarly, you can determine the requirements for CDMA2000 (**Table 2**). Because CDMA2000 is a wideband standard, assume that the spectral density of the phase noise meets the conditions at the nearest corner and improves across the bandwidth of the channel. These assumptions ensure that nothing disrupts any portion of the channel or otherwise impedes the benefits of a distributed communications channel. Therefore, this case assumes that the contribution due to phase noise is  $-174$  dBm/Hz, the value of the thermal-noise limit. □

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#### REFERENCES

You can find the references to this article on the Web version at [www.edn.com](http://www.edn.com).

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#### AUTHOR'S BIOGRAPHY

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