



# THIRD-PARTY IP: A shaky foundation for SOC design

**COMMERCIAL MODULES HELP DESIGNERS MEET SCHEDULES AND COST OBJECTIVES, BUT RISKS ABOUND.**

**L**AWYERS HAVE LABELED reusable design blocks, or cores, as IP (intellectual property), despite the fact that most electronics designers use IP to mean Internet Protocol, and most engineers prefer to describe such products as “virtual cores.” Nonetheless, the use of “IP” as “intellectual property” has become prevalent, marking just one example of the confusion

surrounding this segment of the electronics industry. Although many analysts and marketing professionals point to the IP market as a new phenomenon in the industry, the technology and a market for third-party, reusable IP has been around for almost 20 years. Although the IP market is growing, it suffers from a lack of business and engineering standards. The lack of standard licensing practices and quality metrics too often offsets the advantage of obtaining verified, production-ready, implementations of standard logic functions is. Yet, given the shorter development time that today's electronics market requires, the use of reliable IP saves time, decreases the size of the development team, and may increase the market life of the product.

## IN THE BEGINNING...

Verification models were the first form of commercial IP available to designers. In the second half of the 1980s, small companies such as EIS Modeling sold logic-simulation models written for a number of simulators and emulators. Because standard modeling languages were just being introduced, most models were

*At a glance.....* **38** specific to proprietary simulators that used their own modeling language. As a result, vendors could not reuse most of the development effort, and the profit margin was low enough to keep large companies out of

*IP methodology starts with verification infrastructure.....* **38**

the business. As Verilog and VHDL became accepted, simulators using proprietary modeling languages disappeared from the market. But modeling companies, now using VHDL and Verilog, stayed in business with the added advantage that their engineering efforts now had a larger portion of reusability.

The introduction of logic synthesis provided another market opportunity for “ready-made functional blocks,” because few designers had the training or expertise to efficiently use synthesis. Often, the circuits that untrained designers produced were not optimal in size or speed. In 1991, to support its synthesis-marketing effort, Synopsys obtained a small library of logic cells from an engineer as the basis for a DesignWare library of modules. The DesignWare product, now enhanced and expanded to meet the capabilities of current logic-synthesis products, is still successful.

Just one year before the introduction of DesignWare,



a small company, HDL Systems, sold the architectural rights to the MIPS R3000 CPU under license from MIPS as a synthesizable module. HDL Systems produced both Verilog- and VHDL-synthesizable models of the CPU and sold it as source code with the appropriate synthesis scripts for a \$256,000 one-time license fee. Although the company had surprisingly good sales considering its pioneering status, it could never obtain financing to expand the product line. Philips Semiconductor eventually purchased the company and used the R3000 to develop derivative products for its semiconductor business.

Also in 1991, ARM introduced the ARM6, a microprocessor core sold under license to designers that needed to integrate a processor in their designs. Unlike HDL Systems, ARM found financing from Nippon Investment and Finance in 1993 and is now the world's No. 1 IP provider. Rambus, the second largest IP-product provider, began in 1990 as a developer of

**AT A GLANCE**

- ▶ Successful use of deep-submicron technology requires design reuse.
- ▶ The IP (intellectual -property) market is growing, and revenues now exceed \$1 billion, according to Gartner Dataquest.
- ▶ The top three IP suppliers control about 45% of the market.
- ▶ Platforms bundled with the proper EDA tools will fuel the next incremental growth.

a bus specification to improve the connection of DRAM to a microprocessor. The company continues to develop and market interface options for high-speed application-specific architectures.

Both established IP providers and many small design teams are offering reusable functional blocks for either outright sale or license to meet system-de-

signer demands. The IP market has grown from a few thousand dollars in 1988 to more than \$1 billion in 2003. Jim Tully, vice president and chief of research for the semiconductor sector at Dataquest, says, "In most cases, it does not make sense to design proprietary blocks for functions that are widely available in the IP market. Those functions do not differentiate a product, but they are 'must-have' functions in a system design."

**THE IP MARKET**

Tully expects the IP market to grow 28% for 2004. **Table 1** shows the market share of the top 10 suppliers in 2003. In the fall of 2004, ARM purchased Artisan and thus consolidated its lead in the market. Two of the three leading EDA companies, Synopsys and Mentor, are in the top 10 and have added to their IP inventory by purchasing both small and established IP companies. Jan Willis, senior vice president of industry marketing at Cadence, explains, "Cadence does not

**IP METHODOLOGY STARTS WITH VERIFICATION INFRASTRUCTURE**

*By Sean Smith, Denali Software*

IP (intellectual property) is key to enabling massive SOC (system-on-chip) designs. The use of commercial IP seems simple and easy at the surface, but the electronics industry must address a number of critical issues before it can realize IP's value. Physical issues aside, a cursory look at the functional aspect of verifying and integrating IP reveals some opportunities for significant strides toward a meaningful methodology.

A first step is for the design team to evaluate whether an IP core meets design requirements. In most, if not all, cases, the IP needs some reconfiguration or redesign for the target application. Once the IP consumer has selected a supplier to commit to the required modifications, it is still necessary to verify that the IP functions properly. Even if the IP supplier passes a rigorous verification audit, SOC designers must set up a local environment

to verify protocol functions and compliance, especially with modifications to the core.

Once the modified IP is stable and functioning properly within the protocol specifications, engineers must integrate it into the design for system-level verification. In this context, designers must create a mechanism for generating traffic scenarios within the system-level testbench to verify system-level performance and functions. For chip-to-chip interfaces, such as PCI Express or SATA-II, designers would also need to completely model other devices and initiate compliance from those other devices.

Although it's easy to characterize these issues at a high level, the tasks are enormous when you consider that a typical SOC incorporates several IP blocks, often from different suppliers. With functional verification consuming 70% of the development cycle, designers

cannot afford to build a new compliance testbench and system-level traffic generator for each protocol IP.

Verification is the largest impediment to IP reuse. And, despite all the smart people and companies in the market and those participating in efforts to establish IP standards, no solution is on the horizon. Meanwhile, SOC designs are emerging, and designers must make IP use successful for their chips.

To achieve success, chip designers are realizing that a practical IP methodology begins with a verification infrastructure. That is, SOC designers can invest in commercial VIP (verification IP), which serves a common platform to exercise and evaluate IP at a unit level, and then model other devices and drive traffic scenarios at the system level. Until recently, commercial VIP often consisted of only a BFM (bus-functional

model) and possibly a monitor for protocol checking. For VIP to be effective, it needs more features and functions.

Modern VIP offerings tend to be reconfigurable to support multiple protocols, and they offer more robust verification functions, such as directed random stimulus generation, protocol and temporal checking, functional coverage metrics, and reusable stimulus libraries. For verification reuse, VIP must provide easily or automatically configured stimulus libraries that can adapt to configurations and verification situations. These scenarios are more than simple test cases. They are reusable building blocks that enable teams to quickly and efficiently create the necessarily complex test cases.

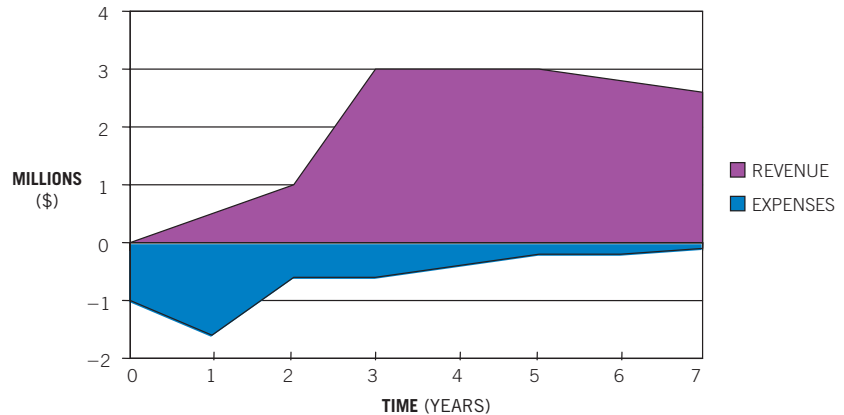
**AUTHOR'S BIOGRAPHY**  
*Sean Smith is a chief verification architect at Denali Software.*

see itself as an IP provider. We believe that merging IP and EDA is not what the customer wants.” Instead, Cadence offers OpenChoice, a program that makes third-party IP available to its customers, and is focusing on developing an environment that eases the integration of third-party IP into customer designs.

The IP industry appears to be following the EDA model as it matures. Large companies are acquiring products and technology by buying small companies. Michael Kaskowitz, general manager of the IP division at Mentor Graphics and chairman of the VSIA (Virtual Silicon Interface Alliance) consortium, states, “You can buy a small company for the cost of developing the same technology in a large organization.” Small companies generally exhaust their financial resources during product development and cannot survive the time required for their IP to become profitable.

Corporate revenue provides just one of the ways you can analyze the IP market. Another method involves dividing the market according to the type of products sold: digital, analog, memories, and verification IP. The digital segment accounts for most IP blocks sold. Microprocessor cores lead in number of units sold or licensed followed by DSP blocks. In addition to ARM and MIPS, other companies, such as Tensilica and FPGA vendors Altera and Xilinx, sell a large number of microprocessor cores. Altera offers its Nios processor, and Xilinx customers can integrate the PowerOne processor, which Xilinx licensed from IBM, into their FPGA designs.

However, neither Altera nor Xilinx appear among the top-10 revenue producers, because of pricing discrepancies between the ASIC and the FPGA markets. The IP blocks targeting the FPGA market sell for considerably less, because the FPGA vendors promote their semiconductor sales by discounting the price of the IP. Kaskowitz, speaking as the chairman of VSIA, observes, “Large IP providers cannot afford to service the FPGA market because Altera, Xilinx, and others are deeply discounting the IP prices to promote the sales of their parts. It is not unusual to see the same IP function sold at one-fifth of the ASIC market price in the FPGA market.” Un-



**Figure 1**

Developing an IP block requires significant upfront investments.

fortunately, the lower profit margins discourage industry leaders from entering this market and leave the segment to small providers, which can rarely afford to provide quality support to designers. Therefore, it is critical for designers to choose an FPGA vendor that can provide all the necessary IP blocks to simplify integration.

Rambus is the leader in interface-protocol IP. Most small IP suppliers address this segment of the market, because developing a block requires a smaller initial investment than developing a microprocessor or a DSP. The need to provide integration between functional blocks and increase the speed of data transfer has required the development of a number of standards, such as PCI Express and AMBA (Advanced Microcontroller Bus Architecture), which have further contributed to the growth of this market segment. Analog IP is a growing part of the market, even if none of the specialty-

product suppliers are among the top-10 revenue producers. More and more, SOC designs require analog functions, and the number of capable analog designers is significantly smaller than required. According to Mahendra Jain, chief executive officer of Qualcomm, “In the analog case, many companies do not have the expertise, so they have to buy IP from the outside or outsource the design.”

True Circuits is another leading provider of analog IP whose products are garnering interest. Because memories constitute a significant portion of SOC designs, providing self-correcting or -protected memories is important. Companies such as Virage Logic, CEVA, and Kilopass serve this market. Verification IP plays a key role in overcoming the verification and quality issues, which loom as barriers to IP reuse. Integrating a third-party IP block in design is difficult, and verification IP can significantly ease this process (see sidebar “IP methodology starts with verification infrastructure”). Embracing verification reuse brings customers and vendors a step closer to realizing the substantial benefits of IP. Companies such as Denali Software provide a way to test and verify that all blocks that communicate on a bus, such as PCI, function properly and always obey the protocol.

**PROBLEMS AND TRENDS**

The need for systems companies to continue to follow Moore’s Law to develop compet-

**TABLE 1—TOP 10 IP-MARKET REVENUES**

Rank	Company	2003 revenue (millions)	Growth (%)	Share (%)
1	ARM	\$175.2	-6	17
2	Rambus	\$118.1	21	12
3	Synopsys	\$81.2	11	8
4	Artisan	\$74.6	71	7
5	TTPCom	\$73.5	4	7
6	MIPS Technologies	\$40.3	-7	4
7	Virage Logic	\$40	-16	4
8	Ceva	\$36.8	-28	4
9	Imagination Technologies	\$23.6	54	2
10	Mentor Graphics	\$22.2	39	2
	Others	\$326	0	33
	Total	\$1011.5	4	100

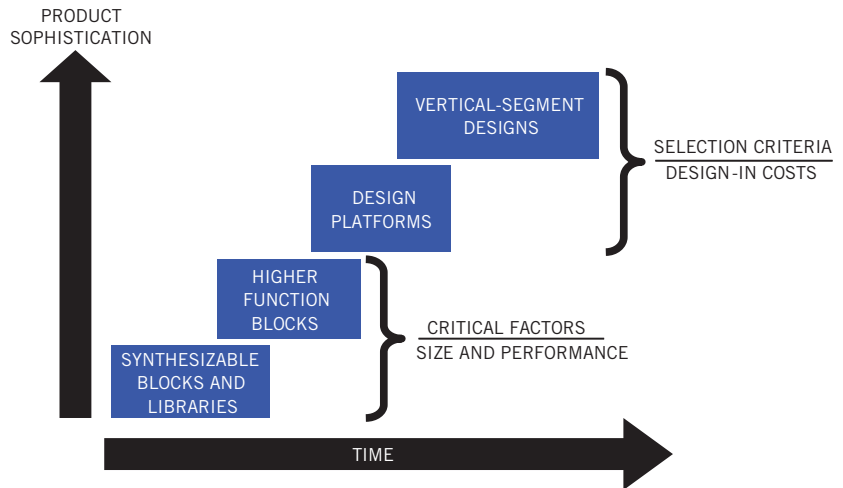
Source: Gartner

itive products has provided a significant boost to the IP market. The 130- and 90-nm processes provide such large die area that engineers can implement very complex systems on one die. The term “SOC” describes products that use these deep-submicron processes. The announced 65-nm process will be available for general production use in a couple of years and will only complicate the design problem. Most engineering teams lack the time and knowledge to develop SOC from scratch, so they reuse functional blocks to shorten development time.

A few problems slow the growth of the market. A major problem is the difficulty of evaluating an IP block without integrating it into a completed design. Richard Tobias, vice president

of the ASIC and Foundry Business Unit at Toshiba America Electronics Components, observes, “Typically, when you buy IP, you get a testbench with it, and, obviously, the IP works with that testbench. So, according to the vendor, [it has] produced a piece of IP that works. IP providers almost never provide an example of integration with a generic system.” Vendors attempt to minimize designers’ worries by offering hard IP that a customer-chosen foundry has successfully produced. Many designers share the notion that this type of IP works correctly and can be fabricated successfully, but that notion is incorrect, and it may in fact lead to additional problems. “‘Hardened’ means it is not changeable, so you have a difficult time to get the timing right if you cannot move a pin or modify a buffer when you are integrating the block with the rest of the design,” says Tobias. Qualcomm’s Jain concurs, “Customers think that buying IP is like buying a component, but this is not the case. Silicon is not quite like a pc board.”

As **Figure 1** shows, developers need to invest money for support and maintenance during the life of the product. John Weekley, director of business development at Synopsys, points out, “The IP product will continue to evolve over use, based on bugs that are found and corrected and updates and enhancements that are a given in any evolving technology. The IP will be stale, obsolete, and unusable unless resources are dedicated to maintain it.”



**Figure 2**

**Growing integration and functional sophistication will fuel the growth of the IP market.**

The IP industry has yet to achieve a standard procedure to handle contracts. IP blocks are distributed in various formats, from rare source code to hard IP consisting of a GDS-II file and directives for a layout tool. For processors or DSPs, software engineers often need information on the internal structure of the device that some vendors do not freely provide. According to Toshiba’s Tobias, it takes as long as six months to negotiate a distribution agreement for an IP block. Given the ever-shortening development times and narrowing market windows, such long negotiations can render a product obsolete even after development is complete. The VSIA, OCP-IP (Open Core Protocol International Partnership), and SPIRIT (Structure for Packaging, Integrating, and Reusing IP within Tool Flows) Consortium are all working on aspects of the IP market to develop various standard practices that will increase the productivity of all parties involved. They have made some progress, and some standards have emerged of late, but much work remains.

TTPCom, which focuses on wireless communications, and Imagination Technologies in the video-game market provide application-specific IP platforms. A platform system comprises a number of IP blocks that might include both hardware and software targeting the implementation of an application-specific system.

Toshiba uses its SOC Mosaic product line to implement CSSP (customer-specific-standard-product) ICs. Each IC in this family can contain as many as 50 or 60 digital and analog IP blocks and allows the customer to add both hardware and software components to quickly implement an ASIC device.

This type of IP significantly diminishes problems inherent in deep-submicron designs. For example, it comprises the largest percentage of the silicon and solves the parasitic and power-consumption problems that often critically impact this type of design. You can expect more offerings of this type from the largest IP vendors. Synopsys and Mentor will likely show that IP platforms are a natural expansion of the EDA market. These companies, as well as Cadence using third-party IP, can provide both the platform and the tools to efficiently integrate customer-specific hardware and software in a design. **Figure 2** shows the likely progression in market maturity: increasingly sophisticated and complex products as process-technology and vendor experience continue to improve. □

**FOR MORE INFORMATION**

For more information on companies in the IP market, please visit [www.edn.com/community/2813/EDA+Tools+and+IP+Cores.html](http://www.edn.com/community/2813/EDA+Tools+and+IP+Cores.html).

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You can reach Technical Editor Gabe Moretti at 1-941-497-9880, fax 1-941-497-9887, e-mail [gmoretti@edn.com](mailto:gmoretti@edn.com).

