

DECADES OF PROCESS DEVELOPMENT HAVE MOSTLY FOCUSED ON INCREASING THE DENSITY AND SPEED OF LOGIC. MINIMUM GATE DIMENSIONS HAVE FALLEN FROM MICRONS TO LESS THAN 100 NM. THE WORLD AROUND YOU, HOWEVER, HAS NOT UNDERGONE ANYTHING LIKE A SIMILAR PROCESS REDUCTION, SO SIGNALS, NOISE, AND APERIODIC EVENTS ARE AS BIG OR BIGGER THAN EVER FOR MANY APPLICATIONS. WHAT'S AN I/O DESIGNER TO DO?

# INDUSTRIAL- STRENGTH ANALOG

**P**URVEYORS OF MODERN, high-speed logic would like to think of their products as the center of the technological universe, and perhaps they are right. But before information gets to the center, it needs to travel from its peripheral origins, and, to be useful, the processed information needs to travel back out to the periphery—that cluttered nonsilicon world of people, machines, and their

natural surroundings. And, despite the fondest wishes of those whose world extends nary a micron beyond the core, the natural universe—far away from convenient, familiar, and occasionally self-serving abstractions—remains steadfastly analog.

There is no doubt that analog IC technologies have followed logic down the path to smaller signal swings, greater integration, and the enormous economies of scale associated with vanilla CMOS and its near variants. Indeed, by taking advantage of fab equipment just a few process generations older than the current state of the art, analog- and mixed-signal-IC manufacturers have benefited from high-yielding, low-voltage processes running on largely depreciated equipment, further reducing factory costs. Accordingly, analog-signal-pro-

cessing blocks operating on fewer than a handful of volts have enjoyed great commercial success and garnered impressive profits for those companies that can ply the analog craft within the confines of CMOS-IC technologies.

As economic as low-voltage-signal processing is, such technology is rarely suitable for an application's physical interface, which defines the electrical conditions for analog-I/O structures. Thus, though industrial applications typify the requirements and design challenges related to robust interface-circuit design, similar issues arise in environments as disparate as test-and-measurement instrumentation, medical electronics, automotive systems, communications, and consumer electronics. Yet, until fairly

recently, most of these applications depended on semiconductor-fabrication processes that have evolved over the years but rarely enjoyed a significant departure from their evolutionary track. Meanwhile, the economic forces that drive low-voltage-IC designers toward smaller geometries can work against chip makers that must accommodate large signal swings (see **sidebar** "The economies of scaling"). Recently, several major analog- and mixed-signal-semiconductor manufacturers have deviated from this trend, developing new, more compact processes and still preserving the robustness that I/O functions require.

## LITTLE PROCESSES THAT CAN

The dielectric breakdown of device layers, such as gate

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oxides, often limits the operating voltage for a given process and device design. But that view looks from the process outward with operating voltage as a parameter—a reasonable perspective as long as a sufficient SNR is attainable within the signal-voltage limits that the process imposes. Indeed, considering the energy required to charge stray capacitances with every signal transition— $E_c = C(\Delta V)^2/2$ —small operating voltages bring a disproportionate energy savings.

But the view from an industrial application's perspective differs greatly. In this case, nominal signal voltages are given—commonly  $\pm 5$  or  $\pm 10V$ —and other attributes in the IC manufacturer's domain are parametric. The problem isn't to scale signals to the device capability, but to scale the device capability to the signal requirements. This distinction affects more than just minimum dimensions, such as gate-oxide thicknesses and electrical lengths; minimum-sized devices do not dominate designs in these applications to the extent that they do in, say, logic designs. Furthermore, the larger operating voltages not only affect individual devices, but also increase device spacing to isolate adjacent devices. An increase in the spacing between devices results in a total area devoted to an individual device that grows a bit faster than linearly (Figure 1).

Process and device engineers—in many ways the unsung heroes of the semiconductor industry—have for decades been striving to make gains on the voltage/scale curve, using combina-

#### AT A GLANCE

▶ Improvements in high-voltage analog processes are allowing greater integration and more effective mixes of analog and digital circuits.

▶ As submicron high-voltage processes become more entrenched, both chip makers and OEM designers will need to rethink their approaches to functional segmentation.

▶ As operating and signal voltages rise, so does the need to consider protection schemes to cope with anomalous and fault conditions.

tions of process chemistry and device physics. Virtually all of the large analog- and mixed-signal-semiconductor suppliers have put significant effort into these developments. One new process that exemplifies the trend is iCMOS from Analog Devices, which the company announced at the most recent Electronica show in Munich. Comparisons between iCMOS and older high-voltage processes indicate the extent of the newer processes' space savings (Figure 2). In addition to saving valuable chip real estate, the process also brings improved power efficiency and provides the means of integrating signal-conditioning and -processing circuits on the same chip. "Industrial designers considering an analog-CMOS [signal-processing] product for its cost or power efficiency bene-

fits were forced to add significant levels of signal conditioning [and] signal biasing ... to get the high speed and low power consumption required to interface [signal-processing functions] to high-voltage industrial systems ranging from actuators to sensors," according to Denis Doyle, a process-development fellow at Analog. "Under those conditions, manufacturing technologies capable of handling 30V were in the range of 3 to 5 microns, and adding digital functionality caused [chips] to grow to unacceptable sizes." By contrast, the new submicron process allows greater integration by isolating small lower voltage parts from the substrate potential, which provides chip designers greater freedom to move signals from the I/O level to lower voltages on one die (Figure 3).

The modular process includes two sets of complementary bipolar transistors. One set can operate to 16V and features cutoff frequencies of 6 and 4 GHz for the npn and pnp, respectively. The second set can operate to 30V and yields a 1-GHz cutoff frequency for both polarities. Additional process modules provide switchable polysilicon-polysilicon capacitor arrays and low-temperature-coefficient and low-voltage-coefficient thin-film resistors, which provide good initial ratiometric matching and an in-factory trim capability. On-chip memory and logic capability allow both factory and OEM chip configuration.

As advanced high-voltage analog processes displace older processes less able to

## THE ECONOMIES OF SCALING

For a given process and wafer size, an IC's fab cost is roughly linear in area. Large die fall off the curve because of the falling area efficiency of tessellating rectilinear chips on a circular wafer. Small die also fall off the curve because of the disproportionately large area that fixed-width scribe streets consume. These streets separate adjacent die and provide a safe area for the saw kerfs during the back-end dicing operation. Between the two ends of the die-area range, die cost per unit area is near constant.

Die cost per unit area is by no means constant with the pro-

cess's minimum feature size as a parameter. Small features require more expensive photolithography tools and are less tolerant of small process variations. Meanwhile, the size of an individual active device is parametric in a number of factors, one of which is operating voltage. Large devices near an IC's I/O pins are thus more expensive than minimum-sized devices that form much of the internal circuitry.

A bit more challenging is the fact that devices scale in three—not just two—dimensions. As logic processes pushed minimum dimensions from near-submicron

to deep-submicron, gate-oxide thicknesses needed to scale, as well. Indeed, early on, one of the challenges in commercializing the 90-nm process node was forming reliable gate oxides that are only several molecules thick.

Large signal swings would punch such a thin oxide layer, so the choice has been to complicate the process with multiple oxide thicknesses beyond the standard gate and field oxides or to manage the integration-versus-segmentation balance in such a way as to move the large signals off the deep-submicron process.

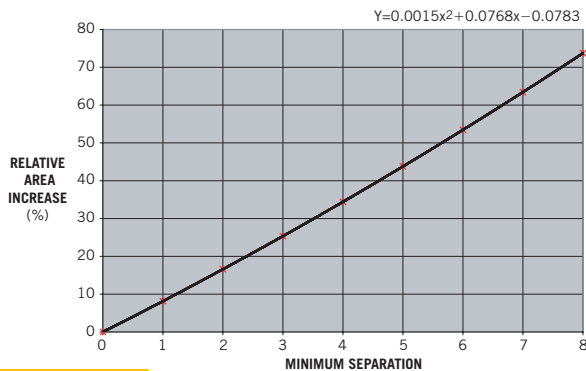
But, as the competitive envi-

ronment has heated up in sectors that exploit or are subject to, depending upon your perspective, large signal swings, semiconductor vendors have sought to improve the economies of high-voltage processes. Recent activities have borne several submicron processes that support operating voltages of several tens of volts. One of the many challenges in such developments is to create a high-yielding process that can support analog, digital, and limited power circuitry with only minimally increasing the mask- or process-step counts.

support high levels of integration, both IC and OEM designers will have reason and the rare opportunity to re-think long-established segmentation schemes for common I/O signal chains. In the meantime, the most immediate use of the technology is likely multichannel versions of individual functions and die and package reductions of single-channel devices. In both cases, chip makers may be able to provide OEMs with significant savings, not only by shrinking the silicon area to implement a function, but also by bringing more of the off-chip components onto the die.

The six-channel AD7656 ADC is a good example of the trend. An input structure, including six on-chip track-and-hold amplifiers, accepts signals in either a  $\pm 5$  or  $\pm 10V$  range, programmable in channel pairs. Each amplifier feeds a 16-bit SAR (successive-approximation-register) converter. Application circuits can simultaneously trigger the six converters or independently trigger converters in pairs. The sample rate is 250k samples/sec per channel, and the full-power bandwidth is typically 8 MHz, allowing you to use the 7656 in undersampled applications.

Minimum SNR and maximum THD are 83 dB and  $-97$  dB, respectively. The converter's dc performance specifications include  $\pm 2.1$ -mV zero error,  $\pm 4$  LSB maximum integral nonlinearity, and no missing codes to a 15-bit resolution. The converter's output data is available through both parallel and high-speed-serial interfaces. The \$17 (1000), self-clocking converter fits into a  $12 \times 12$ -mm LQFP-64 package and dissipates a maximum 192.5 mW at its 250k-sample/sec conversion rate. In power-down mode,



**Figure 1** A process's maximum operating voltage limits the interdevice spacing and the minimum device size. Not surprisingly, the curve describing the total area devoted to a single device as a function of the spacing is slightly hyperbolic.

the dissipation falls to a maximum of 16.5  $\mu W$ . Reduced-resolution versions, the \$12.95 (1000), 14-bit AD7657 and \$10.60 (1000), 12-bit AD7658, are also available in the same package.

Commercial chip makers are by no means the only semiconductor manufacturers developing advanced high-voltage analog processes; foundry fabricators are keeping competitive, too. Austriamicrosystems, for example, which operates both foundry services for fabless semiconductor companies and an IC-development organization for its own branded products, has developed the H35 high-voltage, 350-nm, BiMOS process, which includes 20 and 50V MOS devices, bipolar transistors, capacitors, and high-resistivity polysilicon resistors. The process can fabricate MOS devices with channel resistivities on the order of 0.04 $\Omega$  mm<sup>2</sup>. Available libraries cover digital, analog, and high-voltage elements, as well as peripheral cells with high-output-drive capability.

H35 is an automotive-qualified modular extension of a 350-nm standard-CMOS process that Austriamicrosystems has licensed from TSMC. Despite its apparent flexibility, the extension adds only two mask layers to the basic process. Ac-

ording to Austriamicrosystems' Full Service Foundry Senior Vice President Peter Gasteiner, the company "plans to fully characterize HV devices for 120V" in the future. Meanwhile, the company offers back-end assembly and test services to complement the primary fabrication service. The company also offers quarterly multiproject wafer shuttles, which can help reduce custom-silicon-development costs and time to market. A design kit compatible with Agilent-ADS, Cadence, and Mentor Graphics environments includes simulation

models, active- and passive-device libraries, logic gates, peripheral cells, and simulation models for several IC packages.

#### ACTUATING THE ACTUATORS

The 120V process goal that Gasteiner suggests may sound stratospheric, but several applications require such potentials and greater, particularly for optical, lighting, and transducer drivers. Goal Semiconductor, for example, offers these applications its HVDAC200 quad, high-voltage, 9-bit DAC. Each channel sums the output of its 9-bit main DAC with a 5-bit offset DAC—a calibration aid in many applications. Each sum drives one of the DAC's four output stages, which are current sources that you can configure as a group for either 500- $\mu A$  or 5-mA outputs. You can either select on-chip 600-k $\Omega$  resistors or connect external loads to convert current outputs to voltages. Be sure, however, not to exceed the output stage's compliance voltage lest you clip the output.

In addition to the 5V nominal analog and digital power supplies, a 20 to 200V supply provides the current sources' compliance voltage. Additional on-chip facilities include a temperature sensor, a voltage reference, and overcurrent output protection. The \$2 (production quantities) DAC's maximum conversion rate is 17k samples/sec. Its integral and differential nonlinearities are limited to  $\pm 0.5$  LSB.

Motor-drive amplifiers, at one time rack-mounted devices, have long been available as modules and hybrids for applications requiring moderate currents. Apex Microtechnology, a well-established company in the hybrid segment of

### FOR MORE INFORMATION...

For more information on products such as those discussed in this article, contact any of the following manufacturers directly, and please let them know you read about their products in *EDN*.

<b>Agilent</b> eesof.tm.agilent.com	<b>Austriamicrosystems</b> www.austriamicrosystems.com	<b>Mentor Graphics</b> www.mentor.com	<b>Panasonic Mobile Communications</b> www.panasonicmobile.com
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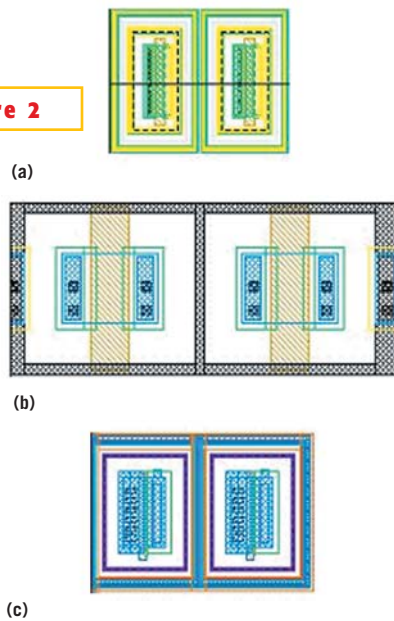
the market, has developed a line of monolithic amplifiers. The company's PA60 dual-amplifier IC can operate on split or unipolar supplies totaling 5 to 40V and delivers a peak 1A from a PSOP-20 package selling for \$6.05 (100) or 1.5A from a SIP-12 package selling for \$8.40 (100). Motor-drive applications include computer peripherals, automotives, and avionics.

The PA60 can form a full-bridge, bidirectional, variable-speed motor drive with one IC package and six external resistors (Figure 4). The amplifier provides a minimum 900-kHz gain-bandwidth product and typical 13.6-kHz full-power bandwidth. The outputs can swing to within 1.8V of the rail over temperature at 1A load current, and they slew at a minimum of 1V/ $\mu$ sec. With 0.02% typical harmonic distortion, you could also use the PA60 as full- or half-bridge audio power amplifiers in medium-fidelity applications, such as external computer speakers.

Low-power-audio-amplifier applications, such as cell-phone- and laptop-speaker drivers, need to provide relatively large currents at low voltages for common low-impedance dynamic transducers. The current drain through the audio subsystem is one of the factors that tend to limit per-charge operating time in such devices. Panasonic Mobile Communications has reduced the space and power that the primary speaker in a mobile-phone handset requires by replacing the dynamic driver with a smaller, high-impedance ceramic speaker, such as those from Taiyo Yuden. Another emerging approach to reducing speaker footprint and power replaces the traditional speaker with a piezoelectric actuator, such as those from NXT. These developments pose a common challenge to handset designers: The ceramic speakers and piezoelectric actuators both require higher drive voltages than those available from standard audio-power-amplifier ICs operating on lithium-ion batteries. Unlike the dynamic speakers that they replace, ceramic speakers require as much as 12V p-p; piezo speakers require 24V p-p.

National Semiconductor's LM4960 piezo driver and the LM4961 ceramic-speaker driver each combine an on-chip boost converter with an audio power amplifier. These newest members of National's Boomer

**Figure 2**



**Newer high-voltage analog processes, such as iCMOS (a), compare positively with older 30V processes (b), and even current 1-micron, 24V processes (c) (courtesy Analog Devices).**

line feature a click-and-pop-suppression circuit, which provides graceful transitions between operating states and a low-power shutdown mode. The LM4960's boost converter operates at a fixed 1.6 MHz and drives a dual audio power-amplifier to deliver 24V p-p in a full-bridge mono configuration with less than 1% THD. More typically, THD+noise is 0.04%. The amplifier's minimum 50-dB power-supply rejection ratio reduces the effects of inband ripple on the low-voltage supply input to inaudible levels. The \$2.50 (1000) bridge amplifier provides overcurrent and overtemperature shutdown as well as a shutdown mode you can invoke from your application.

The LM4961 includes a low-power mode for ear buds, in which the amplifier operates on the power input from the

phone's lithium-ion battery. A high-power mode for ring tones and hands-free speakers uses the on-chip boost converter. In this mode, the driver can typically develop 15V p-p with less than 1% THD. The \$2.10 (1000) amplifier's maximum 14-mA quiescent current drops to a maximum of 4 mA in "receiver mode"—an active-standby mode that can track the phone's transmit/receive switch. Shutdown current is no more than 2  $\mu$ A.

**DESIGN NOTES**

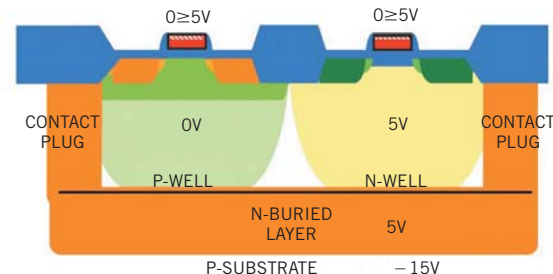
Often as operating voltages increase, so does the available energy that an application must manage, both under normal operating conditions and under fault conditions. Though circuit protection is rarely a concern beyond the power-supply design in applications that operate on a handful of volts or less, you may need to protect I/O nodes, particularly in systems operating on significantly higher voltages.

In I/O-subsystem designs that accommodate large input signals, be sure to compare the I/O device's input topology and ratings, including input-protection circuits, with the expected range of signals under both normal and abnormal operating conditions. For example, if a field-wiring fault in a current-loop-monitoring application can drive a nominal 10V input to a 48V rail, then you should determine the pin's behavior at that elevated potential. Most IC signal pins feature clamp structures that alleviate voltage-overstress conditions and suppress transients from ESD or similar events. There is a limit, however, to the amount of current the clamps can tolerate without sustaining damage. You may need to add a resistor in series with the input pin to limit the current below the damage threshold.

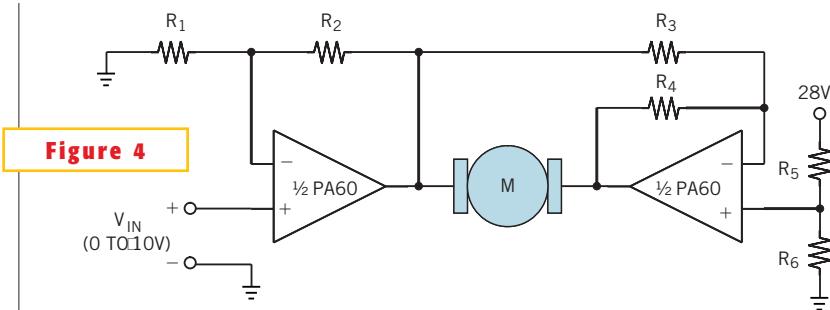
You can determine the lower limit on such a protection resistor's value from the maximum sustainable fault voltage and the maximum tolerable pin current. Don't forget that, in applications that span large areas, signals may be present when the power to the input device is off. The positive clamp, in such a case, may be at ground potential rather than at the nominal supply.

Either noise concerns or the application's tolerance for offset

**Figure 3**



**One effective method for integrating low-voltage mixed-signal circuits with high-voltage analog builds low-voltage MOSFETs of either polarity in wells that provide isolation from the substrate potential (courtesy Analog Devices).**



**Figure 4**

The Apex Microtechnology PA60 dual-IC power amplifier can implement a bidirectional motor drive with few external components.

voltage and offset drift limit the resistor's maximum value. Input bias currents, which these resistors convert into offset voltages, double every 10°C in MOS amplifiers, so include the maximum room-temperature bias current and the maximum operating temperature in your calculations. As a side benefit in cases with input signals that require bandwidth limiting, the same resistor that protects the input from fault conditions can do double duty serving as the resistance in an RC lowpass filter.

Just as input structures may require ex-

ternal components to complement on-chip-protection features, so may outputs.

Wiring faults or load failures can cause overcurrent conditions. Some devices provide explicit current limiting on their outputs or have output structures that are suitably robust as to tolerate their own short-circuit current without sustaining damage. Others may require external protection, which may range from external current

limiters to standard or resettable fuses. Load reactances can also complicate protection schemes by introducing fault modes that don't exist with purely resistive loads. For example, a load that includes a large shunt capacitance looks like a short to ground during a power-up sequence. If input signals are present when you energize the output stage, large currents can flow while the load capacitance charges. Similarly, large series load inductances from long wiring runs, for example, can develop inductive kickback voltages if a sudden change in load current occurs. Check your I/O-drive circuit's overvoltage and overcurrent capability and any on-chip protection.

Also check the phase margin when driving a load with a substantial reactive component in a closed-loop topology. □

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