



Understanding Spice models

TO ENSURE A COMPLETE AND ACCURATE Spice analysis, you must verify your selected Spice model. Verification is a three-part exercise: Verify dc performance to ensure dc accuracy, ac performance to verify ac

accuracy, and boundary conditions to investigate nonlinear behavior. Use the circuit in **Figure 1** to verify the dc gain and input bias current of an op amp.

Run a dc analysis on the circuit in **Figure 1**, table the data, and have a data sheet handy. The outer limit for the calculations is 20% of the typical numbers in the data-sheet specifications. (10% is much better.) If the calculated values vary from the data-sheet specifications by more than 20%, the designer must evaluate each out-of-limit parameter to determine whether it

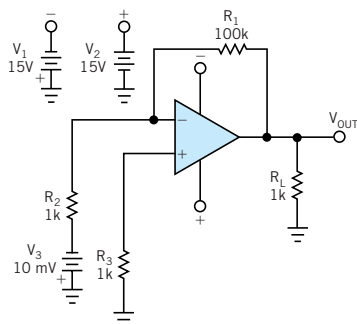


Figure 1 The inverting op-amp configuration yields bias current and dc-gain analysis.

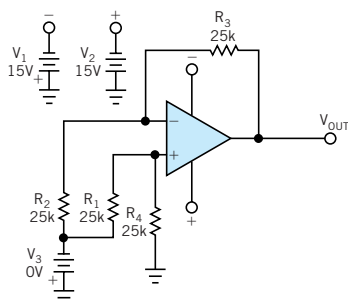


Figure 2 This circuit requires 0.0001% matched resistors, so it is impractical for lab use.

can influence the design.

The first measurement is the noninverting input bias current, which is the current in R_3 . It should be approximately equal for

VERIFY DC PERFORMANCE TO ENSURE DC ACCURACY, AC PERFORMANCE TO VERIFY AC ACCURACY, AND BOUNDARY CONDITIONS TO INVESTIGATE NONLINEAR BEHAVIOR.

both inputs and approximately equal to the input-bias-current specification in the data sheet. The input bias current varies from picoamperes to microamperes depending on the IC process and type of transistor you use. $I_{R1} - I_{R2} = I_{BIAS}$; thus, the currents in R_1 and R_2 are normally unequal, causing an output-voltage error. Very low bias current is negligible when compared with the signal current, so under low bias-current conditions, it appears that $I_{R1} = I_{R2}$. When the designer selects R_3 equal to the parallel value of R_1 and R_2 , the bias current creates a common-mode offset voltage, and the op amp rejects common-mode voltage.

The equation for the op-amp gain, a , is $a = V_{OUT}/(V_+ - V_-)$, which reduces to $a = V_{OUT}/V_-$ when the signal current is much greater than the input bias current. Again, the calculated dc-op-amp-gain value should be within 20% of the data-sheet value. Running a series of simulations with closed-loop gain, power-supply voltage, load resistance, and other parameters as variables yields more data. A worst-case Bode analysis demands that the Bode calculations use the highest possible loop gain, and this data establishes it. The dc loop

gain is the intercept point for the ac loop gain, so it is a required point for establishing the overall loop gain.

It is necessary to verify the dc CMRR (common-mode rejection ratio), which you can calculate using the circuit in **Figure 2**.

Using this circuit for laboratory measurements requires resistors matched to 0.0001% to measure CMRR greater than 100 dB. This matching is extremely hard to

accomplish on an ongoing lab basis, thus CMRR measurements use more complicated circuits. Spice uses perfect resistors so it can measure the CMRR with the circuit in **Figure 2**. For this circuit, $CMRR = 20 \log(2\Delta V_{IN}/\Delta V_{OUT})$. First, set the battery equal to 0V and record the output voltage. Next, set the battery voltage to 1V and record the output voltage. The resulting data gives a reasonably accurate dc CMRR that should compare favorably with the data-sheet CMRR. Now you can vary the input-voltage range, power-supply range, and other parameters, to obtain CMRR data as a function of them.

Although these dc-measurement techniques are valid, they contain approximations and assumptions that need periodic examination. For instance, these calculations neglect input offset voltage, which could be important in some applications. After dc verification of the model, you need an ac verification of the model—the topic of my next column. □

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