

ALTHOUGH A NUMBER OF RECENT PUBLICATIONS HAVE OUTLINED THE BENEFITS OF USING DIFFERENTIAL SIGNALLING TECHNOLOGY OVER SINGLE-ENDED TECHNOLOGY FOR SERIAL INTERFACES, LESS INFORMATION EXISTS ON THE HIDDEN FORCES DRIVING SUCH MIGRATIONS AT THE SIGNAL-TRANSMISSION LEVEL.

Low-Power Differential Interface Technologies for Portable Products

Designs in the consumer and communications sectors are witnessing a transition from parallel to high-speed serial I/O solutions. Interface technologies that can balance the conflicting requirements for very high data rates, at lower power consumption, and with improved EMI performance are experiencing rapid growth. This article analyses the architectures of the most commonly used differential signalling technologies to illustrate the trade-off between power consumption, throughput and electromagnetic interference (EMI) emission. It also introduces a new I/O approach, current transfer logic (CTL).

KEY SPECIFICATIONS

As the resolution of high-end cell phone LCD displays exceeds SVGA (800×600), the RGB data throughput between the application processor and the LCD module can become very high. For XGA mode with a 60 Hz refresh rate, it can exceed 750 Mbps. The high magnitude swing (0 to V_{cc}) of existing TTL technology between the baseband controller and the LCD module restricts the signal data throughput between logic transitions, especially with the regulatory EMI requirements limiting the edge rate. If it is not possible to meet these conflicting demands, the project team may be forced into a redesign of the baseband chipset itself.

In addition, since next-generation camera phones offer a pixel resolution of more than three million, the RGB data throughput read back to the baseband processor for snapshots pushes the limits of

existing TTL technology. The same challenge applies to consumer designs such as high-speed DVD-RW design (at over 16× speeds), where a high volume of data is transferred between the Read/Write controller and the laser diode driver (LDD).

For most battery-powered devices, power consumption remains a factor that must always be considered. Any interface technology adopted in baseband design needs to have ultra-low power consumption, in addition to meeting the throughput requirements. The dynamic power consumption of any such device is a function of load capacitance, signal swing, power supply and data rate. Reducing the signal swing allows existing technologies, such as LVDS, TMDS and CML, to reach very high throughput, although the power consumption for these interfaces may still be out of tolerance for portable design requirements. The capacitance load on driven signal lines is also a major factor that limits the data throughput for these technologies.

NOISE MARGIN

In most portable and consumer electronic designs, connections are typically over low-bandwidth flex cable or even ultra-low-bandwidth ribbon cable. The low-bandwidth media can eventually degrade the signal edge, cause signal attenuation, and generate reflections in long cables. For example, in DVD-RW and DVD changer applications, the distance between the DVD-RW processor and Laser Diode Driver (LDD) can be more than 400 mm. To

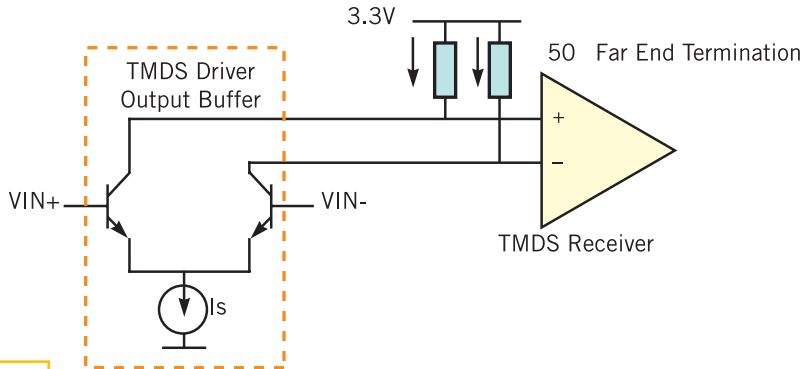


Figure 1

Simplified TMDS input/output buffer

minimise the bit error rate while maintaining the capability to drive a usable cable length, it is critical to have sufficient noise margin, defined as the difference between the driver output voltage and the corresponding receiver input threshold voltage. Longer cable driving capability becomes a very desirable attribute when using low-bandwidth media such as flexible cables. This allows the designer more flexibility in the routing of the signal data path.

Traditional TTL technology has typically used large signal amplitudes with faster edge rates, resulting in reflections and EMI problems. Slowing down the edge rate of the TTL signal reduces the reflections and EMI, but limits the throughput—particularly on low-bandwidth cable. Furthermore, for applications such as cell phone designs, the RF noise and other EMI noise surrounding the flex cable between the baseband processor and LCD module or camera image processor is significant.

Accordingly, differential technologies such as Transition Minimised Differential Signalling (TMDS) and Low Voltage Differential Signalling (LVDS) come into play with improved throughput, noise immunity or EMI performance. But these technologies still consume a considerable amount of power, which is not desirable in battery-operated devices.

DIFFERENTIAL SOLUTIONS

Currently, two interface technologies dominate in portable and consumer designs. The TMDS signalling scheme is mainly adopted by the HDMI and DVI standard as the link for both HDTV digital video/audio and the PC monitor RGB data link with speeds as high as 1.65 Gbps. LVDS is also widely used in flat-panel display designs to transmit RGB data between the LCD controller and LCD Modules (LCM). These two technologies are very similar except for the difference between the sink or source current scheme.

The TMDS-based driver typically has an open-drain or open-collector output with far-end termination to Vcc (3.3V) for transmission line impedance match. The output buffer usually is an amplifier-type architecture with a constant tail current of typically 10 mA. The typical swing of the single-ended signal is about 500 mV, and the differential swing is 1000 mV_{p-p}. The common-mode signal of the driver output is Vcc - 0.25V.

The TMDS driver (Figure 1) sinks the current at its plus or minus line from the far-end termination voltage, depending on the logic input. This creates a voltage drop over the termination resistor, which is sensed as logic “1” or “0” by the receiver. Depending on which line is sinking the current, the other line will be pulled high to Vcc by a 50- termination resistor. Thus, the latter not only acts as a matching resistor ($R_t=Z_0$) for signal integrity purposes, but also performs the job of creating a voltage drop for logic “0”. Z_0 is the characteristic impedance of the cable or traces. The resistor value is critical for both signal integrity and noise margin in terms of signal magnitude. Typical standards require a 10%-tolerance in the resistor value. In order to perform high throughput transfer and maintain a satisfactory noise margin for the receiver, the TMDS link could have a rise/fall time as fast as 75 psec. This fast edge rate can cause very fast current switching, with worsening EMI as throughput rises. For these reasons, designers mainly use TMDS for high-speed data transfer in applications such as digital YCbCr video signals. However, they attain this high throughput at the cost of high power

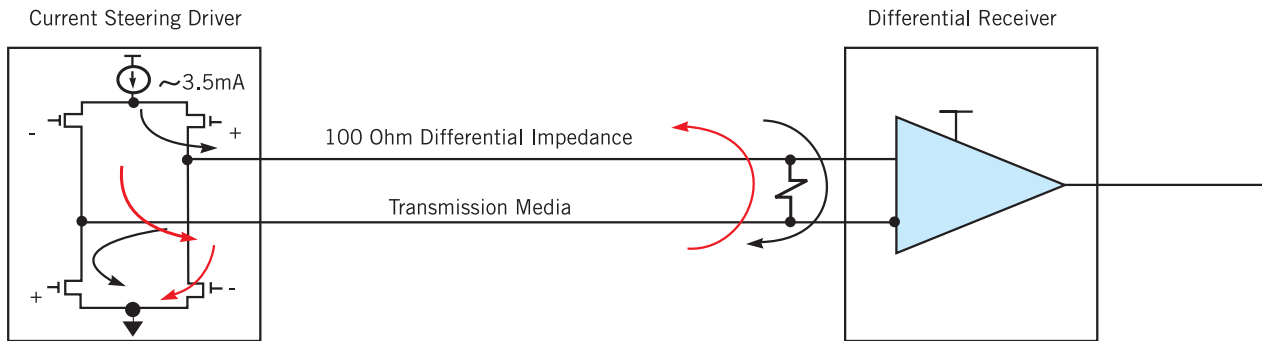


Figure 2

Conceptual schematic for the LVDS differential driver/receiver

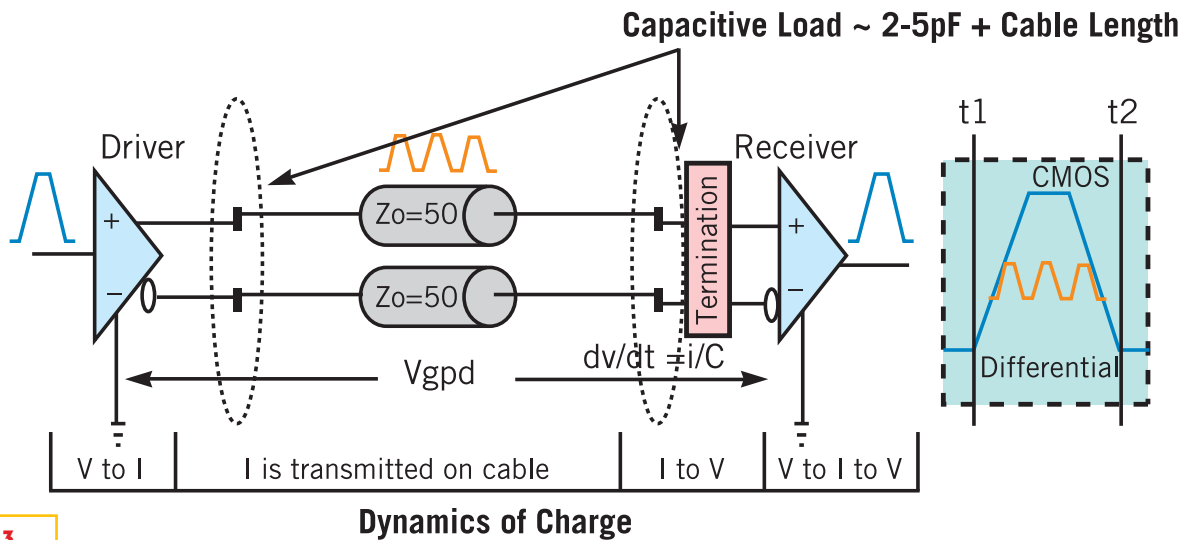


Figure 3

Typical signalling scheme with current mode driver and voltage mode receiver

consumption in the output driver. Increasing the EMI is another big sacrifice that makes it possible to achieve such high throughput (1.65 Gbps). 8b/10b encoding is needed to obtain minimised transition and DC-balanced character.

One could call this type of scheme a “pseudo-current interface”, since it is necessary to convert the output current of the driver to voltage at the receiver side so it can be received correctly. Of course, once voltage comes into play, parasitic capacitance will effectively hamper the throughput for such I/Os as TMDS and LVDS, governed by the relationship $i = C \cdot dV/dt$.

For constant-current output from drivers, the higher the parasitic capacitance in the data path, the lower the edge rate. This results in limited throughput. Consequently, the capacitance effect along the data path not only contributes to higher power consumption but also heavily limits the data throughput. Parasitic capacitance here includes ESD capacitance, gate input capacitance, cable capacitance and stub/connector capacitance.

Unlike TMDS, LVDS requires the flow of a balanced current (3.5 mA) in the loop between the plus and the minus line as shown in **Figure 2**. The direction of the current is dependent on the input logic of the drivers. This 3.5 mA current creates a voltage drop over the termination resistor (100 Ω) at the receiver side, which is sensed by the internal receiver ampli-

fier and interpreted as logic “1” or “0”, depending on the direction of the current flow.

Meanwhile, the opposite flow of the currents in the loop generates magnetic fields which cancel each other if the media, such as traces, are laid out close enough. Since the LVDS signal’s edge rates (typically 1 V/nsec) are much slower than TMDS, this reduces the di/dt , leading to smaller electromagnetic emissions. Of course, traditional LVDS technology offers lower throughput than TMDS due to reduced edge rate, which nonetheless is rewarded with less EMI. Efforts are in place to further reduce the LVDS swing to achieve lesser EMI and power consumption for portable and consumer electronics. However, this comes at the cost of lower throughput, reduced noise margin, and less cable driving capability.

As the video display market migrates to high definition with more resolution than UXGA, data throughput between display controllers and LCD modules in both portable and consumer electronics, such as cell phones and LCD TVs, is approaching the bottleneck that exists in the current single-ended TTL technology. Despite efforts to extend their capabilities, today’s differential solutions will have a difficult time meeting all the key specifications of such a design.

Although it is very difficult to define a perfect interface technology to meet all of the key specifications simultaneously,

by better understanding the signalling schemes we can reduce the interdependence between the important specification parameters. This offers a route to lower power and lower EMI signalling technology for portable and consumer designs. A general block diagram, such as that shown in **Figure 3**, can represent the most critical areas that are limited by the performance of today’s technologies.

All of these technologies use similar current mode drivers on the driver side. A current source is used to source the current out of the driver. This current flows through the cable and then through the terminating resistance, thus creating a voltage drop which is sensed by a voltage amplifier. To create logic “1” or “0”, the direction of the current flowing through the terminating resistor is changed using some properly-sized switches at the driver. Thus, terminating resistance not only helps in terminating the cable which acts as a transmission line, but it also creates the differential voltage that the receiver must sense. Usually, the receiver is a trans-conductance amplifier followed by an I-V conversion stage. The sensitivity of the receiver depends on the size of the input devices and the signal swing at the receiver, which, in turn, depends on the current sourced by the driver. The noise margin on the receiver side constrains the minimal allowable signal swing. For longer cables, the signal attenuates as it moves along the length of the cable due to the resistive drop from the cable itself. This effect is

particularly severe at high frequencies, as resistance increases due to the skin effect which consequently attenuates the signal at the receiver and degrades the noise margin. For a lesser signal swing, the noise margin will depend on the rate of change of the input signal and the minimum input swing required to switch the receiver or the sensitivity of the receiver.

One way to increase the sensitivity of a typical CMOS voltage receiver is to increase the size of the input devices. However, this will increase the input capacitance and degrade the slew-rate, which will ultimately set the limits on power and speed requirements to transmit the signal reliably.

Signal swing determines the noise margin and the power while the edge rate determines the speed. Signal swing at the receiver is in turn determined by $i \times R$, where i is the current sourced by the driver and R is the terminating resistance. EMI is dependent on both the edge rate and the signal swing. A slow edge rate with less signal swing will give less EMI. Edge rate (slew rate), dv/dt , at the receiver is primarily determined by i/C . Capacitance C is the sum of capacitance of the cable, input device, bond pad, pin, and other parasitics and strays. Reducing i will require a bigger input device to achieve the same noise margin which will increase the input capacitance, and thus reduce and dv/dt limit the speed. To solve these problems, it is imperative to address fundamental constraints in

the signalling technology. Most of these constraints originated from the requirements on the receiver side.

CURRENT TRANSFER LOGIC

What would happen if the current output from the driver were not converted to voltage and the receiver were capable of taking the current directly? This would eliminate the trans-impedance amplifier in the receiver, which would not only reduce the propagation delay, but would also greatly diminish the effect of parasitic capacitance on the channel bandwidth. This model will require a fundamental shift in the signalling technology by replacing the voltage mode receive circuit with a current mode receive circuit.

A current-sensing circuit can be designed to work with low input currents without compromising the noise margin. If some mechanism can reliably sense the current sourced by the driver and make the sensing process less dependent on the capacitance, it should be able to guarantee high speed at much less swing, which leads to less power consumption. This mechanism signifies a “true-current transfer” scheme differentiating from traditional “pseudo-current schemes” such as TMDs and LVDS technologies.

This current-transfer scheme forms the basis of Current Transfer Logic (CTL). The key point is to replace the high-input impedance of the voltage amplifier with a low-input impedance

current-sensing circuit followed by an I-V conversion stage to drive the digital logic. An immediate advantage of using a differential current-sensing circuit will be very low voltage swing, leading to reduced current spikes and low EMI. Work in memories has demonstrated that current-mode signals are much less affected by the load capacitance and can provide significant performance improvement over the voltage mode signals (Reference 1).

Figure 4 shows a typical interface system employing CTL. Conceptually, the current signal transferred between the driver and the receiver is sensed with a current-sensing circuit. Depending on the requirements, the current-sensing circuit can also be designed to terminate the transmission media. Since the receiver is designed to sense the current, we can afford to transmit very low current, which is typically not possible using a voltage mode receiver. LVDS technology derives its power and EMI advantage by matching the currents in the forward and return paths. In CTL, the current in the forward direction is I , while the current which loops back to the driver is $0.5 \times I$. The current change in both the lines to achieve logic “1” or logic “0” is $0.5 \times I$ in opposite directions, thus cancelling the magnetic field generated. Due to the low input impedance of the receiver, the remaining 50% of current I is absorbed in the receiver. Depending on the direction of the current flow, one pin (plus or

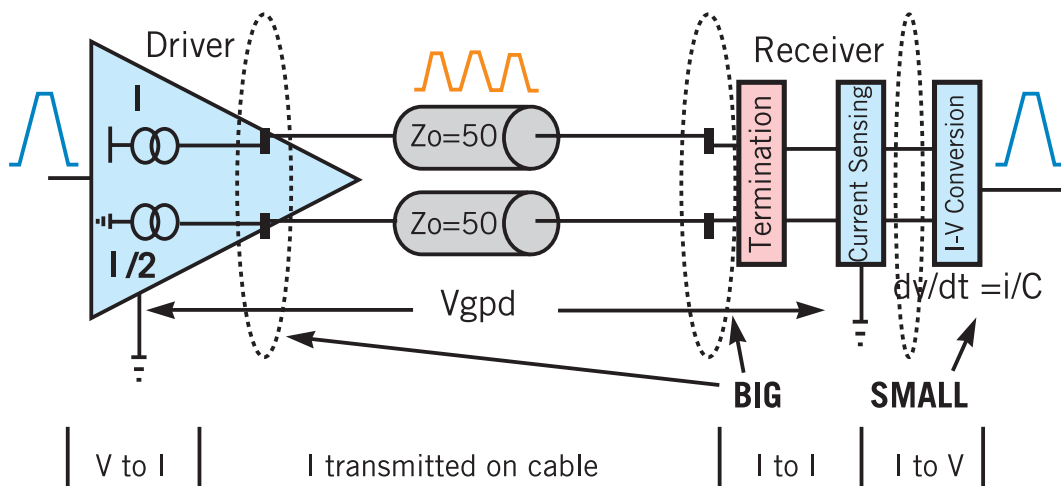


Figure 4

Typical CTL signalling scheme

minus) of the receiver will absorb more current than the other. This will create a differential current between the positive and negative pins. Current gain is not needed at the input stage, and unity gain can be employed to transfer the differential current from heavily-loaded input nodes to a lightly-loaded node internal to the chip. Subsequently, differential current is multiplied, if required, before the current-to-voltage transformation using a simple trans-conductance stage. Low-to-high impedance transformation takes place inside the chip, where the capacitive load is not big enough to affect the voltage signal.

Low input impedance is ideal for current processing and much less dependent on capacitive loading, while the digital circuit that follows the analogue input amplifier needs to be driven by a voltage at its high input impedance. Using the CTL technique avoids current-to-voltage conversion at the high capacitive input node and allows current-to-voltage conversion to take place at a point where capacitance is insignificant. This helps to achieve high throughput and enables transferring the signal at very low power, specifically when compared to LVDS and TMDS technologies. Similar to LVDS, for cables with low dispersive loss, it is either possible for the receiver to set the total common-mode value, or for the driver to force it. The return current helps in biasing the receiver around its common-mode value. It is possible to design the $0.5 \times I$ return current and the current the receiver absorbs to track the current that the driver sources, thus providing a good common-mode range to accommodate the potential ground mismatch between drivers and receivers. Due to the fact that receiver can take the current input directly, the input threshold voltage of receiver is not as critical as it is in TMDS and LVDS interfaces. With a smaller swing, the slew rate can have an even bigger range for the same throughput. With a slower edge rate and less power consumption, one can transfer the same bandwidth of data with much less EMI and channel latency if the receiver has current-sensing capability.

EXPERIMENTAL TRIALS

To prove the concept with basic circuit techniques, researchers designed a pair of

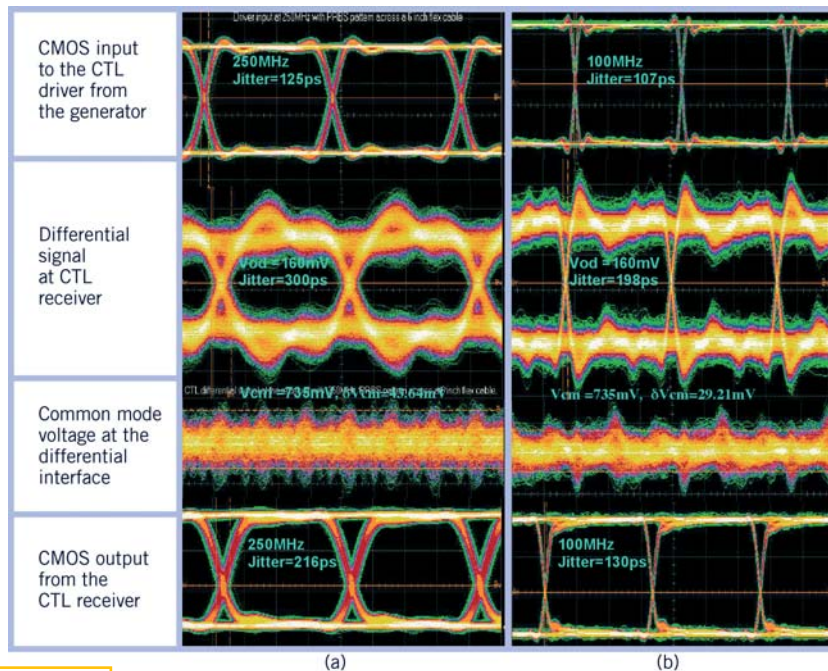


Figure 5

Eye-diagram with PRBS pattern at (a) 250MHz and (b) 100MHz

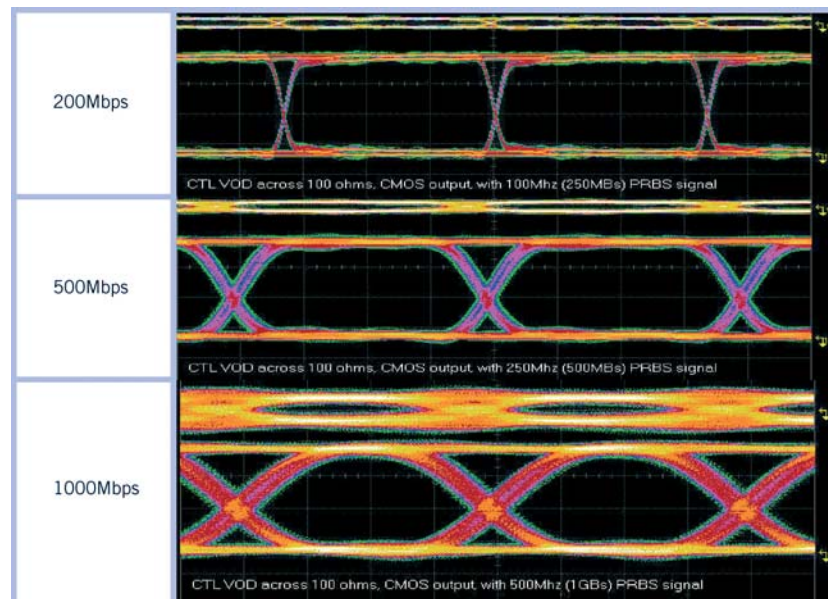


Figure 6

CMOS output from the CTL receiver demonstrates excellent eye-opening capability (data was collected across 6 inches of flex cable using multiple PRBS input)

LVC MOS-to-CTL and CTL-to-LVC MOS translators. For this experiment, they developed a CTL driver to source 1 mA of current and sink 0.6 mA of current. The transmission line was terminated with a 100- resistance across the receiver input.

They designed the receiver to take in the remaining 0.4 mA of current and generate a swing of 65 mV across its input, and they placed much emphasis on comparing CTL with the reduced-swing LVDS technology (250 instead of 350 mV).

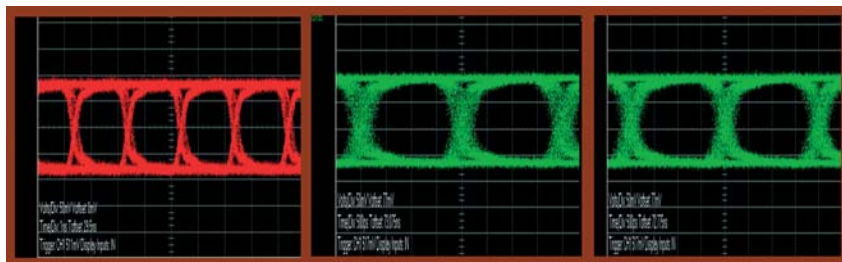


Figure 7

500MB/s signal through (a) 24 inches of 18-channel flex cable, $T_I=400ps$ (b) 30 feet of twisted pair, $T_I=465ps$ (c) 50 feet of twisted pair (other lines tied to ground), $T_I=501ps$

To make the comparison as accurate as possible, they designed the prototype CTL translator chipset to fit exactly in the same footprint as an existing reduced-swing LVDS translator chipset. They changed only the analogue front-end of the driver and receiver while keeping the remainder of the digital and analogue circuits identical. Thus, with identical boards and the socket and test set up in place, the difference in key specifications comes only from the difference in the interface signalling technique.

POWER AND THROUGHPUT

CTL derives its power and speed advantage from the low loop current of the current-sensing receiver. With less than one-fourth the swing of the corresponding LVDS approach, the DC power dissipation in the driver stage reduces dramatically. Due to the smaller drive current and a common-mode-generating receiver, CTL doesn't require a powerful pre-driver and a common-mode feedback circuit, which leads to dynamic power saving. Since current-to-voltage conversion is done at a reduced-capacitance node, power requirements on the receiver side are not restrictive. Reduced swing also leads to higher speeds. Furthermore, it is possible to design the current-sensing receiver to be sensitive enough to respond to differential current of only a few microamperes—resulting in very high speeds, while reducing power consumption. In a translator design, the LVCMOS side of the signal path is the main element that limits speed.

Since CTL is fundamentally different from LVDS at the receiver input, it makes more sense to compare bit error rate instead of comparing the voltage signal at

the differential I/O. However, for completeness, **Figure 5** shows an eye-diagram of a CTL signal at 250 and 100 MHz at the differential I/O, as well as at the CMOS output. The data was collected with a PRBS data pattern running through 6 inches of flex cable (typical of cell phone applications) with a CTL driver and receiver paired.

With throughput of 200 Mbps (100 MHz), the additive jitter of the CTL driver and receiver is only 23 psec peak to peak. The common-mode variation of the driver output is only 29.21 mV. This also leads to the conclusion that for the same speed and eye-opening, CTL takes only 50% of the power compared to reduced-swing LVDS, 70% of power versus traditional LVDS and at least 90% less power compared with TMDS technology. The impact of this reduction in power becomes significant in high-throughput applications like SerDes (serialiser/deserialiser) deployed between the LCD display and the base-band processor. In a specific SerDes architecture, using CTL as the serial I/O can provide up to 30% power savings over reduced-swing LVDS I/O.

CTL offers excellent eye-opening capability to achieve high throughput at low power due to its current-sensing inputs. A voltage receiver, as in LVDS, will require complex equalisation techniques to detect the data reliably from a closed eye. Further equalisation needs to be adaptive for different cable lengths. With CTL, easily-implemented circuit techniques at the input sensing nodes provide the same eye opening. Data collected using PRBS input at different data rates yield the waveforms shown in **Figure 6**.

NOISE MARGIN AND DRIVE

As explained earlier, noise margin carries a direct trade-off with drive capability. CTL is inherently capable of driving very long cables with little attenuation due to the current-sensing circuit present at the far end. As long as there is no significant dispersion loss in the cable, the current reaching the receiver at the far end will remain constant, according to Kirchoff's Current Law. Since current received at the end of the link is not attenuated during transmission as is voltage in the case of LVDS, designers can use CTL over longer cable length—it still provides reliable signal detection. **Figure 7** shows eye diagrams over various distances and cable types with 500 Mbps PRBS data.

EMI AND SUSCEPTIBILITY

As CTL is differential in nature and employs low signal swing-edge rate, it should—according to the reasoning outlined above—provide good EMI performance. The emissions from CTL were compared with LVDS, reduced-swing LVDS (LpLVDS) and TTL, on a 250-MHz input signal over a 10cm-long flex cable, typical for a cell phone application. Observed from the magnetic emission collected by a near-field probe, CTL technology on average delivers EMI that is over 10 dB lower than LVDS technology and 20 dB less than TTL signalling scheme. This is achieved with a power consumption of only 1 mA (typical) for each channel, which is much less than the 3.5 mA per channel for LVDS technology and 10 mA for TMDS interfaces.

REFERENCES

1. "Current Mode Techniques for High Speed VLSI Circuits with Applications to Current Sense Amplifier for CMOS SRAMS," Seevinck et al, IEEE Journal of Solid State Circuits, vol. 26, Nr 4, April 1991, p. 525-535.
2. "A 1-Gb/s Bidirectional I/O Buffer Using the Current-Mode Scheme," Sim et al, IEEE Journal of Solid State Circuits, vol. 34, Nr 4, April 1999, p. 529-535.

AUTHORS' BIOGRAPHY

Pravas Pradhan and Jeff Ju are Staff Application/Design Engineers at Fairchild Semiconductor.